Lab7
CS211
Arithmetic Circuits and Units

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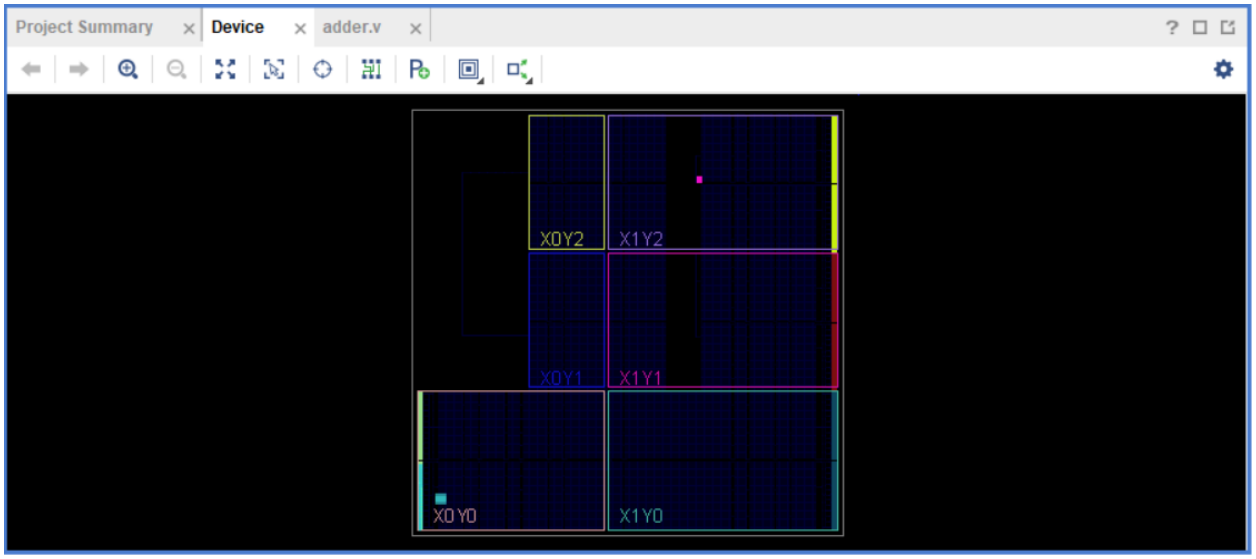
Roll No-2106339

1.Adder



DSize-8

Resource	Utilization	Available	Utilization %
LUT	8	53200	0.02
IO	24	200	12.00

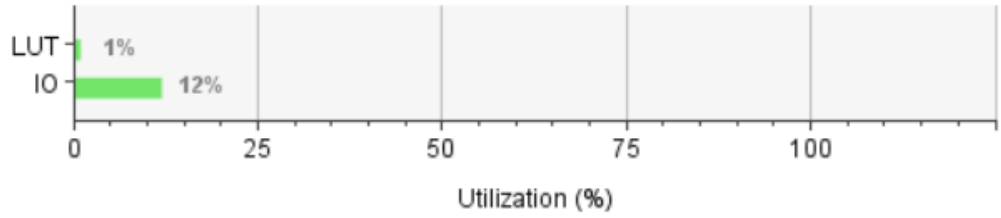


Fig-1.1 Adder utilization

Tcl Console

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Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

1. Setup Path Characteristics 1-1
---------------------------------

+--------------------------+------------------------------+
|      Characteristics     |            Path #1           |
+--------------------------+------------------------------+
| Requirement              |                        0.000 |
| Path Delay               |                        8.614 |
```

Fig-1.2 Adder Delay

DSize-16

Resource	Utilization	Available	Utilization %
LUT	16	53200	0.03
IO	48	200	24.00

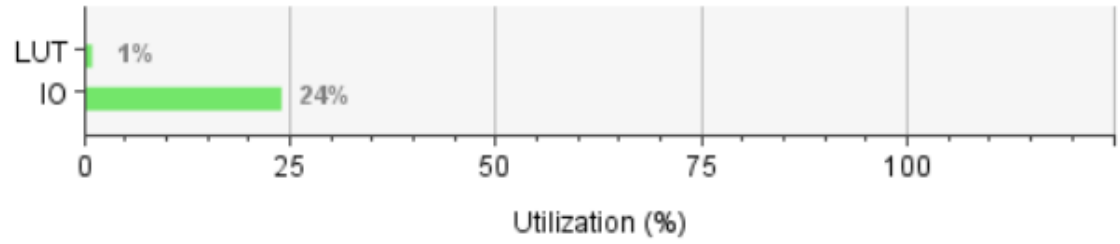

Fig-1.3 Adder utilization

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Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

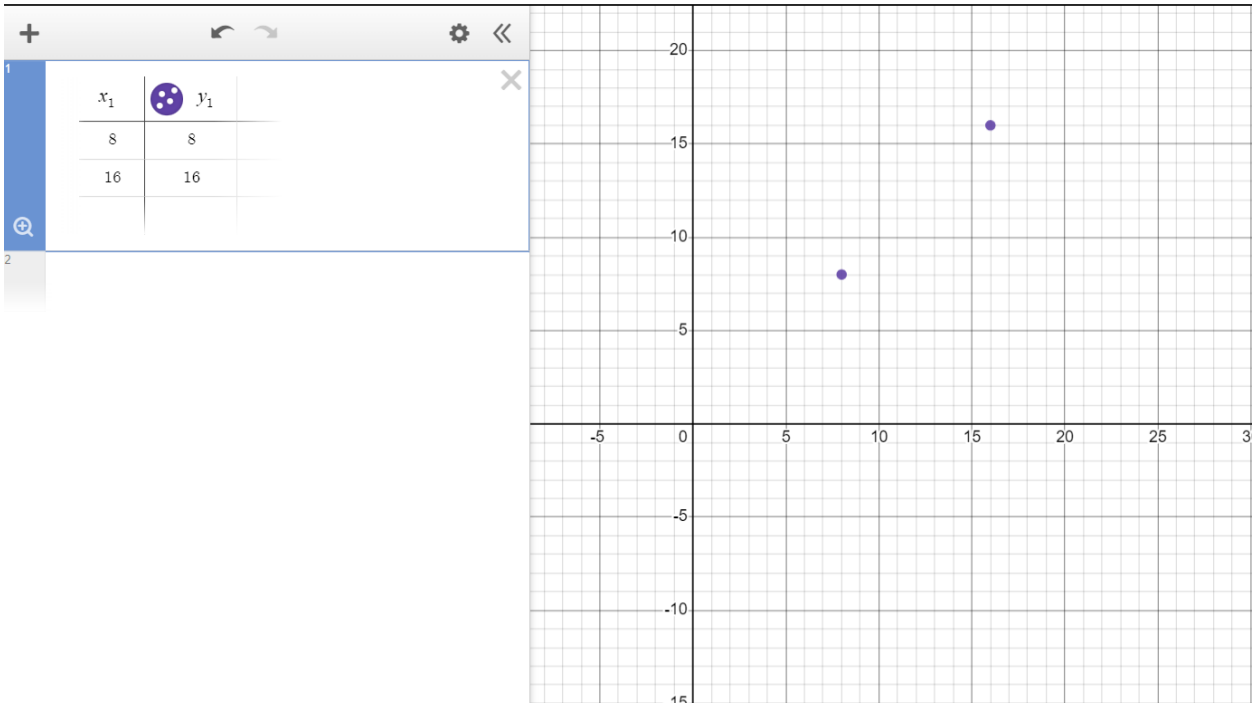
1. Setup Path Characteristics 1-1
---------------------------------

+--------------------------+-----------------------------------------------+
|      Characteristics     |                    Path #1                    |
+--------------------------+-----------------------------------------------+
| Requirement              |                                         0.000 |
| Path Delay               |                                         9.788 |
```

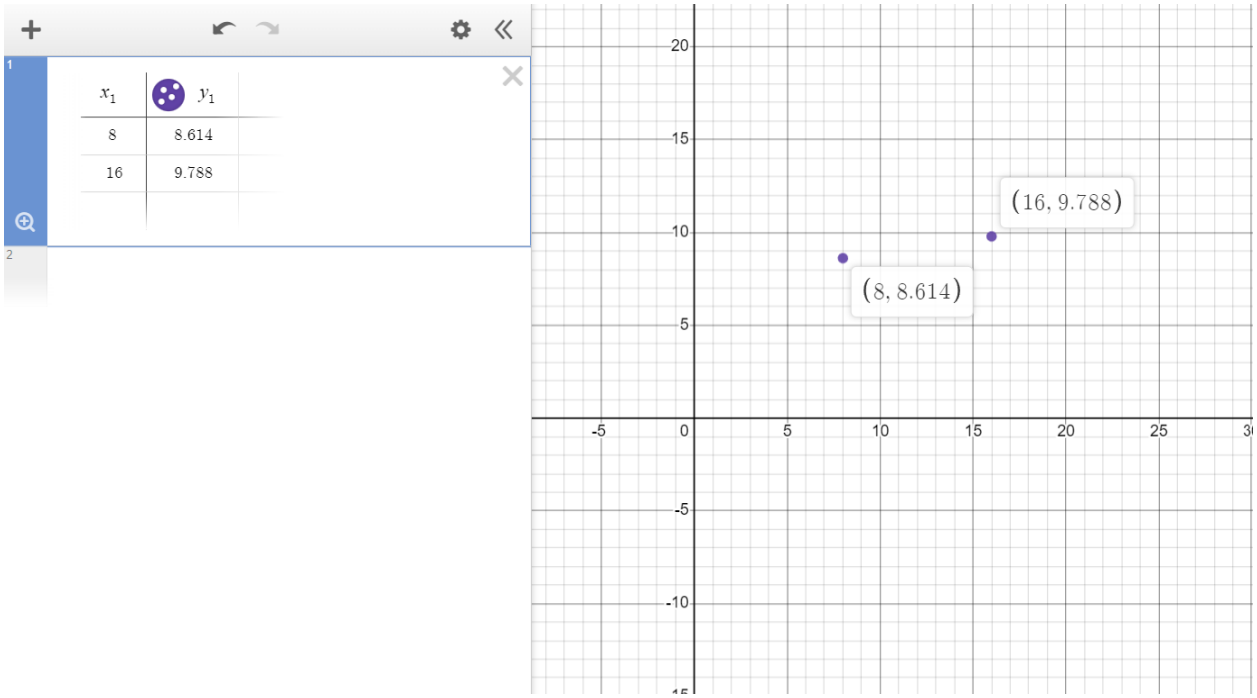
Fig-1.4 Adder Delay

Parameter: DSIZE	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	8	8.614
16	16	16	9.788

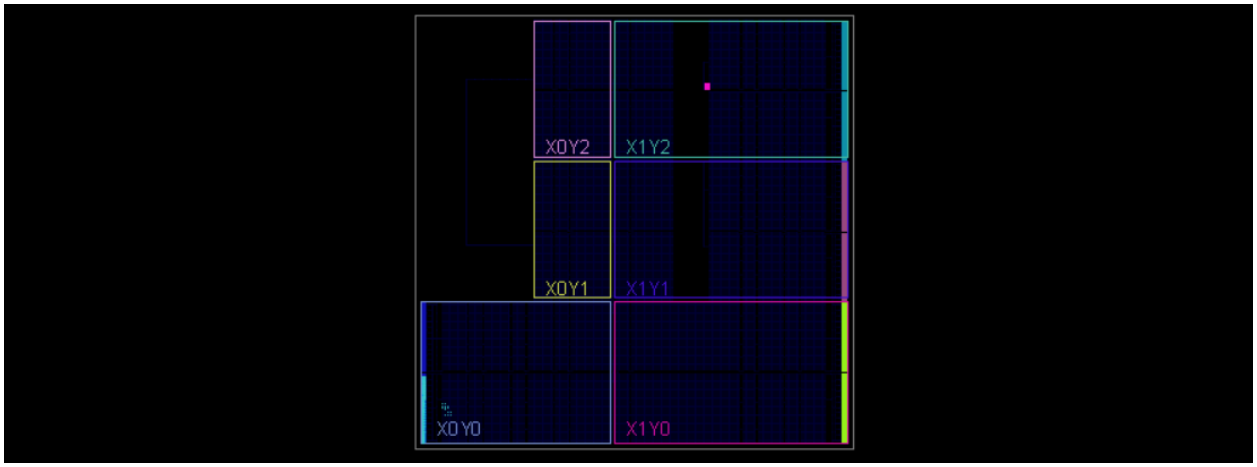
area (vs) bit-width



delay (vs) bit-width



2.Multiplier



DSize-8

Resource	Utilization	Available	Utilization %
LUT	34	53200	0.06
IO	24	200	12.00

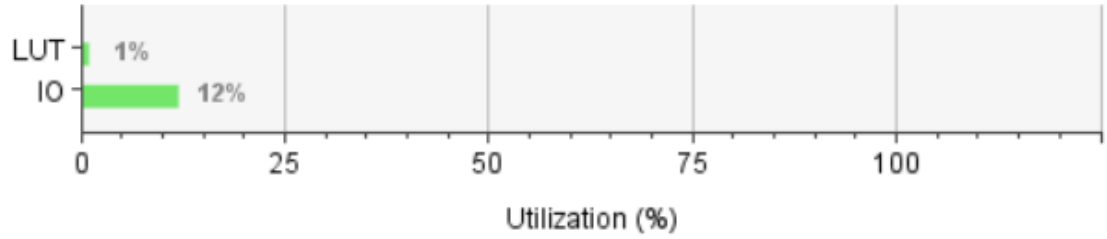


Fig-2.1 Multiplier Utilization

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Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

1. Setup Path Characteristics 1-1
---------------------------------

+--------------------------+-----------------------------------------------------+
|      Characteristics     |                       Path #1                       |
+--------------------------+-----------------------------------------------------+
| Requirement              |                                              0.000 |
| Path Delay               |                                             11.898 |
```

Fig-2.2 Multiplier Delay

DSize-16

```
+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |  151 |     0 |     41000 |  0.37 |
|   LUT as Logic          |  151 |     0 |     41000 |  0.37 |
```

Fig-2.3 Multiplier Utilization

```
Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

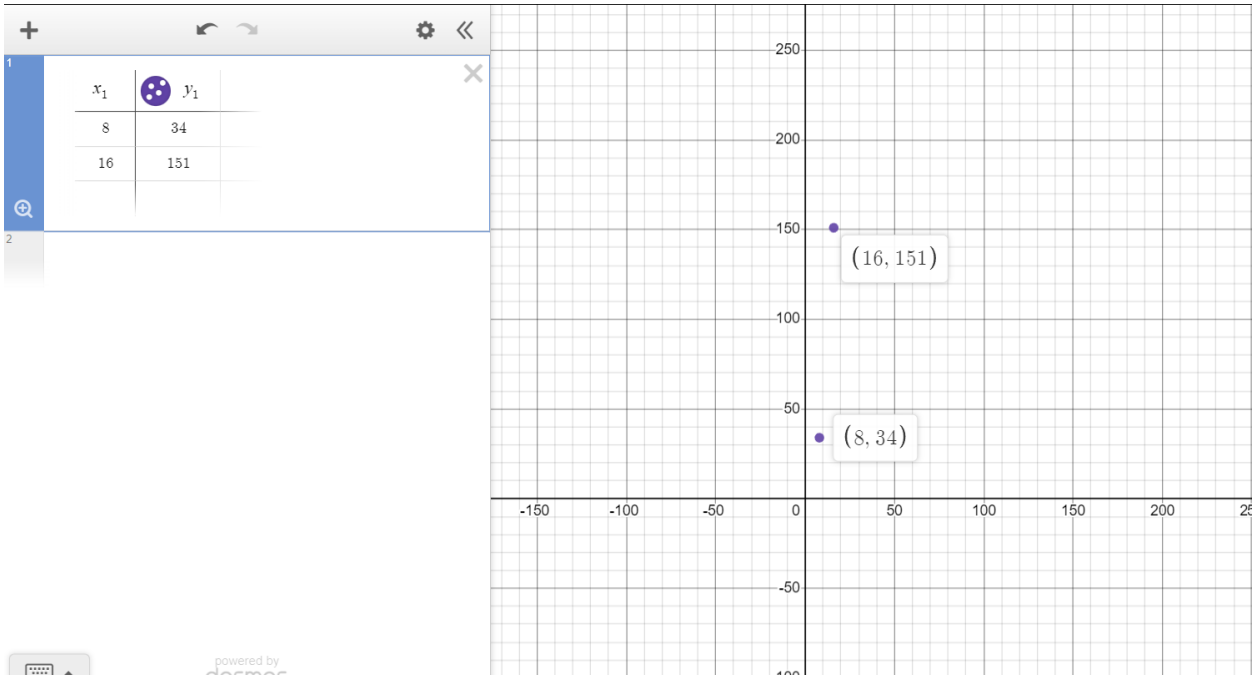
1. Setup Path Characteristics 1-1
---------------------------------

+---------------------------+-------------------------------------------------------------------------------+
|      Characteristics      |                                    Path #1                                    |
+---------------------------+-------------------------------------------------------------------------------+
| Requirement               |                                                                         0.000 |
| Path Delay                |                                                                        16.771 |
```

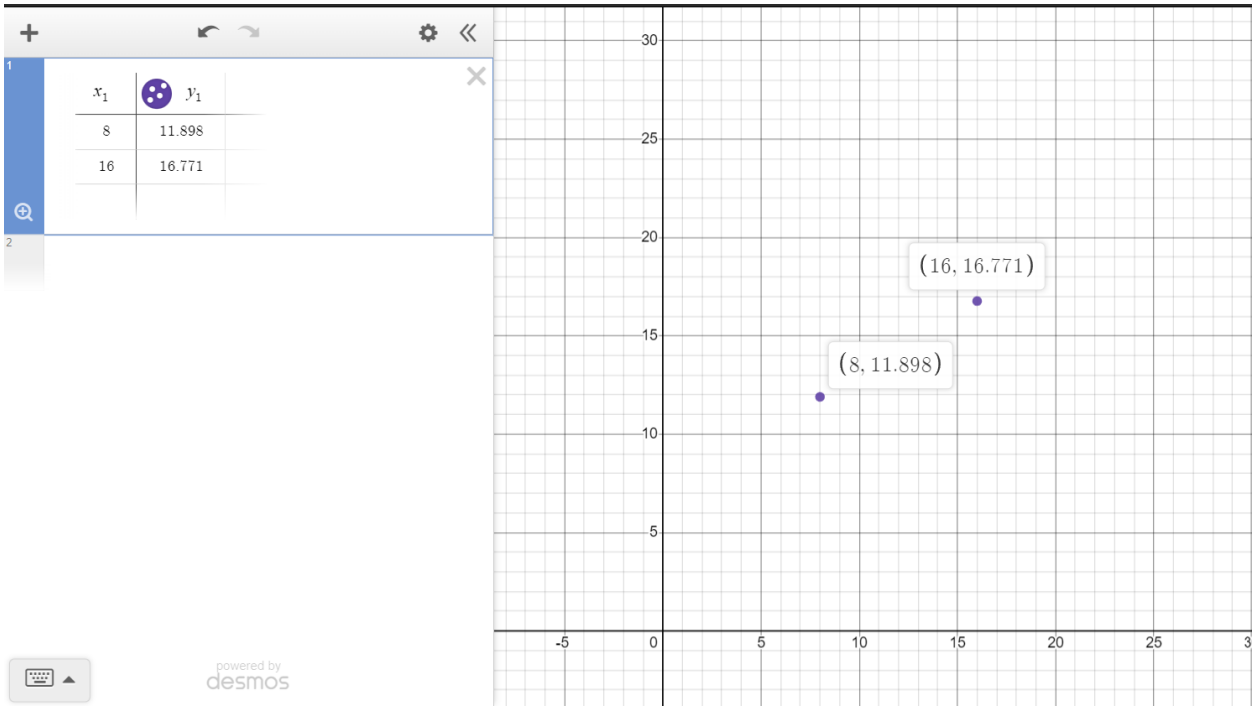
Fig-2.4 Multiplier Delay

Parameter: DSIZE	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	34	11.898
16	16	151	16.771

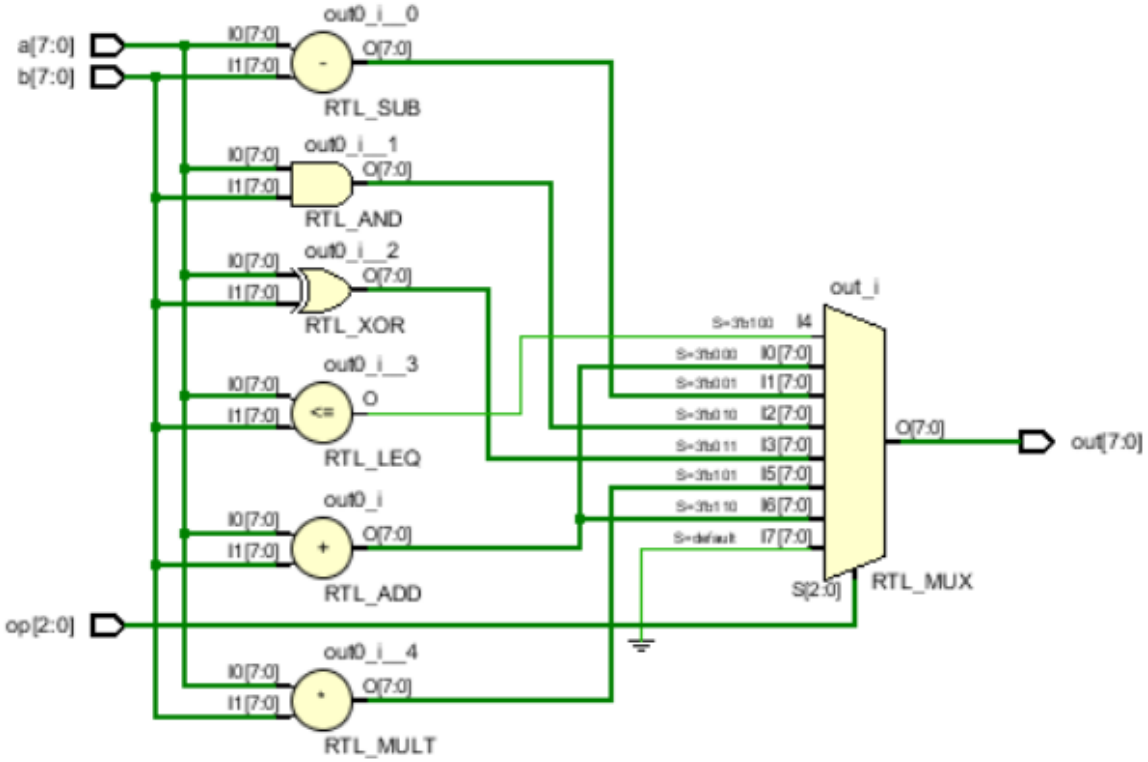
area (vs) bit-width



delay (vs) bit-width


x_1
y_1
8
11.898
16
16.771
(16, 16.771)
(8, 11.898)
powered by
desmos

3.ALU


a[7:0]
b[7:0]
op[2:0]
out0_i__0
RTL_SUB
out0_i__1
RTL_AND
out0_i__2
RTL_XOR
out0_i__3
RTL_LEQ
out0_i
RTL_ADD
out0_i__4
RTL_MULT
out_i
RTL_MUX
O[7:0]
out[7:0]
S[2:0]

DSize-8

Resource	Utilization	Available	Utilization %
LUT	71	53200	0.13
IO	27	200	13.50

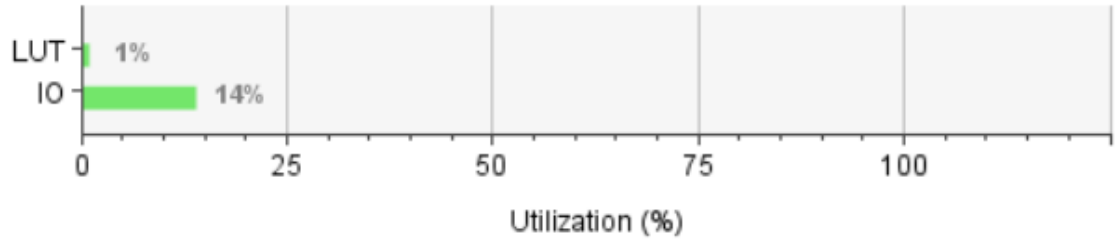


Fig-3.1 ALU Utilization

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Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

1. Setup Path Characteristics 1-1
---------------------------------

+--------------------------+-------------------------------------------------------------+
|      Characteristics     |                          Path #1                            |
+--------------------------+-------------------------------------------------------------+
| Requirement              |                                                      0.000 |
| Path Delay               |                                                      9.115 |
```

Fig-3.2 ALU Delay

DSize-16

Resource	Utilization	Available	Utilization %
LUT	224	53200	0.42
IO	51	200	25.50

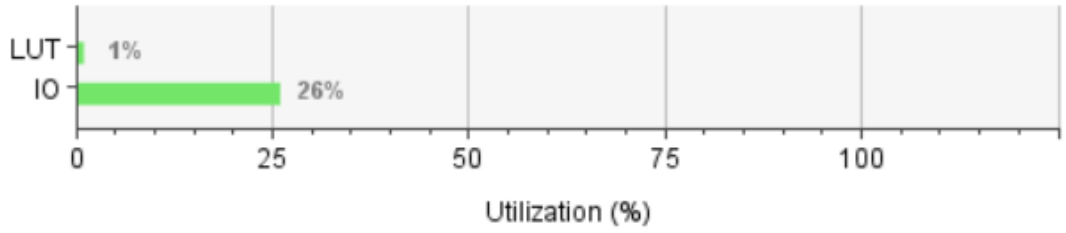

Fig-3.3ALU Utilization

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Report Design Analysis

Table of Contents
-----------------
1. Setup Path Characteristics 1-1
2. Logic Level Distribution

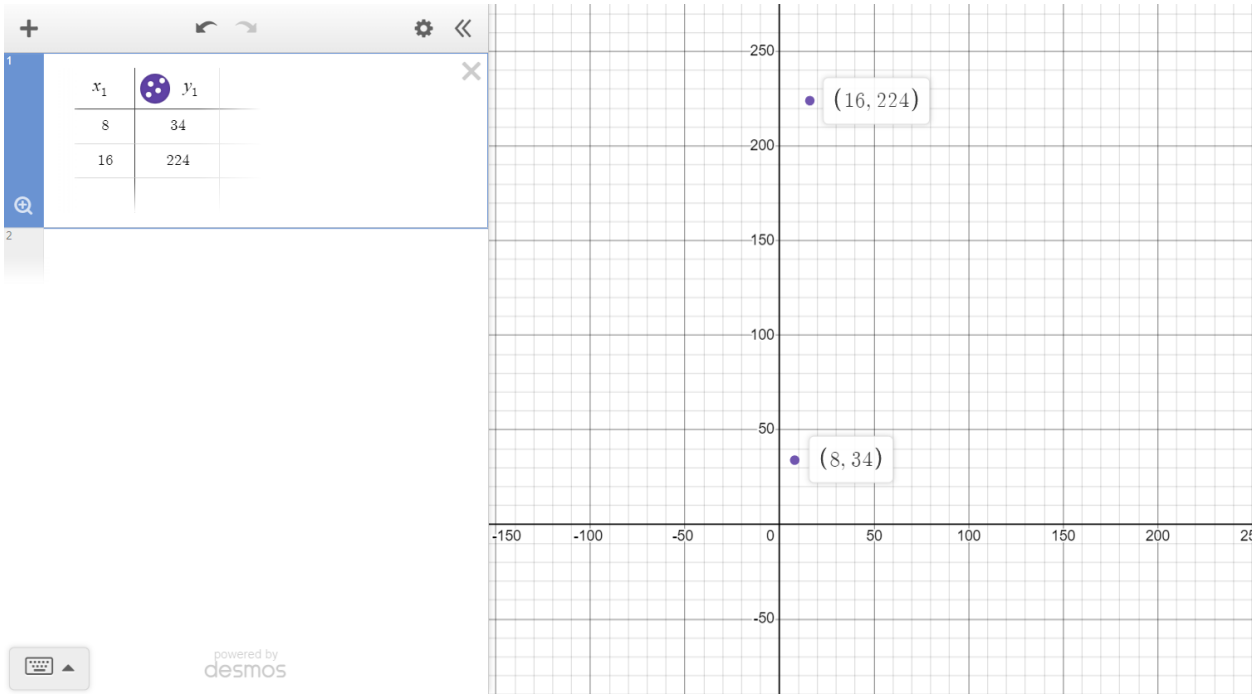
1. Setup Path Characteristics 1-1
---------------------------------

+--------------------------+-------------------------------------------------------------------------+
|      Characteristics     |                                 Path #1                                 |
+--------------------------+-------------------------------------------------------------------------+
| Requirement              |                                                                   0.000 |
| Path Delay               |                                                                  11.819 |
```

Fig-3.4 ALU Delay

Parameter: DSIZE	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	34	9.115
16	16	224	11.819

area (vs) bit-width



delay (vs) bit-width