# Lab8 CS211

# **Lab8-Datapath Implementation**

Name-Pranav Tambe Roll No-2106339

# **Evaluation 1**

Q.1]

DSize=32

NREG=4

#### 1. Slice Logic

-----

++			+-		+-		+-		+-		+
1								Available			
+-			+-		+-		+-		+-		+
-	Slice	LUTs*	l	186	I	0	I	53200	I	0.35	I
1	LUT	as Logic	I	186	I	0	I	53200	I	0.35	I
1	LUT	as Memory	I	0	I	0	I	17400	I	0.00	I
1	Slice	Registers	I	128	I	0	I	106400	I	0.12	I

## Utilization

## NREG=8

Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

\_\_\_\_\_

+	+		+
Characteristics	1	Path #1	1
+	+		+
Requirement	1	0.000	)
Path Delay	1	16.513	3

#### 1. Slice Logic

-----

+				+-		+-		+		+-		+
1		Site Ty	mpe I	I	Used	I	Fixed	I	Available	I	Util%	I
+				+-		+-		+		+-		+
1	Slice	LUTs*		ı	302	Ī	0	I	53200	ı	0.57	ı
1	LUT	as Logic	:	I	302	I	0	I	53200	I	0.57	I
1	LUT	as Memor	. Y	I	0	I	0	I	17400	I	0.00	I
1	Slice	Register	:s	ı	256	ı	0	ı	106400	ı	0.24	ı

## Utilization

### NREG=16

Report Design Analysis

# Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

+	+		+
Characteristics	1	Path #1	- 1
+	+		+
Requirement	1	0.	000
Path Delay	1	16.	933

#### 1. Slice Logic

-----

+			+-		+		+		+-		+
1		Site Type	I	Used	I	Fixed	I	Available	I	Util%	I
+			+-		+		+		+-		+
1	Slice	LUTs*	I	502	Ī	0	Ī	53200	I	0.94	I
1	LUT	as Logic	I	502	Ī	0	Ī	53200	I	0.94	Ī
1	LUT	as Memory	I	0	I	0	I	17400	I	0.00	I
1	Slice	Registers	I	512	I	0	I	106400	I	0.48	I

## Utilization

## NREG=32

Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

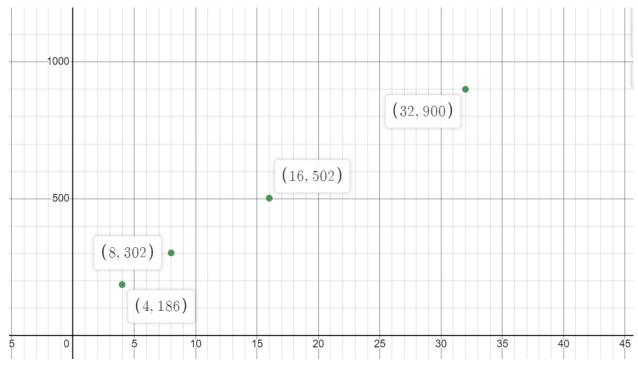
+	+		+
Characteristics	1	Path #1	1
+	+		+
Requirement	1		0.000
Path Delay	1		18.731

# Slice Logic

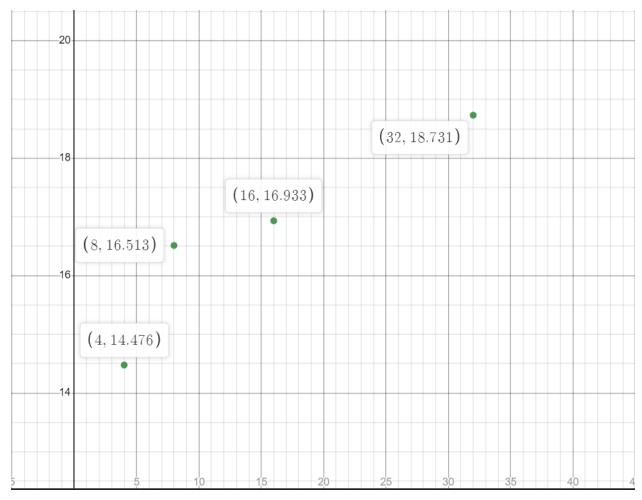
+	++										
1		Site Type	I	Used	I	Fixed	I	Available	ı	Util%	I
+			-+-		+		+-		+-		+
1	Slice	LUTs*	I	900	Ī	0	ı	53200	ı	1.69	ı
1	LUT	as Logic	I	900	I	0	I	53200		1.69	I
-	LUT	as Memory	1	0	I	0	I	17400	ı	0.00	I
-1	Slice	Registers	1	1024	ı	0	ı	106400	ı	0.96	ı

# Utilization

Bit-width of the register (DSIZE)	No. of registers (NREG)	No of register slices used	No of LUT slices used	minimum clock period in ns
32	4	128	186	14.476
32	8	256	302	16.513
32	16	512	502	16.933
32	32	1024	900	18.731



LUT slices (vs) No. of registers (NREG)



Delay (vs) No. of registers (NREG)

# Q.2]

# No of registers =32

### DSize=4

Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

+	+		+
Characteristics	1	Path #1	- 1
+	+		+
Requirement	1	0.00	00
Path Delay	1	10.65	56 I

# Delay

#### 1. Slice Logic

-----

++			+-		+		+		+-		+
1		Site Type	I	Used	I	Fixed	I	Available	I	Util%	I
+			+-		+		+		+-		+
1 3	Slice	LUTs*	I	144	I	0	I	53200	l	0.27	I
1	LUT	as Logic	I	144	I	0	I	53200	I	0.27	I
1	LUT	as Memory	I	0	I	0	I	17400	ı	0.00	ı
1.5	Slice	Registers	ı	128	I	0	ı	106400	ı	0.12	ı

## Utilization

DSize=8

#### Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

+	++
Characteristics	Path #1
+	++
Requirement	0.000
Path Delay	12.620

# Delay

1. Slice Logic

-----

+			-+		-+-		+		+-		+
İ		Site Type	į	Used	į	Fixed	i	Available	į	Util%	į
Ī	Slice	LUTs*	-+ 	252	ï	0	Ī	53200	ī	0.47	ī
-1	LUT	as Logic	1	252	I	0	I	53200	I	0.47	I
- 1	LUT	as Memory	-	0	I	0	I	17400	I	0.00	I
1	Slice	Registers	-	256	I	0	I	106400	I	0.24	I

# Utilization

DSize=16

### Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

+	+	+
Characteristics	1	Path #1
+	+	+
Requirement	1	0.000
Path Delay	1	15.091

# Delay

#### 1. Slice Logic

-----

+-			+		+		+-		+-		+
1		Site Type						Available			
Ī	Slice		1	468		0	Ċ			0.88	
-	LUT	as Logic		468	I	0	I	53200	I	0.88	I
-	LUT	as Memory		0	I	0	I	17400	I	0.00	I
-	Slice	Registers	- 1	512	I	0	I	106400	I	0.48	I

## Utilization

DSize=32

#### Report Design Analysis

#### Table of Contents

-----

- 1. Setup Path Characteristics 1-1
- 2. Logic Level Distribution
- 1. Setup Path Characteristics 1-1

-----

+	++
Characteristics	Path #1
+	++
Requirement	0.000
Path Delay	18.731

# Delay

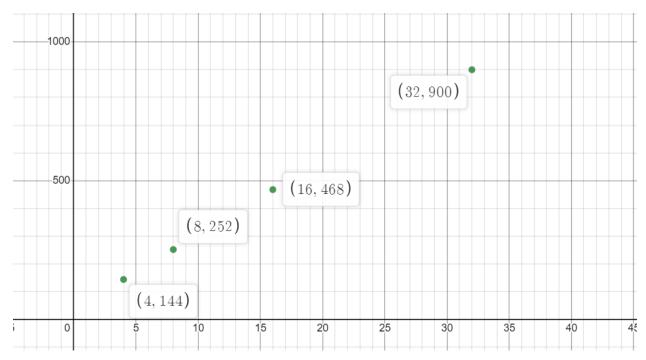
#### 1. Slice Logic

-----

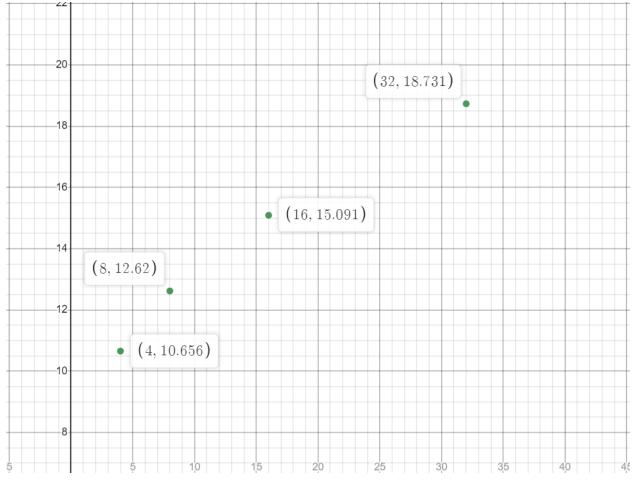
+-		-+		+		+		+-		+
1	Site Type	-	Used	I	Fixed	I	Available	I	Util%	I
+-		-+		+		+		+-		+
1	Slice LUTs*	-	900	I	0	I	53200	I	1.69	I
1	LUT as Logic	-1	900	I	0	I	53200	I	1.69	I
1	LUT as Memory	- 1	0	I	0	I	17400	I	0.00	I
1	Slice Registers	-1	1024	I	0	I	106400	I	0.96	I

Utilization

Bit-width of the register (DSIZE)	No. of registers (NREG)	No of register slices used	No of LUT slices used	minimum clock period in ns		
4	32	128	144	10.656		
8	32	256	252	12.620		
16	32	512	468	15.091		
32	32	1024	900	18.731		



LUT slices (vs) bit-width of register (DSIZE)



Delay (vs) bit-width of register (DSIZE)