Lab8
CS211
Lab8-Datapath Implementation

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Evaluation 1

Q.1]

DSize=32

NREG=4

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Report Design Analysis

Table of Contents
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1. Setup Path Characteristics 1-1
2. Logic Level Distribution

1. Setup Path Characteristics 1-1
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+--------------------------+---------------------+
|      Characteristics     |       Path #1       |
+--------------------------+---------------------+
| Requirement              |               0.000 |
| Path Delay               |              14.476 |
```

Delay

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	186	0	53200	0.35
LUT as Logic	186	0	53200	0.35
LUT as Memory	0	0	17400	0.00
Slice Registers	128	0	106400	0.12

Utilization

NREG=8

Report Design Analysis

Table of Contents

1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	16.513

Delay

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	302	0	53200	0.57
LUT as Logic	302	0	53200	0.57
LUT as Memory	0	0	17400	0.00
Slice Registers	256	0	106400	0.24

Utilization

NREG=16

Report Design Analysis

Table of Contents

1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	16.933

Delay

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	502	0	53200	0.94
LUT as Logic	502	0	53200	0.94
LUT as Memory	0	0	17400	0.00
Slice Registers	512	0	106400	0.48

Utilization

NREG=32

Report Design Analysis

Table of Contents

1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	18.731

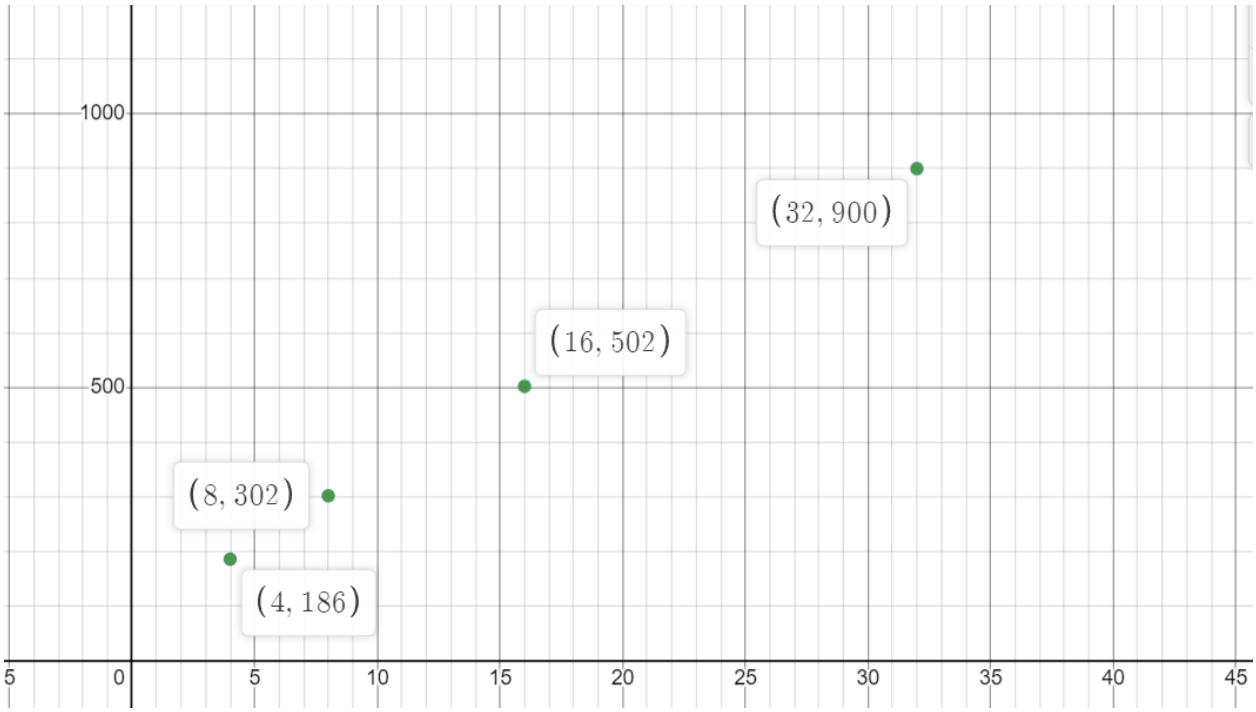
Delay

1. Slice Logic

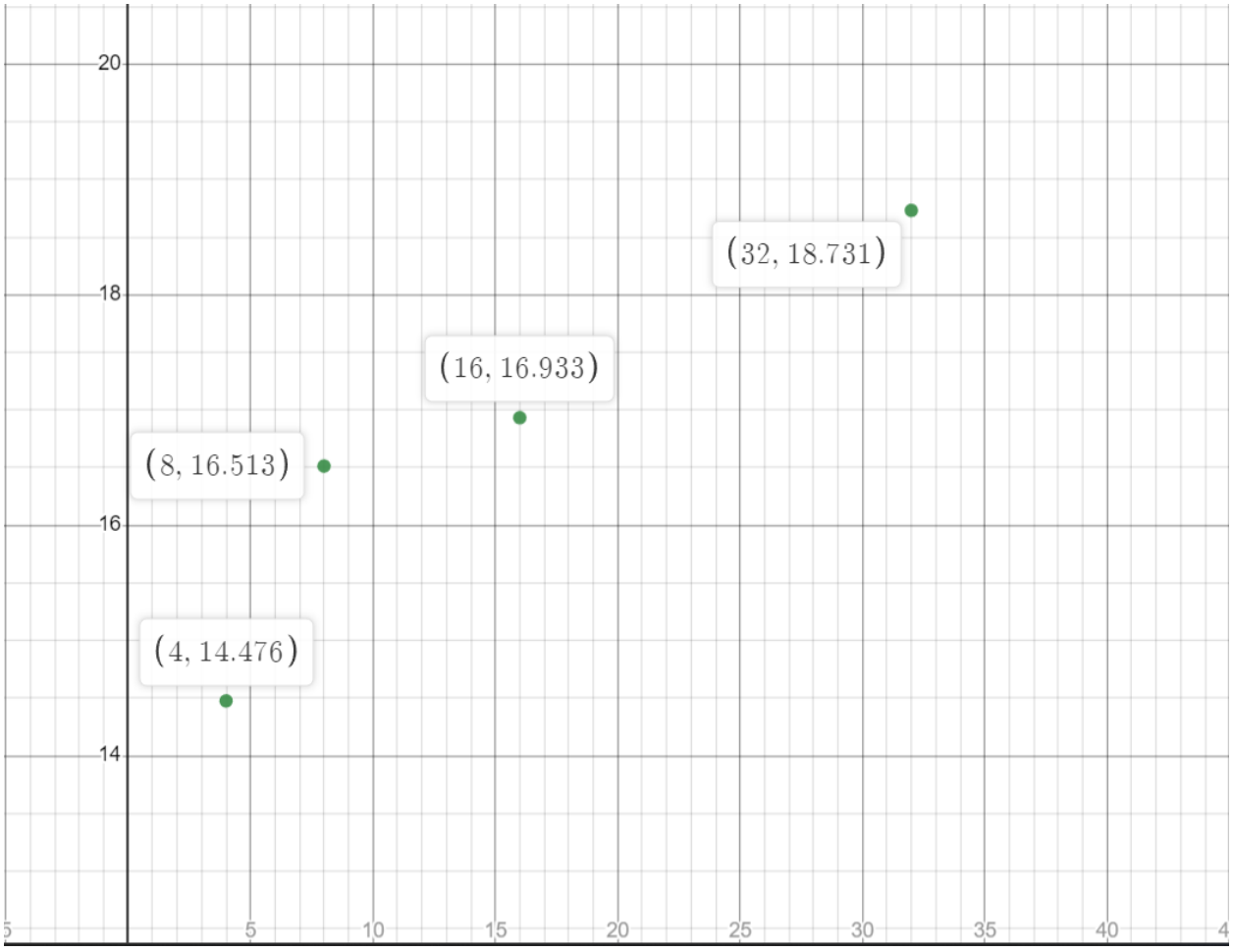
Site Type	Used	Fixed	Available	Util%
Slice LUTs*	900	0	53200	1.69
LUT as Logic	900	0	53200	1.69
LUT as Memory	0	0	17400	0.00
Slice Registers	1024	0	106400	0.96

Utilization

Bit-width of the register (DSIZE)	No. of registers (NREG)	No of register slices used	No of LUT slices used	minimum clock period in ns
32	4	128	186	14.476
32	8	256	302	16.513
32	16	512	502	16.933
32	32	1024	900	18.731



LUT slices (vs) No. of registers (NREG)



Delay (vs) No. of registers (NREG)

Q.2]
No of registers =32

DSize=4

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Report Design Analysis

Table of Contents
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1. Setup Path Characteristics 1-1
2. Logic Level Distribution

1. Setup Path Characteristics 1-1
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+---------------------------+----------------------------------+
|      Characteristics      |              Path #1             |
+---------------------------+----------------------------------+
| Requirement               |                            0.000 |
| Path Delay                |                           10.656 |
```

Delay

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1. Slice Logic
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+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |  144 |     0 |     53200 |  0.27 |
|   LUT as Logic          |  144 |     0 |     53200 |  0.27 |
|   LUT as Memory         |    0 |     0 |     17400 |  0.00 |
| Slice Registers         |  128 |     0 |    106400 |  0.12 |
```

Utilization

DSize=8

Report Design Analysis

Table of Contents
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1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	12.620

Delay

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	252	0	53200	0.47
LUT as Logic	252	0	53200	0.47
LUT as Memory	0	0	17400	0.00
Slice Registers	256	0	106400	0.24

Utilization

DSize=16

Report Design Analysis

Table of Contents
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1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	15.091

Delay

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	468	0	53200	0.88
LUT as Logic	468	0	53200	0.88
LUT as Memory	0	0	17400	0.00
Slice Registers	512	0	106400	0.48

Utilization

DSize=32

Report Design Analysis

Table of Contents
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1. Setup Path Characteristics 1-1

Characteristics	Path #1
Requirement	0.000
Path Delay	18.731

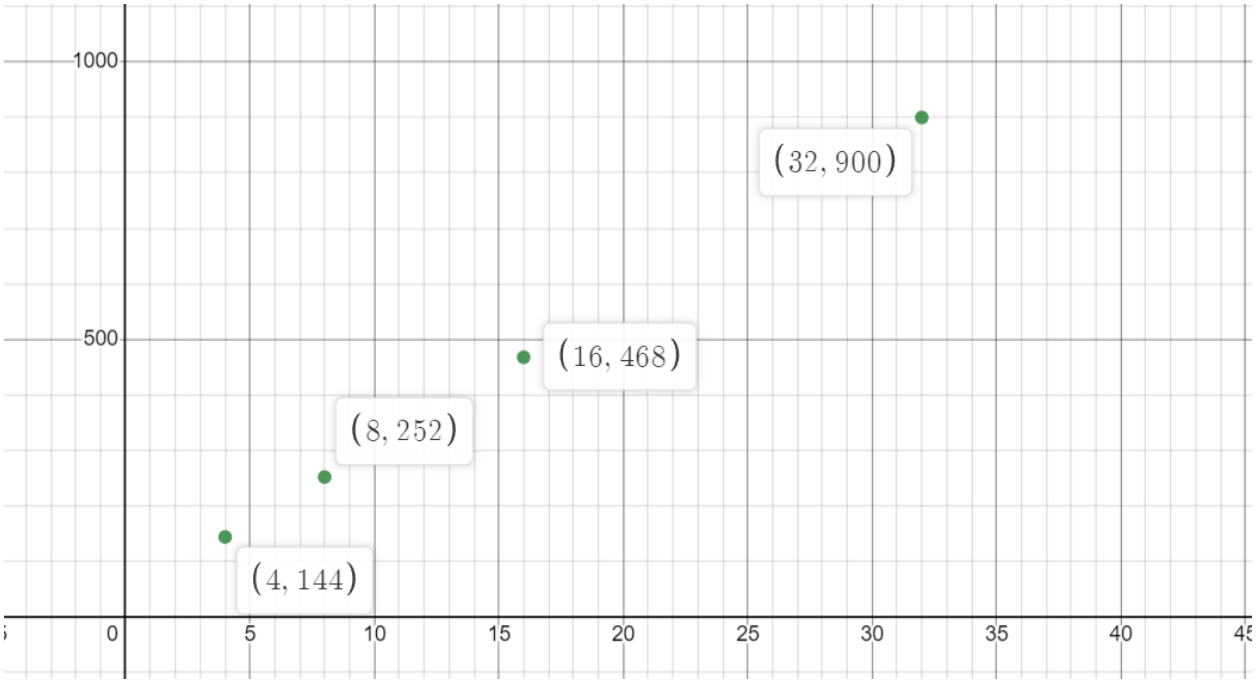
Delay

1. Slice Logic

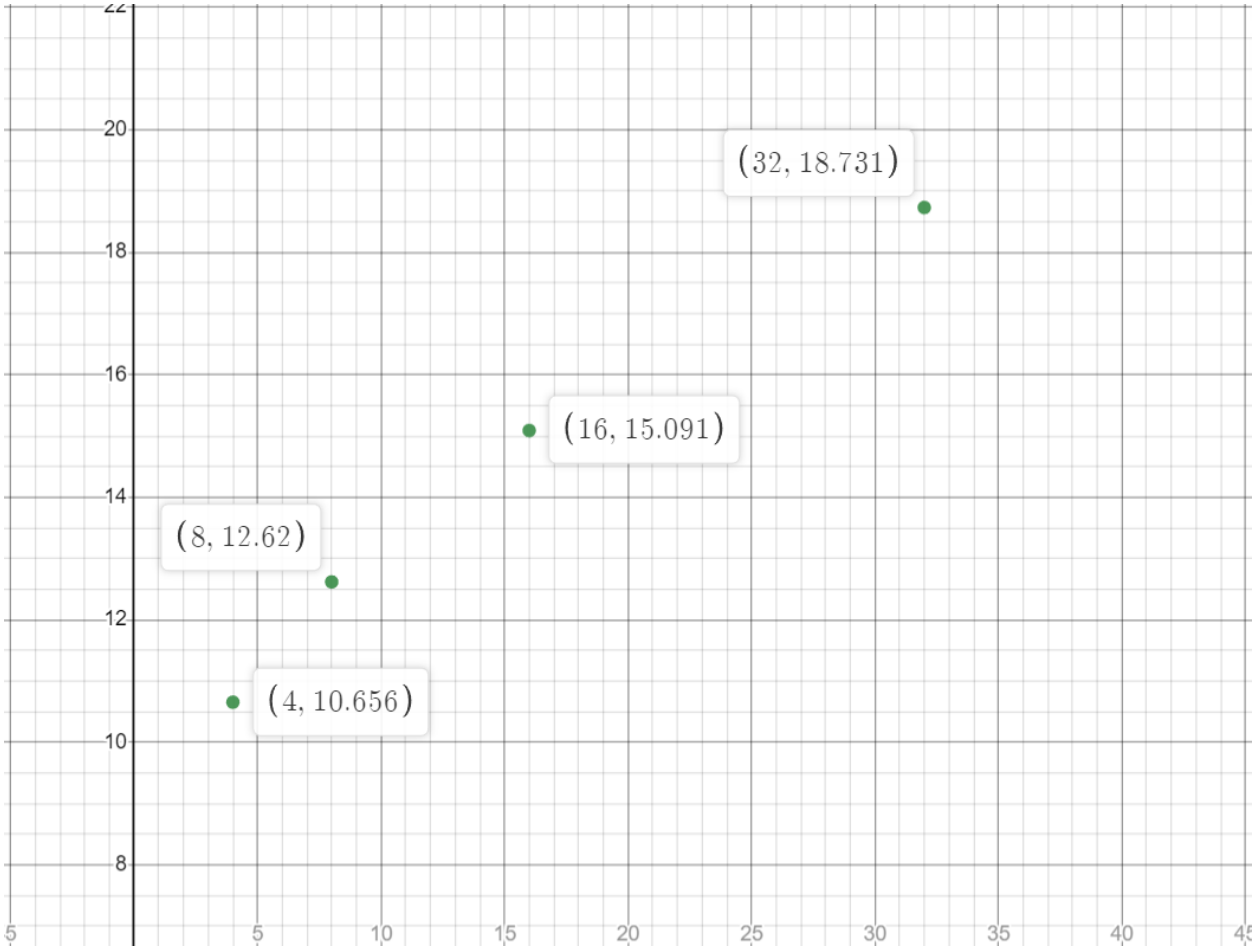
Site Type	Used	Fixed	Available	Util%
Slice LUTs*	900	0	53200	1.69
LUT as Logic	900	0	53200	1.69
LUT as Memory	0	0	17400	0.00
Slice Registers	1024	0	106400	0.96

Utilization

Bit-width of the register (DSIZE)	No. of registers (NREG)	No of register slices used	No of LUT slices used	minimum clock period in ns
4	32	128	144	10.656
8	32	256	252	12.620
16	32	512	468	15.091
32	32	1024	900	18.731



LUT slices (vs) bit-width of register (DSIZE)



Delay (vs) bit-width of register (DSIZE)