

WEEK 7 submission

Department	Computer Science
Campus	RR

Direct Mapping:

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8
Memory Size (power of 2): 64
Offset Bits: 0

Reset Submit

Instruction Load: 25 (in hex)#
8,19,6,25,8,16,35
Gen. Random Submit

Information
Valid bit is 0, therefore CACHE MISS is obtained. Cache is updated with the new dataset.

Next Fast Forward

Statistics
Hit Rate: 0%
Miss Rate: 100%

List of Previous Instructions:
• Load 4 [Miss]
• Load 3 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

100	101	0
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	1	000	BLOCK 3 WORD 0 - 0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

Memory Block

B.3.W.0
B.4.W.0
B.5.W.0
B.6.W.0
B.7.W.0
B.8.W.0

MISS

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8
Memory Size (power of 2): 64
Offset Bits: 0

Reset Submit

Instruction Load: 25 (in hex)#
8,16,35
Gen. Random Submit

Information
Valid bit is 1, therefore we should look into the tag. Requested Tag and cached tag is the same. Therefore, CACHE HIT

Next Fast Forward

Statistics
Hit Rate: 0%
Miss Rate: 100%

List of Previous Instructions:
• Load 4 [Miss]
• Load 3 [Miss]
• Load 25 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

100	101	0
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001	BLOCK 8 WORD 0 - 0	0
1	1	011	BLOCK 19 WORD 0 - 0	0
2	0	-	0	0
3	1	000	BLOCK 3 WORD 0 - 0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	0	-	0	0
6	1	000	BLOCK 25 WORD 0 - 0	0
7	0	-	0	0

Memory Block

B.6.W.0
B.7.W.0
B.8.W.0
B.9.W.0
B.A.W.0
B.B.W.0

HIT

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8

Memory Size (power of 2): 64

Offset Bits: 0

Reset Submit

Instruction

Load (in hex) 8

16,35

Gen. Random Submit

Information

Valid bit is 1, therefore we should look into the tag. Requested Tag and cached tag is the same. Therefore, CACHE HIT

Next Fast Forward

Statistics

Hit Rate : 14%

Miss Rate : 86%

List of Previous Instructions :

- Load 4 [Miss]
- Load 3 [Miss]

DIRECT MAPPED CACHE

Instruction Breakdown

001	000	0
3 bit	3 bit	0 bit

Memory Block

B. 25 W. 0
B. 26 W. 0
B. 27 W. 0
B. 28 W. 0
B. 29 W. 0
B. 30 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	011	BLOCK 8 WORD 0 - 0	0
1	0	-	BLOCK 19 WORD 0 - 0	0
2	0	-	0	0
3	1	000	BLOCK 3 WORD 0 - 0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	1	100	BLOCK 25 WORD 0 - 0	0
6	1	000	BLOCK 6 WORD 0 - 0	0
7	0	-	0	0

compare

HIT

2 Way Set Associative

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8

Memory Size (power of 2): 64

Offset Bits: 0

Reset Submit

Instruction

Load (in hex) 4

3,25,8,6,25,8

Gen. Random Submit

Information

OR gate is updated from cache blocks result. Both of the AND gate is MISS, therefore CACHE MISS

Next Fast Forward

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 4 [Miss]
- Load 2 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0001	00	0
4 bit	2 bit	0 bit

Memory Block

B. 6 W. 0
B. 1 W. 0
B. 2 W. 0
B. 3 W. 0
B. 4 W. 0
B. 5 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

MISS

MISS

MISS

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8

Memory Size (power of 2): 64

Offset Bits: 0

Reset Submit

Instruction

Load (in hex) 25

8,6,25,8

Gen. Random Submit

Information

OR gate is updated from cache blocks result. Both of the AND gate is MISS, therefore CACHE MISS

Next Fast Forward

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 4 [Miss]
- Load 2 [Miss]

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

1001	01	0
4 bit	2 bit	0 bit

Memory Block

B. 3 W. 0
B. 4 W. 0
B. 5 W. 0
B. 6 W. 0
B. 7 W. 0
B. 8 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 4 W. 0 - 0	0
1	0	-	0	0
2	0	-	0	0
3	1	0	B. 3 W. 0 - 0	0

MISS

MISS

MISS

ParaCache

Replacement Policies: ☒ FIFO ☐ LRU ☐ Random

Write Policies: ☒ Write Back ☐ Write Through ☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8
Memory Size (power of 2): 64
Offset Bits: 0

Reset Submit

Instruction Load: 25 (in hex#)
8,45,8
Gen. Random Submit

Information
OR gate is updated from cache blocks result.
One of the AND gate is HIT, therefore CACHE HIT

Statistics
Hit Rate: 0%
Miss Rate: 100%
List of Previous Instructions:
• Load 4 (Miss)
• Load 3 (Miss)
• Load 8 (Miss)
• Load 6 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B 4 W 0 - 0	0
1	1	1	B 25 W 0 - 0	0
2	1	1	B 6 W 0 - 0	0
3	1	0	B 3 W 0 - 0	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 8 WORD 0 - 0	0
1	1	2	0	0
2	0	-	0	0
3	0	-	0	0

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 8 WORD 0 - 0	0
1	1	2	0	0
2	0	-	0	0
3	0	-	0	0

com. pare

HIT

MISS

HIT

ParaCache

Replacement Policies: ☒ FIFO ☐ LRU ☐ Random

Write Policies: ☒ Write Back ☐ Write Through ☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 8
Memory Size (power of 2): 64
Offset Bits: 0

Reset Submit

Instruction Load: 8 (in hex#)
List of next 10 Instructions
Gen. Random Submit

Information
OR gate is updated from cache blocks result.
One of the AND gate is HIT, therefore CACHE HIT

Statistics
Hit Rate: 17%
Miss Rate: 83%
List of Previous Instructions:
• Load 4 (Miss)
• Load 3 (Miss)
• Load 25 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B 4 W 0 - 0	0
1	1	9	B 25 W 0 - 0	0
2	1	1	B 6 W 0 - 0	0
3	1	0	B 3 W 0 - 0	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 8 WORD 0 - 0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 8 WORD 0 - 0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

com. pare

MISS

HIT

HIT