



PES UNIVERSITY

Department of Computer Science & Engineering

Microprocessor & Computer Architecture Lab

UE23CS251B

WEEK 3 submission

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**Department of Computer Science & Engineering
Microprocessor & Computer Architecture Lab**

UE23CS251B

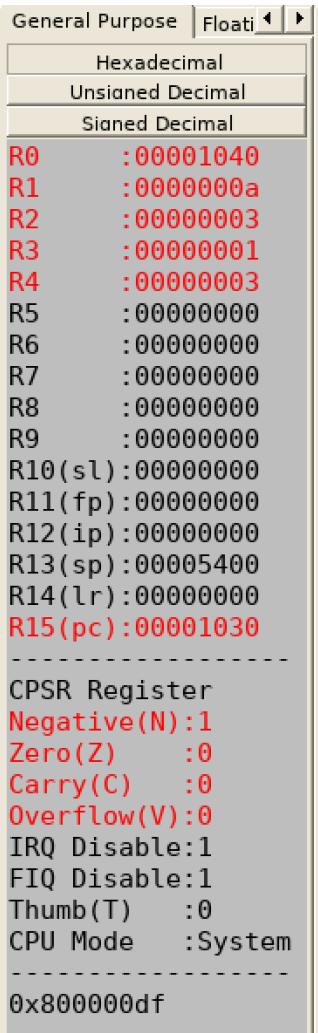
- | | |
|---|---|
| 1 | Write an ALP using ARM7TDMI to find the remainder of a number.(ie 10/3, remainder is 1)
.DATA
A: .word 10
B: .word 3 |
|---|---|

Program screen shot:

```
ARMSSim_files > asm lab3_q1.s
1   @ Write an ALP using ARM7TDMI to find the remainder of a number.(ie 10/3, remainder is 1)
2
3   .data
4       A: .word 10
5       B: .word 3
6       R: .word 0
7
8   .text
9
10  init:
11      LDR R0, =A
12      LDR R1, [R0]
13      LDR R0, =B
14      LDR R2, [R0]
15
16  start:
17      MOV R3, R1
18      MOV R4, #0
19
20  Division_Loop:
21      CMP R3, R2
22      BLT Store_Result
23      SUB R3, R3, R2
24      ADD R4, R4, #1
25
26      B Division_Loop
27
28  Store_Result:
29      STR R3, [R0]
30
31  end:
32      SWI 0x011
```

Screen shot of Register set output:

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2	<p>Write an ALP using ARM7TDMI to search for an element in an array of 16 bit each using Linear search technique</p> <p>.DATA A::hword 1,2,3,4,5,6,7,8,9</p> <p>Program screen shot:</p>

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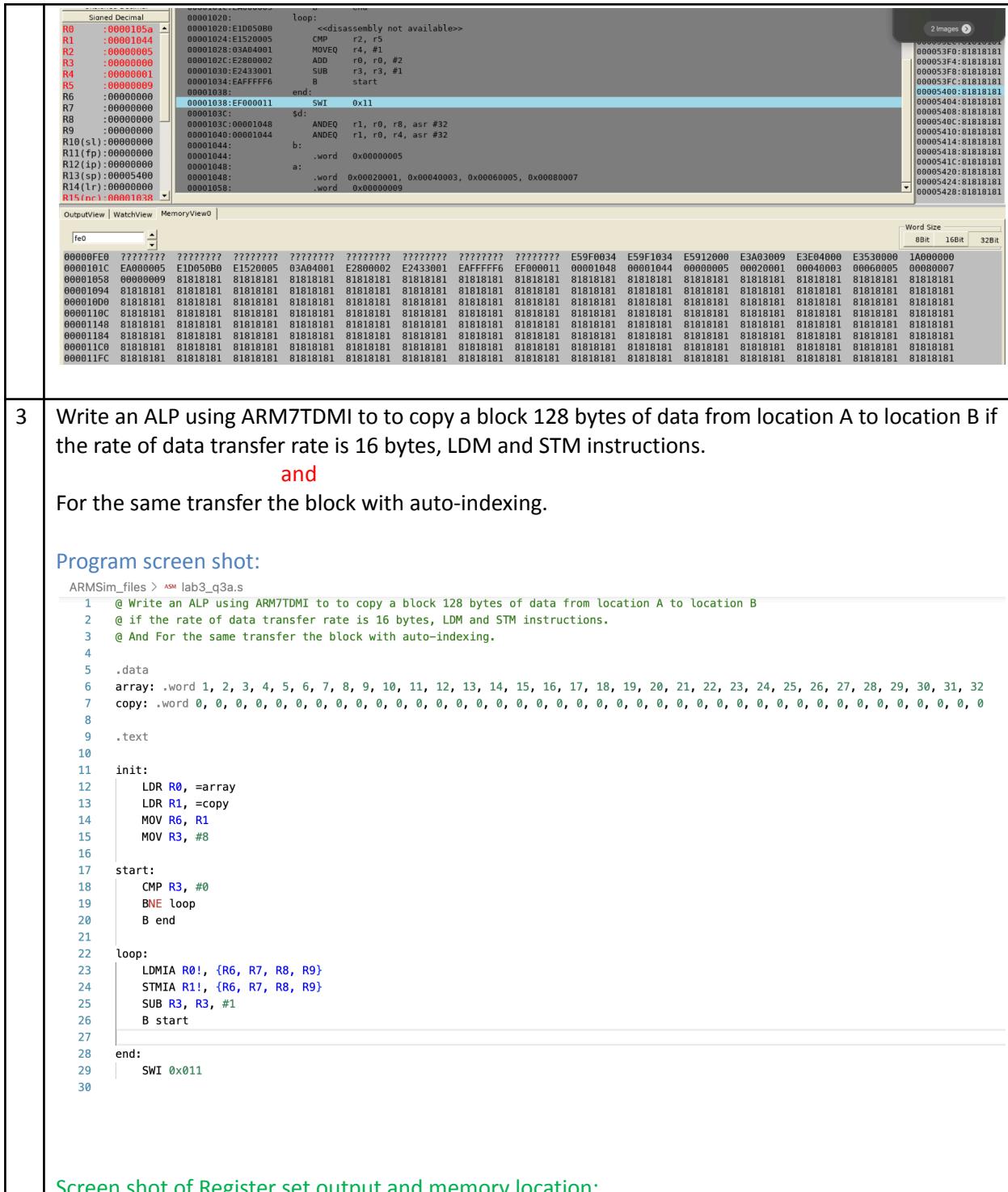
```

ARMSim_files > asm lab3_q2.s
1   @ Write an ALP using ARM7TDMI to search for an element in an array of 16 bit each using Linear search technique
2   @ Store -1 in R4 if not found, else 1
3
4   .data
5   B:.word 5
6   A:.hword 1,2,3,4,5,6,7,8,9
7
8   .text
9
10 init:
11     LDR R0, =A
12     LDR R1, =B
13     LDR R2, [R1]
14     MOV R3, #9
15     MOV R4, #-1
16
17 start:
18     CMP R3, #0
19     BNE loop
20     B end
21
22 loop:
23     LDRH R5, [R0]
24     CMP R2, R5
25     MOVEQ R4, #1
26     ADD R0, R0, #2
27     SUB R3, R3, #1
28     B start
29
30 end:
31     SWI 0x011
32

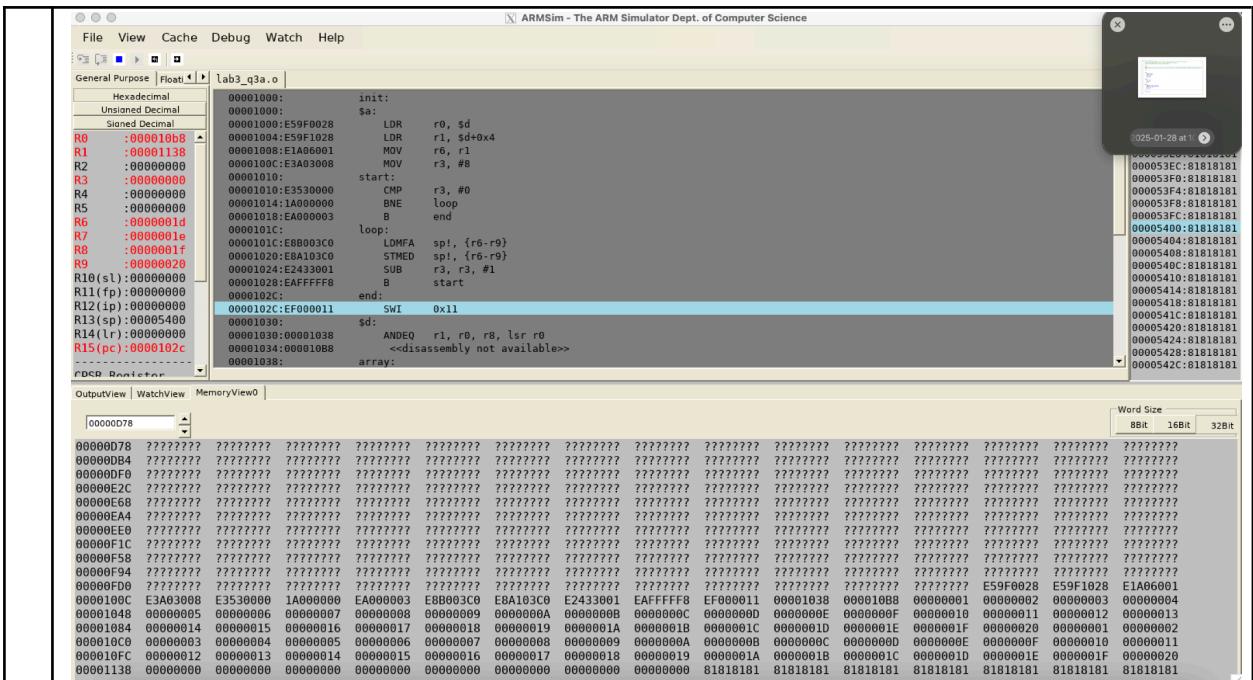
```

Screen shot of Register set output and memory location:

lab3_q2.o		
General Purpose	Floati	
Hexadecimal		init:
Unsigned Decimal		\$a:
Signed Decimal		LDR r0, \$d
R0 : 4186		00001000:E59F0034
R1 : 4164		00001004:E59F1034
R2 : 5		00001008:E5912000
R3 : 0		0000100C:E3A03009
R4 : 1		00001010:E3E04000
R5 : 9		00001014:0
R6 : 0		00001014:E3530000
R7 : 0		00001018:1A000000
R8 : 0		0000101C:EA000005
R9 : 0		00001020:0
R10(sl):0		00001024:E1D050B0
R11(fp):0		<<disassembly not available>>
R12(ip):0		00001024:E1520005
R13(sp):21504		CMP r2, r5
R14(lr):0		00001028:03A04001
R15(pc):4152		MOVEQ r4, #1
<hr/>		
CPSR Register		ADD r0, r0, #2
Negative(N):0		0000102C:E2800002
Zero(Z) :1		SUB r3, r3, #1
Carry(C) :1		B start
Overflow(V):0		00001038:0
IRQ Disable:1		end:
FIQ Disable:1		00001038:EF000011 SWI 0x11
Thumb(T) :0		<hr/>
CPU Mode :System		0000103C:\$d:
0x600000df		ANDEQ r1, r0, r8, asr #32
		00001040:00001044 ANDEQ r1, r0, r4, asr #32
		b: .word 0x00000005
		a: .word 0x00020001, 0x00040003, 0x00060005, 0x00080007
		00001048: .word 0x00000009
		00001058: .word 0x00000000

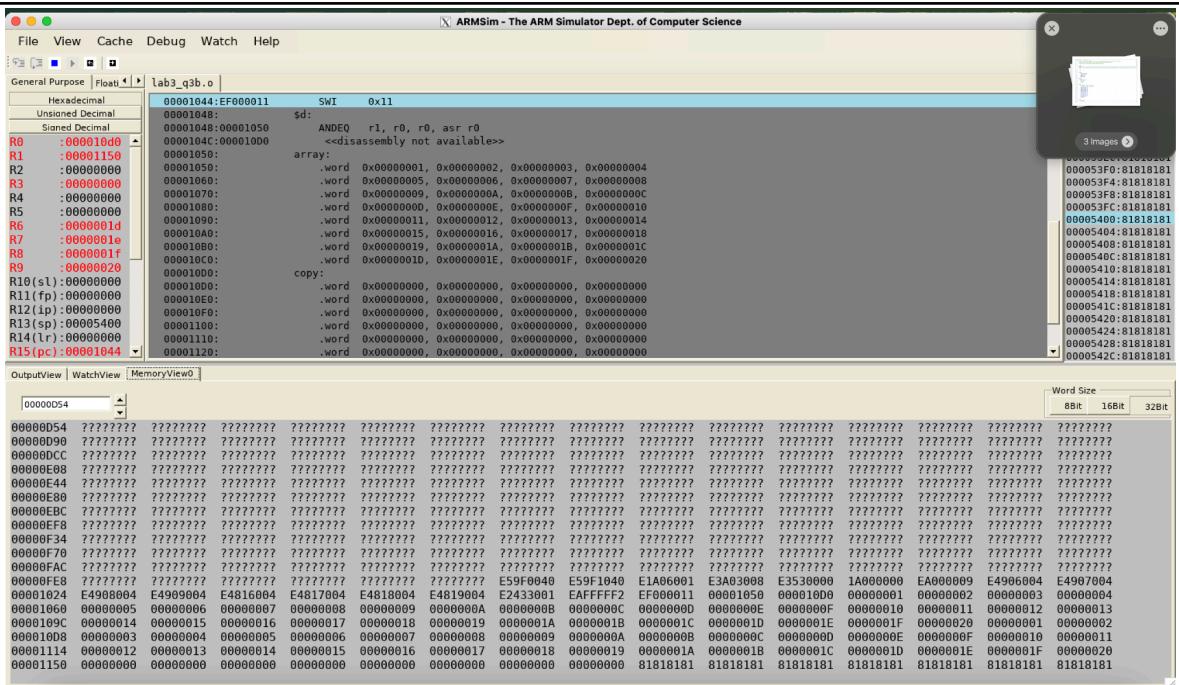


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2nd approach:

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- 4 Write an ALP using ARM7TDMI, for the given matrix arranged in row major order, find the index of an element if coordinates of a matrix is given and also find the address of the indexed element. (Using MLA instruction)

Program screen shot:

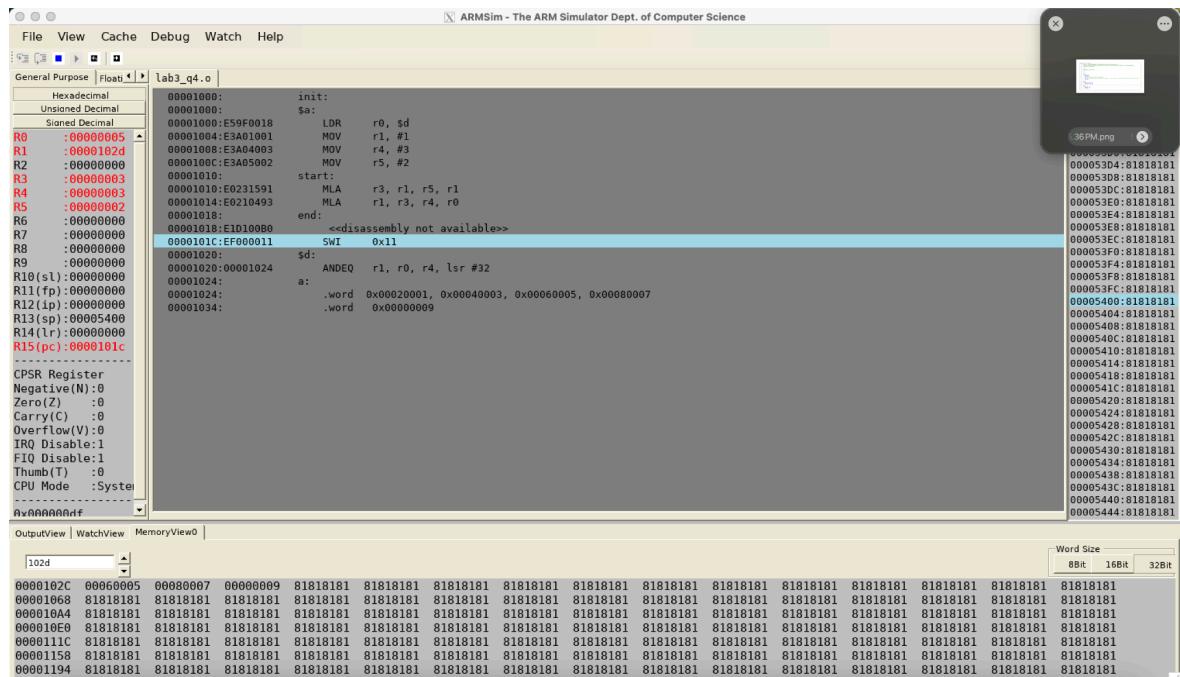
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```

ARMSim_files > asm lab3_q4.s
1 @ Write an ALP using ARM7TDMI, for the given matrix arranged in row major order,
2 @ find the index of an element if coordinates of a matrix is given and also find the address of the indexed element.
3 @ (Using MLA instruction)
4
5 .data
6 A:.hword 1,2,3,4,5,6,7,8,9
7
8 .text
9
10 init:
11     LDR R0, =A
12     MOV R1, #1
13     @ Lets assume [i,j] = [2,2] as an example
14     MOV R4, #3 @ This is set to 3 and not 2 eventhough i = 2. This is because indexing starts from 0, we hv to correct for that
15     MOV R5, #2
16
17 start:
18     MLA R3, R1, R5, R1
19     MLA R1, R3, R4, R0
20
21 end:
22     LDRH R0, [R1]
23     SWI 0x011
24

```

Screen shot of Register set output and memory location:



Assignments Questions

- 5 a)Write an ALP using ARM7TDMI to perform Convolution using MUL instruction (Addition of multiplication of respective numbers of loc A and loc B)
 b Write an ALP using ARM7TDMI to perform Convolution using MLA instruction (Addition of multiplication of respective numbers of loc A and loc B).

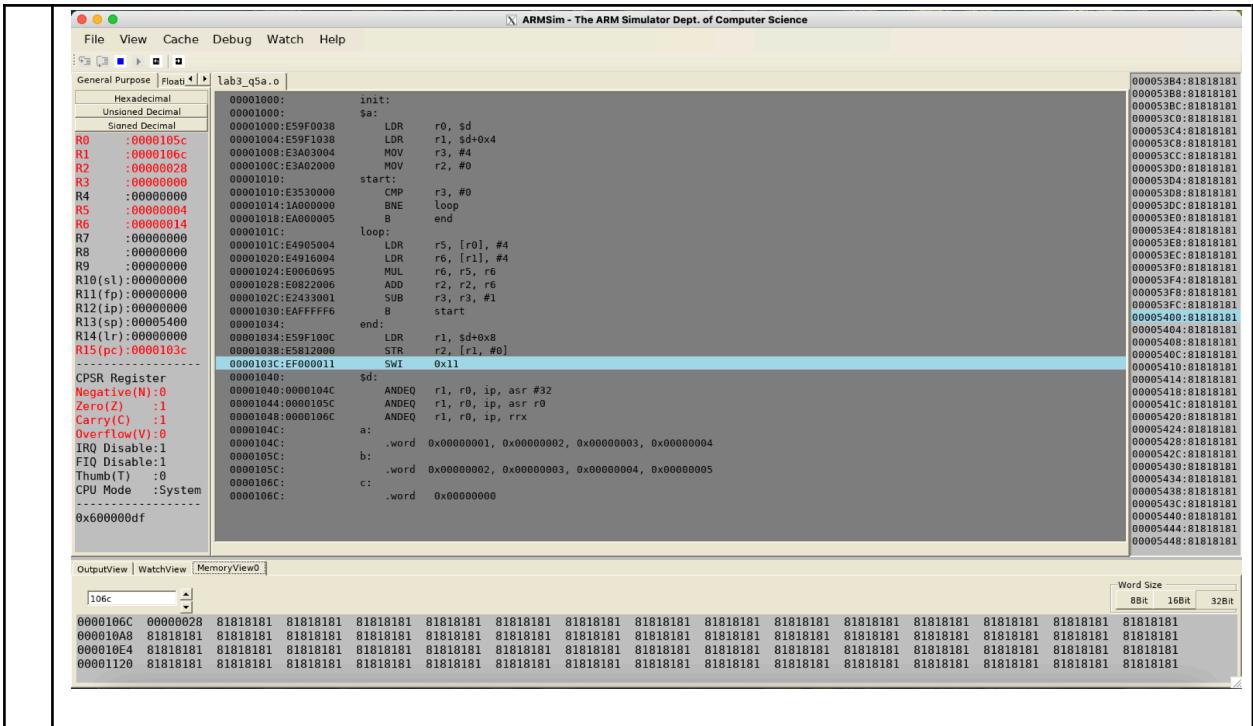
Program screen shot:

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```
ARMSSim_files > ASM lab3_q5a.s
 1  @ a )Write an ALP using ARM7TDMI  to perform Convolution using MUL  instruction
 2  @ (Addition of multiplication of respective numbers of loc A and loc B)
 3
 4  .data
 5  A:      .word 1,2,3,4
 6  B:      .word 2,3,4,5
 7  C:      .WORD 0
 8
 9  .text
10
11 init:
12   LDR R0, =A
13   LDR R1, =B
14   MOV R3, #4
15   MOV R2, #0
16
17 start:
18   CMP R3, #0
19   BNE loop
20   B end
21
22 loop:
23   LDR R5,[R0],#4
24   LDR R6,[R1],#4
25   MUL R6,R5,R6
26   ADD R2,R2,R6
27   SUB R3,R3,#1
28   B start
29
30 end:
31   LDR R1,=C
32   STR R2,[R1]
33   SWI 0x011
34
```

Screen shot of Register set output:

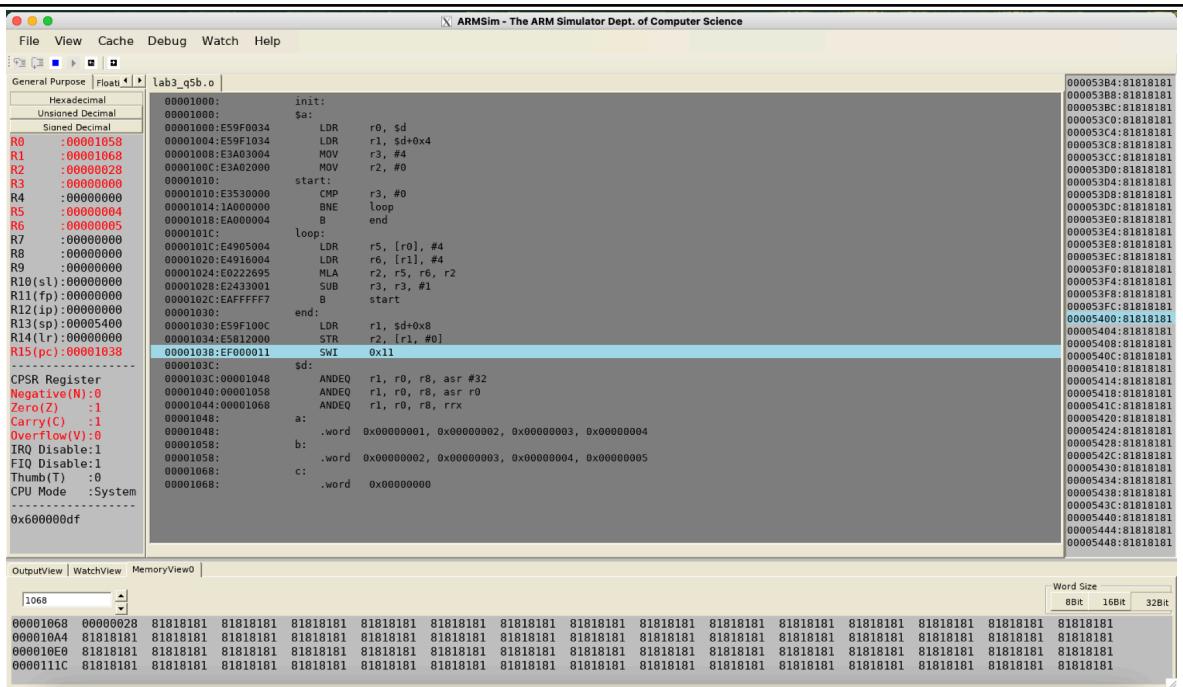
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```
ARMSim_files > ASM lab3_q5b.s
3
4     .data
5     A:      .word 1,2,3,4
6     B:      .word 2,3,4,5
7     C:      .WORD 0
8
9     .text
10
11    init:
12        LDR R0, =A
13        LDR R1, =B
14        MOV R3, #4
15        MOV R2, #0
16
17    start:
18        CMP R3, #0
19        BNE loop
20        B end
21
22    loop:
23        LDR R5, [R0],#4
24        LDR R6, [R1],#4
25        MLA R2,R5,R6,R2
26        SUB R3,R3,#1
27        B start
28
29    end:
30        LDR R1,=C
31        STR R2, [R1]
32        SWI 0x011
33
```

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	 <pre> File View Cache Debug Watch Help General Purpose Float[4] lab3_q5b.o Hexadecimal Unsigned Decimal Signed Decimal 00001000: init: 00001000: \$a: 00001000: LDR r0, \$d 00001000: LDR r1, \$d+0x4 00001000: MOV r3, #4 00001000: MOV r2, #0 00001010: start: 00001010: CMP r3, #0 00001010: BNE loop 00001014: SUB r3, r3, #1 00001018: B start 0000101C: loop: 0000101C: LDR r5, [r0], #4 00001020: LDR r6, [r1], #4 00001024: MLA r2, r5, r6, r2 00001028: SUB r3, r3, #1 0000102C: B start 00001030: end: 00001030: STR r1, \$d+0x8 00001034: STR r2, [r1], #0 00001038: SWI 0x11 0000103C: \$d: 0000103C: ANDNE r1, r0, r8, asr #32 00001040: ANDNE r1, r0, r8, asr r0 00001044: ANDNE r1, r0, r8, rrx 00001048: a: 00001048: .word 0x00000001, 0x00000002, 0x00000003, 0x00000004 00001058: b: 00001058: .word 0x00000002, 0x00000003, 0x00000004, 0x00000005 00001068: c: 00001068: .word 0x00000000 CPSR Register Negative(N):0 Zero(Z):1 Carry(C):1 Overflow(V):0 IRQ Disable:1 FIQ Disable:1 Thumb(T):0 CPU Mode :System 0x600000df -----</pre> <p>OutputView WatchView MemoryView0 </p> <p>Word Size: 8Bit 16Bit 32Bit</p> <table border="1" style="margin-top: 10px; width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">1068</td> <td style="width: 90%; text-align: right;"> 00001068 00000028 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 000010A4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 000010E0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 0000111C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 </td> </tr> </table>	1068	00001068 00000028 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 000010A4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 000010E0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 0000111C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
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6	<p>Write an ALP using ARM7TDMI to find the sum of all the BCD digits of a given 32 bit number. (hint:788 =7+8+8)</p> <p>Program screen shot:</p> <pre> ARMSim_files > ASM lab3_q6.s 1 @ Write an ALP using ARM7TDMI to find the sum of all the BCD digits of a given 32 bit number. 2 @ (hint:788 =7+8+8) 3 4 .data 5 num: .word 0x00000788 6 sum: .word 0 7 8 .text 9 10 init: 11 LDR R0, =num 12 LDR R1, [R0] 13 MOV R2, #0 14 MOV R3, #4 15 16 start: 17 CMP R3, #0 18 BEQ end 19 20 loop: 21 AND R4, R1, #0xF 22 ADD R2, R2, R4 23 MOV R1, R1, LSR #4 24 SUB R3, R3, #1 25 B start 26 27 end: 28 LDR R0, =sum 29 STR R2, [R0] 30 SWI 0x011 31 </pre>		

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The screenshot shows the ARMSIM interface with the following details:

- File View Cache Debug Watch Help**
- General Purpose**: Shows registers R0-R15 with values: R0: -4164, R1: 0, R2: 23, R3: 0, R4: 0, R5: 0, R6: 0, R7: 0, R8: 0, R9: 0, R10(sl): 0, R11(fp): 0, R12(ip): 0, R13(sp): 21504, R14(lr): 0, R15(pc): 4148.
- CPSR Register**: Negative(N): 0, Zero(Z): 1, Carry(C): 1, Overflow(V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb(T): 0, CPU Mode : System.
- Hexadecimal Unsigned Decimal Signed Decimal**: Registers R0-R15 are displayed in both hex and decimal formats.
- Assembly Code (lab3_q6.o):**

```

00001000:    init:
00001000:        sa:
00001000:        LDR r0, sd
00001004:        LDR r1, [r0, #0]
00001008:        MOV r2, #0
0000100C:        MOV r3, #4
00001010:        start:
00001010:        CMP r3, #0
00001010:        BEQ end
00001018:        loop:
00001018:        E201400F: AND r4, r1, #15
0000101C:        E0822004: ADD r2, r2, r4
00001020:        E1A01221: MOV r1, r1, lsr #4
00001024:        E2433001: SUB r3, r3, #1
00001028:        EAFFFFF8: B start
0000102C:        end:
0000102C:        E59F0008: LDR r0, sd+0x4
00001030:        E5802000: STR r2, [r0, #0]
00001034:        EF000011: SWI 0x11

00001038:        sd:
00001038:        E00001040: ANDEQ r1, r0, r0, asr #32
0000103C:        E00001044: ANDEQ r1, r0, r4, asr #32
00001040:        num:
00001040:        .word 0x00000788
00001044:        sum:
00001044:        .word 0x00000000

```
- Memory Dump:** A list of memory addresses from 000053B4 to 0005448, each followed by the value :81818181.