Replacement Policies

FIFO LRU Random

Write Policies

Write Back Write Through

Write On Allocate Write Around

Cache Size (power of 2) 3

Memory Size (power of 2) 2

Offset Bits 2

Reset Submit

Instruction

Load

(in hex)#

Gen. Random Submit

Information

The cycle has been completed. Please submit another

Next Fast Forward

Statistics

Hit Rate : 29%

Miss Rate

FULLY ASSOCIATIVE CACHE

Instruction Breakdown

000000111	00
9 bit	2 bit

Memory Block

B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3
B. A W. 0	B. A W. 1	B. A W. 2	B. A W. 3
B. B W. 0	B. B W. 1	B. B W. 2	B. B W. 3
B. C W. 0	B. C W. 1	B. C W. 2	B. C W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000101101	BLOCK 2D WORD 0 - 3	0
1	1	000010110	BLOCK 16 WORD 0 - 3	0
2	1	000011001	BLOCK 19 WORD 0 - 3	0
3	1	000001000	BLOCK 8 WORD 0 - 3	0
4	1	000000011	BLOCK 3 WORD 0 - 3	0
5	1	000000111	BLOCK 7 WORD 0 - 3	0
6	1	000010000	BLOCK 10 WORD 0 - 3	0
7	1	000100011	BLOCK 23 WORD 0 - 3	0

:

71% **List of Previous**

Instructions :

- **Load 10 [Miss]**
- **Load C [Miss]**
- **Load 64 [Miss]**
- **Load 20 [Miss]**
- **Load 4C [Miss]**
- **Load 18 [Miss]**
- **Load 64 [Hit]**
- **Load 20 [Hit]**
- **Load 40 [Miss]**
- **Load 8C [Miss]**
- **Load B4**