ERROR-TOLERANT ARITHMETIC CIRCUIT DESGIN FOR ENERGY EFFICIENT COMPUTING

A project report submitted

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BACHELOR OF TECHNOLOGY

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by

CHAGANTI SRIRAM	2105A41033
NARADASU PRANAY	2105A41044
ADICHERLA RAM TEJA	2105A41055
BERE UMESH CHANDRA	2105A41058

Under the guidance of

Dr. ARUN SEKAR R

Assoc. Prof. and Assoc. Head, Department of ECE.

Department of Electronics and Communication Engineering

SR UNIVERSITY

Ananthasagar, Warangal.

SR UNIVERSITY

CERTIFICATE

This is to certify that this project entitled "**Error-Tolerant Arithmetic Circuit Design for Energy Efficient Computing**" is the Bonafide work carried out by **CH. SRIRAM, N. PRANAY, A. RAM TEJA and B. UMESH CHANDRA** as a Major project for the partial fulfillment to award the degree **BACHELOR OF TECHNOLOGY in ELECTRONICS & COMMUNICATION ENGINEERING** during the academic year 2024-2025 under our guidance and Supervision.

Dr. ARUN SEKAR R
Assoc. Prof. and Assoc. Head,
SR University,
Ananthasagar, Warangal.

Dr. K. Rajkumar
Assoc. Prof. & HOD (ECE),
SR University,
Ananthasagar, Warangal.

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ABSTRACT

Approximate adders are the special type of adders that makes minute, controlled errors on purpose to conserve energy and enhance speed. They are mainly useful in the areas like IOT, Machine learning and image processing, in this where small errors will be causing major problems. These adders will be using only less amount of power, will be taking up only less space, and will be working faster, making them perfect for the battery-powered devices that need to be much efficient.

Since they will be having simple design, these approximate adders can be process the data fastly, which is very important for the real-time applications. When it comes to the machine learning, they help speeding up training and predictions, and then when it comes to image processing they will allow the quick operations like filtering and compression without noticeable quality loss. New designs will be keeping improve their efficiency, and make them suitable for many specialized tasks. Overall approximate adders will be helping in creating future systems those are suitable for power and energy-efficient

CONTENTS

LIST OF FIGURES

CHAPTER-1

1.1 INTRODUCTION

Approximate adders are the special type of circuit which are designed to perform addition fastly by using less power and minimizing the cost. Unlike the normal adders, in which it aims for perfect precision, in which this adders will be allowing the small mistakes perfectly on purpose. This trade-off is mainly useful in the areas where the exact calculations are always not necessary. While they have simpler design, these approximate adders will be using only the less space and will be working efficiently, making them ideal for the modern technology.

In the real-world applications, perfect precision is not always necessary. For example, Image processing, signal processing and artificial intelligence(AI) will be tolerating the small errors with some noticeable effects. These approximate adders will be helping the AI systems to train and will be helping to make predictions faster, and they will be improving the speed and energy efficient of image and video processing. Since some of the minor changes of the pixel values are invisible to human eye, using approximate adders can save energy without affecting quality.

One of the major advantage of the approximate adders is their low power usage, which is very crucial for the battery powered devices like those of Internet if Things. These devices need to run efficiently for the long period of time without the draining the battery fastly. Approximate adders will be helping these to achieve by minimizing power consumption. Their smaller size allows them to processing more units to fit in limited spaces, enhancing overall performance.

These adders are mostly useful in systems where minute errors will not be causing the problems or it can be fixed by the software. For example they are very helpful in the multimedia applications like video, audio and image processing, where minute errors are noticeable. Machine learning models, which handle large amounts of data sets, will also be benefitting because thsese approximate adders will be allowing more energy efficient and faster processing. In which this one is mainly important for the mobile computing and edge computing devices that have only limited power and limited resource.

For making the best use of the approximate adders, it is mainly important to compare their performances in the distinct applications. Here some of the adders are designed for the maximum speed, while others will be focusing on the power saving factors. By analyzing the factos like speed, power-efficiency, precision, and the size of the circuit, the researchers can be choose the correct type of approximate adders for some specific tasks.

In summary, approximate adders are the important innovation in the dogotal circuits, in which they are offering the balance between energy, efficiency, speed and simplicity. They are mainly useful in the multimedia processing, AI, IOT and machine learning, where minute errors are acceptable. By studying different types of approximate adders, designers will be optimizing the performance on the various applications, making them essential for the future low-power, high-speed and power efficient computing systems

1.2 MOTIVATION AND SCOPE OF THE WORK

In modern applications such as machine learning (ML), digital signal processing (DSP), and image processing, minor calculation errors are often acceptable. These systems can function effectively even when the results are not 100% accurate, as the impact of small inaccuracies is negligible in many scenarios. In modern generation the approximate adders are becoming more popular because they are allowing the small errors in the calculations for the better energy efficiency,and will be processing faster,and the size of the circuit will be smaller in the size.Not like the exact adders,which will be focusing on the perfect accuracy,approximate adders might make slight compromises in accuracy to enhance overall performance.

There arey many uses of the approximate adders,the adders are mainly evaluated on the accuracy,speed,power,hardware size.When it comes to accuracy,the amount of the error introduced compared to exact adders.When it comes to speed how fast the data will be processed and the effect on the overall performance.And the other one is power consumption how much amount of the energy is saved or conserved.And the size of the hardware,the amount of the physical space is required.

The main aim is to make an high speed,and energy efficient solution for the modern applications suchas analog-to-digital-converters (ADCs).By finding the correct balance between the accuracy and efficiency,approximate adders helps to optimize power use and space while still meeting the demand's for modern technology. This makes them a compelling choice for applications where precision can be slightly compromised in favor of enhanced efficiency and compact design.

1.3 LITERATURE SURVEY

Jothin, R., M. Peer Mohamed, and C. Vasanthanayaki, This paper displays the design of the high performance, error-tolerant multipliers, and adders for 16-bit image processing applications and energy efficiency. The principal advantage includes minimized power usage, lower area utilization, and enhanced speed, making them suitable for applications requiring maximum-speed digital processing. Anyhow, here the Replace-offs involve a loss In computational accuracy due to approximation techniques and maximized complexity in maintaining a balance between efficiency and accuracy.

Priyadharshni, M., and Sundaram Kumaravel, This paper presence a low-power and area-efficient error-tolerate adder developed for image processing operations. The main gains of this design involve decline of power consumption, and evolved processing efficiency, making it well-suit to specific application required approximate computing.

M. Biasielli, C. Bolchini, L. Cassano, A. Mazzeo and A. Miele, This paper displays a fault-tolerant approach for image processing by integrating approximate computing and machine learning techniques. In changing traditional duplication-based error detection with an approximated replica, it minimizes unnecessary computations and maintains its reliability. This proceeds towards in improving energy efficiency, improves processing speed, and it optimizes fault tolerance for domain-specific applications. Moreover, it involves in design complexity and mainly suitable for the tasks that can tolerate slight errors.

E. Napoli, E. Zacharelos, A. G. M. Strollo and G. Di Meo, This paper mostly involves in approximate full adders,in which it trade accuracy for enhancement in area,power and speed.These

designs are mostly useful in error-tolerant applications line video and image processing,where precision of computation are not necessary.By checking different implementaions using advanced semiconductor technology,in this the study recogonizes optimal designs that stabilizes efficiency and error.While these adders provides some of the benefits such as reduced area,power consumption,and faster computation,they also involves in the problems like increased in design complexity and reduced generalizability.

J. Lee, H. Seo, H. Seok and Y. Kim, This paper displays a novel approximate adder design that uses and error-reduced carry prediction and continual truncation technique that enhances hardware efficiency and maintaining its computational accuracy.There are many advantages in this approach that includes minimized error rates ,improved energy efficiency when it compared to the exsisting approximate adder,and these are mostly suitable for the error-tolerant applications like machine learning and digital image processing.Anyhow,the design presents some trade-offs,like potential accuracy decline in some of the scenarios and increased complexity in case of additional logic for error reduction.

P. Balasubramanian, R. Nayar, D. L. Maskell and N. E. Mastorakis, This paper displays approximate adder design that is optimized for the hardware efficiency in maintaining a near-normal error distribution.The main advantage of this approach is its ability to minimize power usage,delay while maintaining acceptable accuracy,area and making that mostly suitable for the applications such as machine learning and image processing.Any how,the trade-offs includes potential degradation in small computational accuracy and many applications-specific problems due to approximation.

F. Seiler and N. TaheriNejad, This paper mainly displays about IMPLY-based approximate adder optimized in-memory many of the computing targeting applications such as image processing.The main advantage of this approach is,it includes improvement speed,minimized power usage,and lower hardware complexity when it is compared to conventional adders,and making it suitable for energy efficient accuracy in order to approximation and potential applications-specific problems.

1.4 PROBLEM STATEMENT

The growing need for energy-efficient computing has spurred the development and adoption of approximate adders, which intentionally trade a small degree of accuracy for significant improvements in power consumption, computational speed, and hardware size. These specialized circuits are particularly advantageous in error-tolerant applications where perfect precision is not essential, such as image processing, machine learning, and multimedia systems. By allowing minor inaccuracies in calculations, approximate adders enable faster processing and reduced energy usage, making them ideal for modern technologies that prioritize efficiency over absolute precision. Application, posing challenges in evaluating the designs, selecting the most appropriate architecture for specific uses are the base for the performance of approximate adders. This variability shows the importance of the thorough analysis and the comparison to ensure the optimal performances in the real-world scenarios. This study mainly focuses on evaluating the performance of the types of approximate adders with an emphasis on the key metrics like speed, efficiency, energy and accuracy. By studying about the performance of adders under different conditions, result aims to identify the most effective designs for specific applications. For example, in IOT and edge computing, power and space are limited, the approximate adders can offer valid solution by reducing the energy consumption, and the hardware requirements without valid compromising performance. These findings highlight the potential of approximate adders to optimize computational performance and meet the increasing demands of modern technologies, particularly in scenarios where efficiency and compact design are critical.

A strategic shift in computing is represented by the adoption of approximate adders, where the minor swap in accuracy may lead to the substantial gains in energy efficiency and the processing speed. Due to the growing demand in energy-efficient solutions, especially in the fields like machine learning, and digital signal processing, approximate adders play a crucial role in enabling sustainable ,faster and cost-effective computing system. This concludes the understanding of the capabilities and limitations, of effective integration into a wide range of applications.

1.5 ROADMAP OF CHAPTERS

This document is structured in order to provide a comprehensive understanding of the main agenda, beginning with foundational concepts and the progressing towards the advanced applications and future directions. The first chapter includes the introduction, provides the context and significance of the work, describing the motivation and scope of the research. This also includes a literature survey, in which existing methodologies and identifies gaps in current research are discussed. This chapter ends with a clean and clear problem statement, by defining the specific challenges the research focuses on.

The Existing Methodology and second chapter tells about the new designs and present approaches similar to the fields. They point out the methodologies present now and showcasing and spotting their strengths and limits.

By observing these existing methodologies and strengths it serves as a strong foundation by which it helps us in more improvement and also helps us to innovate new things. Next comes the Third Chapter the Proposed Methodology this says about the innovations, designs, and approaches made from the existing designs from our research. This methodology focuses on the present designs it says about the Proposed Approximate Circuit Design by explaining about its design, architecture, its uses, principles and also innovations and designs made from the existing Solution.

The fourth chapter, Results tells about the outputs, outcomes conclusions from the research it tells about the outcomes,gerformance and effectiveness of the design from the proposed methodologies. It tells about the detailed content of the design by comparing with the existing methods in terms of their performance, design and tells about the improvements made in view of its accuracy, efficiency, thought process.

Here finally comes the fifth chapter Future Scope and Conclusion, this tells about the overall outcome of the project about the final results and outputs. This tells about the future need how the present proposed system helps in the future tells how this design can we implemented for future

needs. Finally, we end the document with Bibliography it tells about the references and sources and web contents and websites we have referred.

This document tells about the flow of the project starting from the problem statement to the conclusion of the project. It lists the problems, proposed and existing systems and finding the solution for the problem and conclusion and future scope of the project.

CHAPTER-2

EXISTING METHODOLOGY

2.1 EXISTING METHODOLOGIES AND EXISTING DESIGNS

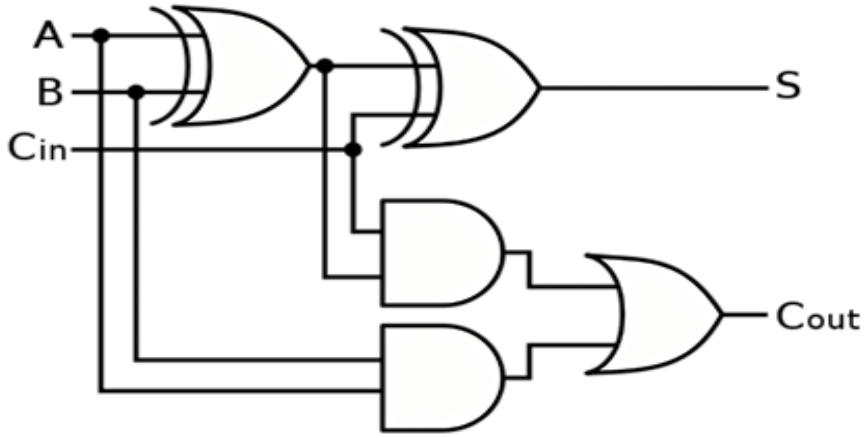


Fig_2. 1 Exact full adder

The full adder which is known as the basic digital circuit which is used to add the three binary numbers A,B,Cin(carry-in).It will be giving two results which are known as the Sum and Carry.This circuit will be making sure that the addition is correct for all the input values,which is more important for the accurate calculations in the digital system.

The working will be done with the sum calculations,the sum is found by using the two XOR gates and the first XOR gate will be taking the A and B as the inputs.And when it comes to the second XOR gate it will be taking the result from the first XOR gate and will be combining it with Cin for producing the final Sum.

And when it comes with the carry calculations the carry will be found by using the AND and OR gates.In this one AND gate will be finding the carry between the inputs A and B.The other AND gate will be finding the carry between the result of the firest XOR gate and the Cin.

Then the total number of the gates.The full adder will be needing the five logic gates and 2 XOR gates,2 AND gates and 1 OR gate.And this circuit is very important for the addition of the numbers in the digital devices like Arthemetic logic unit and the different computing systems. The expression of the out for the carry and sum are equation 1 and equation 2 expression for the Sum and Carry

The truth table of the exact full adder is shown in the figure 2.2And graphical representation for the exact full adder is shown in the figure 2.3.

$$Sum=a\hat{}b\hat{}c \quad (1)$$

$$Carry=(a\hat{}b).c+a.b \quad (2)$$

INPUT			Exact Full Adder	
a	b	c	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig_2.2 THE TRUTH TABLE OF EXACT FULL ADDER

The Output of the Exact Circuit:

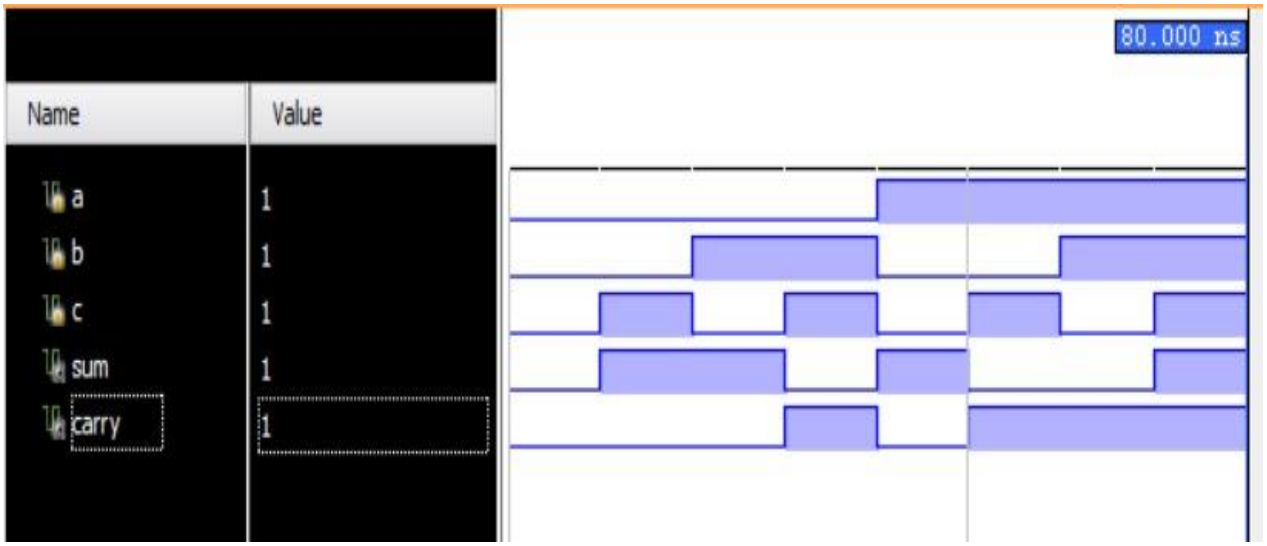


Fig_2.3: GRAPHICAL REPRESENTATION OF EXACT FULL ADDER

2.1.1 Type-1 Approximate Full Adder-1:

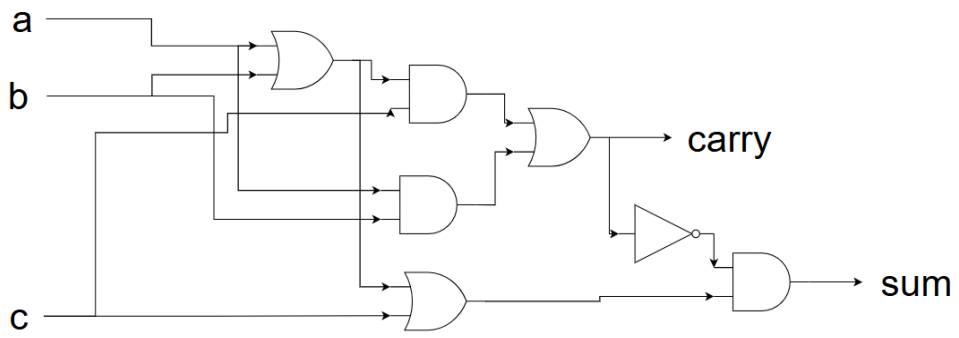


Fig_2.4 Approximate full adder-1

An approximate full adder is a digital circuit which will take three inputs such as a,b,c and will give two outputs called sum and carry. This approximate full adder is a little different from regular adder this type of circuit will allow for a small error in the sum output but the carry output is always correct.

The error in the sum output will only occur when all the three inputs are 1 that is (1,1,1). In this case, the sum output will be slightly incorrect while the carry output will remail correct in all possible cases.This small difference is known as an error distance of one. Since the carry is always correct, the circuit still gives correct results when performing multi-bit addition.

The circuit has a specific logic equation. The sum output is calculated using a formula that tales the inputs and the inverted carry bit. The carry output is calculated using another formula that uses AND and OR operation to make sure accuracy.

To perform these operations, the circuit uses AND,OR and NOT gates. Based on how the circuit is bult the exact number of gates are determined but design's mail goal is to keep the circuit simple and also allowing a controlled level of approximation in the sum. This is why the approximate full adder is useful in applications where there is slight error in the sum are acceptable,

but an accurate carry is important. This is commonly used in low-powe computing,image processing and artificial intelligence.

$$.sum = carry'.(a + b + c) \quad (3)$$

$$carry = a.b + c.(a + b) \quad (4)$$

2.1.2 Type-2 Approximate Full Adder-2:

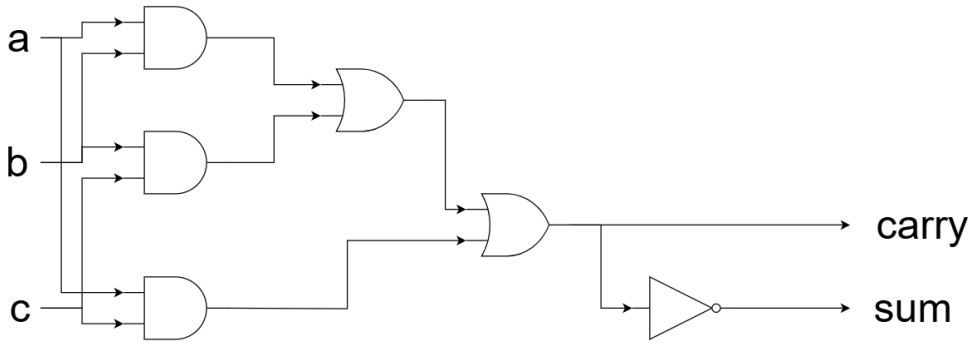


Fig_2.5 Approximate Full adder-2

An approximate adder as shown in Fig_2.5[1] is a digital circuit that has three inputs say a,b,c and will give two outputs, they are sum and carry. This circuit is designed in such a way to keep a small,controlled error in sum output and giving a carry output that is accurate in all other possible cases.The error in the sum bit happens in 2 distinct cases that is when the inputs are '000' and '111' as in Fig_2.7. In these cases, the sum output will be exactly opposite of the carry bit. This will increase computational efficiency and also maintains reasonable accuracy.

This circuit has a specific logic equation. The sum output is calculated using a formula that has a inverted carry bit to determine the result. The carry output is calculated using a separate formula using AND and OR operations to make sure accuracy.This design reduces complexity and improves efficiency. It is useful in applications where a slight errors in sum are acceptable, but a carry must be accurate.

An approximate adder, as shown in Fig_2.6[1], is a digital circuit that has three inputs say a,b,c and two outputs they are sum and carry. The circuit uses AND,OR and NOT gates to perform logical operations. Based on the specific design exact number of gates are determined but it is improved to balance simplicity and functionality. This makes the approximate adder best suited for applications where minor inaccuracies in the sum are acceptable, but the carry must be accurate, as shown in Fig_2.6[1].

$$sum = carry' \quad (5)$$

$$carry = a.b + b.c + c.a \quad (6)$$

2.1.3 Type-3 Approximate Full Adder-3:

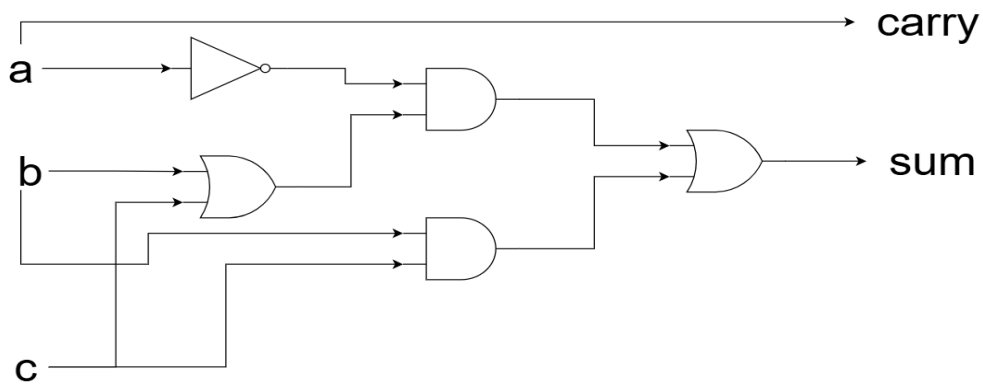


Fig_2.6 Approximate Full Adder-3

The approximate adder, as shown in Fig_2.6[1], is a digital circuit that has three inputs say a,b,c and two outputs they are sum and carry. This circuits gives errors in both the sum and carry bits, as a result incorrect values are produced in all eight possible input combinations. Specifically, the sum and carry outputs are incorrect in the input cases ‘0 1 1’ and ‘1 0 0’, as given in Fig_2.7. In these cases, the carry output same as input 'a', simplifying the computation but giving inaccuracies.

The behavior of the circuit is provided with certain logical rules. The output of sum is determined through a equation eqn 7, where "a′" is the opposite (complement) of input "a". To determine the sum bit this formula applies both AND and OR operations, however in some circumstances this may result with errors. Another formula eqn 8, is used to determine the "carry" output as well as regardless of the other inputs, it acts by simply copying the value of input "a".

An approximate adder makes use of AND, OR, and NOT gates to carry out its job . The precise number of gates based on how it's made. This type of adder is created to be easy, which makes it helpful for the tasks where tiny errors in the sum and carry bits are fine. It functions effectively in energy-saving or fast computers because it consumes less energy and functions more quickly by permitting a small mistakes. The minor mistakes are helpful to keep the circuit effective and simple, making it as a right choice for specific computing tasks.

$$sum = a'b + bc + a'c \quad (7)$$

$$carry = a \quad (8)$$

INPUT			Exact Full Adder		AFA-1		AFA-2		AFA-3	
a	b	c	Sum	Carry	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	1*	0	0	0
0	0	1	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1*	0*
1	0	0	1	0	1	0	1	0	0*	1*
1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1
1	1	1	1	1	0*	1	0*	1	1	1

Figure-2.7: TRUTH TABLE OF AFA-1, AFA-2, AFA-3

KARNAUGH MAPS OF EXSISTING CIRCUITS:

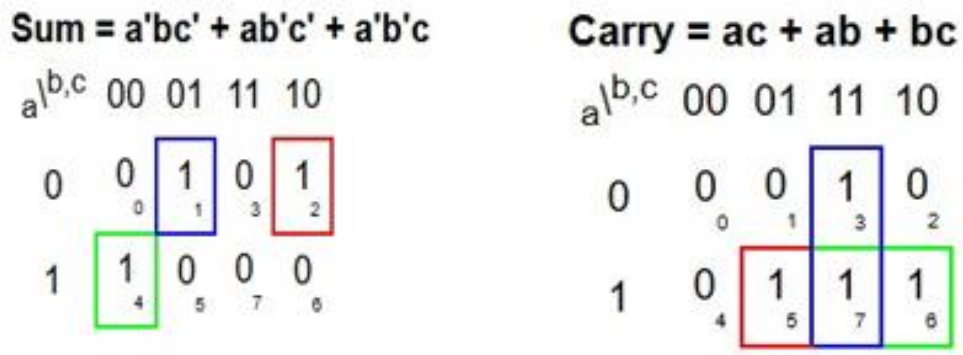


Fig_2. 8 Karnaugh Maps of AFA-1

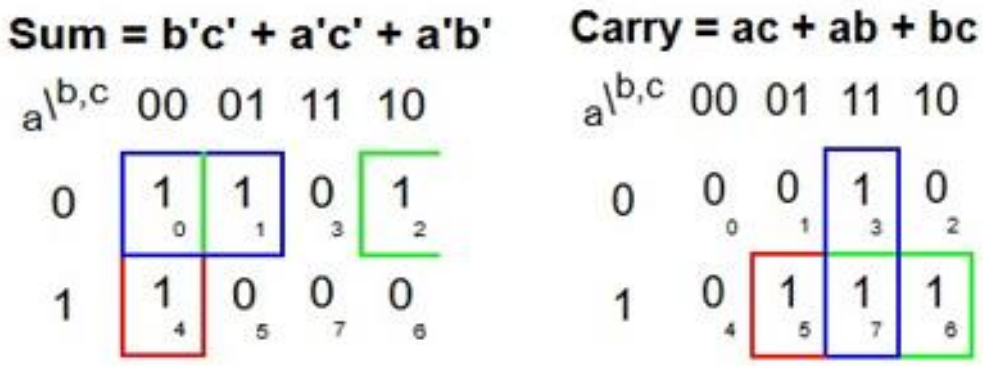


Fig_2. 9 Karnaugh Maps of AFA-2

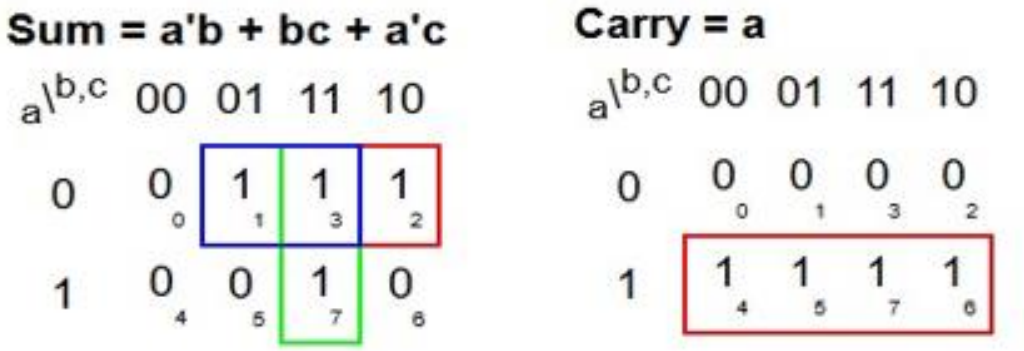


Fig_2.10 Karnaugh Map of AFA-3

Outputs of the Existing circuits

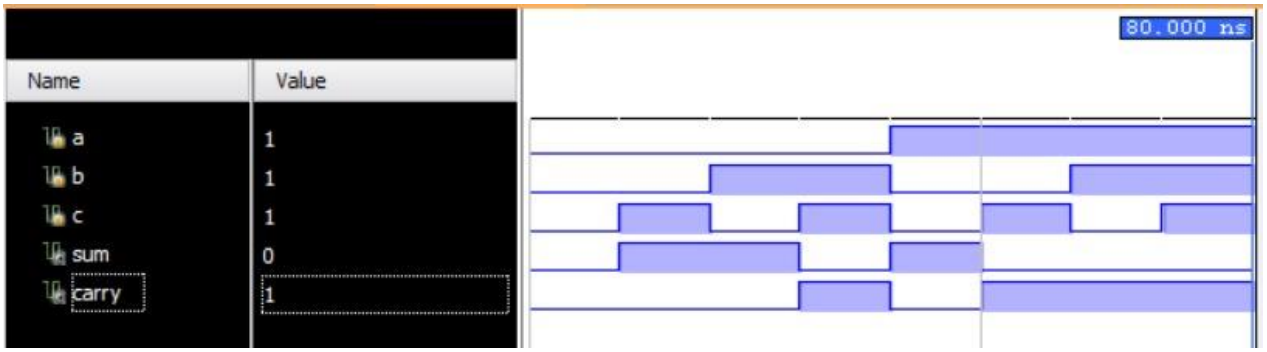


Fig_2.11 Graphical representation of AFA-1

Fig_2.12 Graphical representation of AFA-2

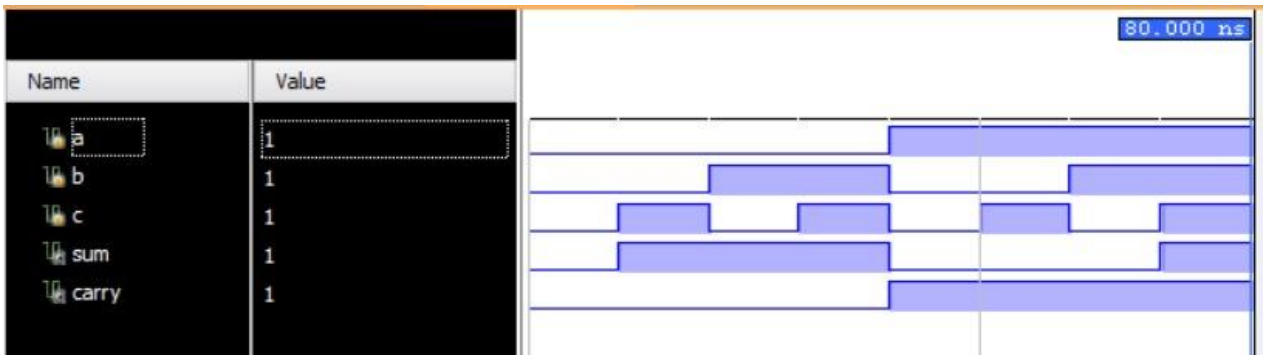


Fig_2.13 Graphical representation of AFA-3

CHAPTER-3

PROPOSED METHODOLOGY

3.1 PROPOSED APPROXIMATE CIRCUIT DESIGN

The proposed Approximate Full Adder (Fig_3.3) is an optimized version of the AFA-3(Fig_2.6) approximate adder, by modifying the Karnaugh map of AFA-3, is illustrated in Fig_3.1, designed to improve efficiency while maintaining functionality. It features three inputs (A, B, and C) and two outputs: Sum and Carry. The primary modification in this circuit involves changing the 0th bit in the sum output from '0' to '1', which simplifies the logical expression for the sum. In the original AFA-3 design, the sum was calculated using the expression "sum = a'b + bc + a'c "(eqn(7)) but in the proposed circuit, this is streamlined to "sum = a' + bc "(eqn(9)) ." This optimization reduces the complexity of the sum computation without significantly impacting the accuracy of the circuit. In the above design,the output the carry stays as same as the input of the A,the meaning is that the carry bit is the copy of A.The working of the circuit,here the output of the sum is calculated using the three types of the logic gates.The NOT gate will be inverting the input A.And the ANd gate will be multiplying the inputd B and C.And the OR gate will be combining the A and BC for getting the final Sum.

Since the carry output is just A,there will ne no need of the extra gates for it.This will be reducing the number of gates,and making the circuit simpler and will be more efficient.This design is much useful,because there will be only less gates this indicates that circuit will be consuming only less power,and will be working in any situation where small errors will be accepting like,machine learning,image processing and multimedia systems.

It will be balancing the accuracy and efficiency,and make suring that the minor error in the sum output will not be effecting the overall performance.And the circuit will be using only less energy,will be working faster,and will be taking only less space,it is great for the modern applications which will be needing more efficiency and exact accuracy.

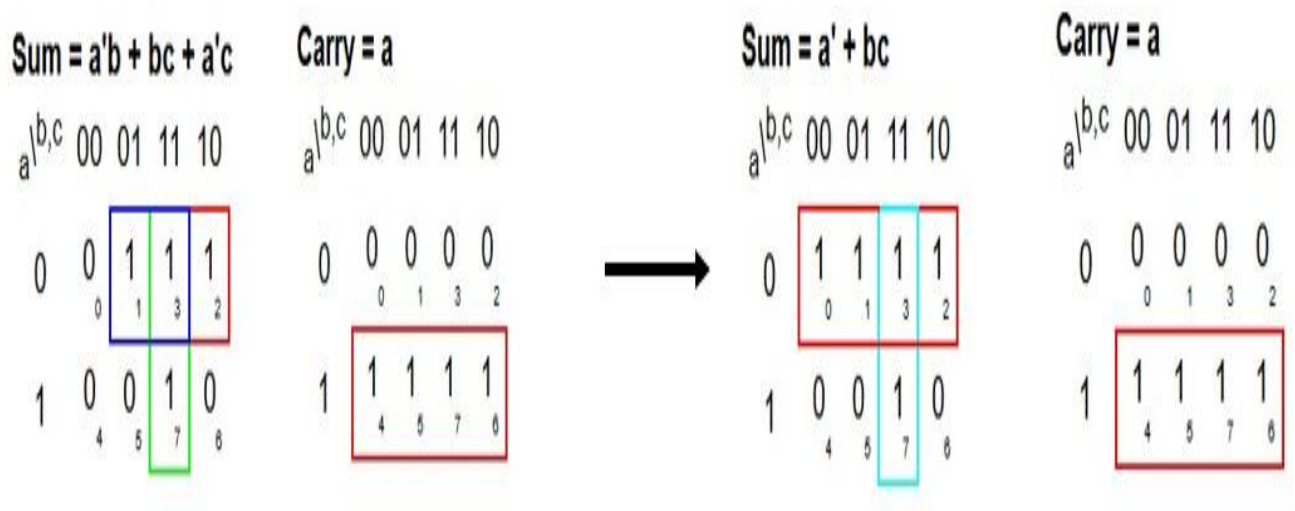


Fig_3.1 Bit Modification of AFA-3 Karnaugh Map for Proposed Karnaugh Map

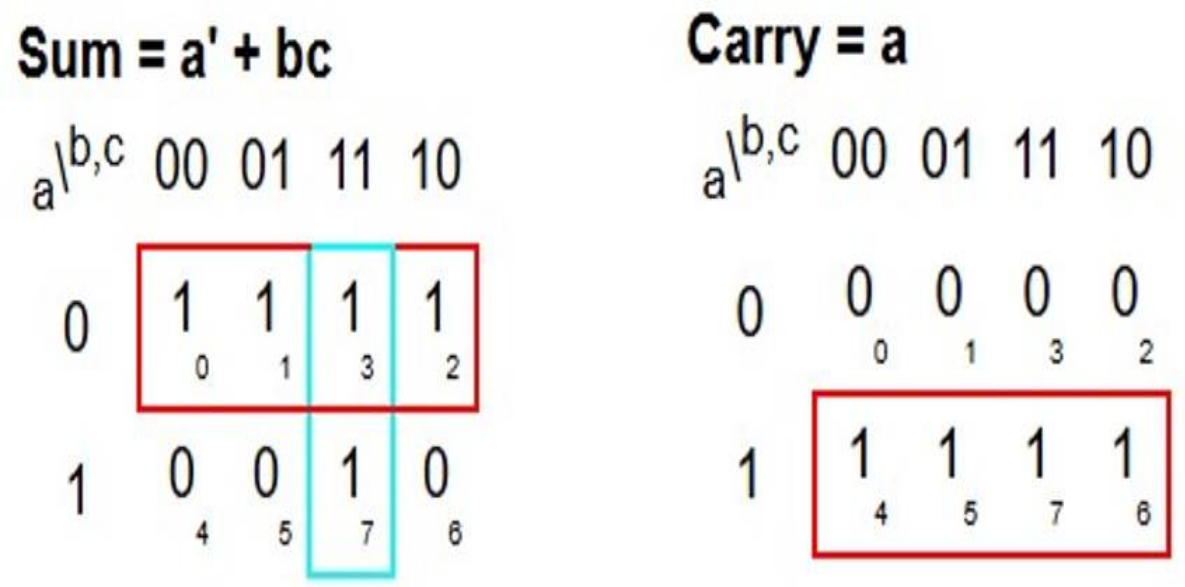


Fig_3.2 Karnaugh Map of Proposed Approximate Full Adder

Sum=a’ + bc (9)

Carry=a (10)

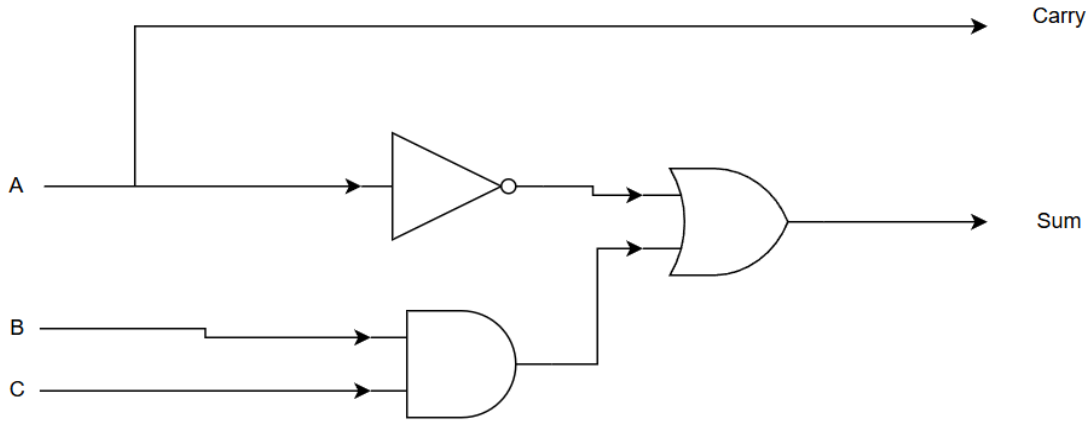


Fig_3.3 Proposed Approximate Full Adder

INPUT			Exact Full Adder		PROPOSED CIRCUIT	
a	b	c	Sum	Carry	Sum	Carry
0	0	0	0	0	1 *	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	1 *	0 *
1	0	0	1	0	0 *	1 *
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

Fig_3.4 Truth table of Proposed Approximate Full Adder

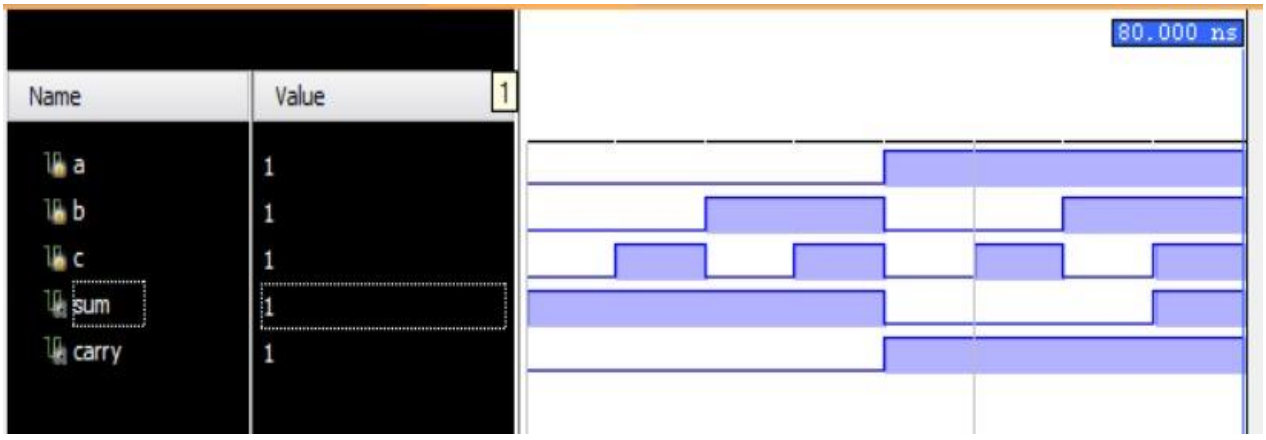


Fig_3.5 Graphical representation of Proposed Approximate Full Adder

3.1.1 AREA

cell.rep					
Instance	cells	Cell Area	Net Area	Total Area	Wireload
AFA-1	5	17	0	17	<none> (D)
AFA-2	3	12	0	12	<none> (D)
AFA-3	3	12	0	12	<none> (D)
proposed circuit	1	5	0	5	<none> (D)

Fig_3. 6 Cell area of AFA-1, AFA-2, AFA-3, and Proposed circuit

Comparing Proposed circuit with AFA-1

Now by comparing the proposed circuit with AFA-1 . The AFA-1 total cell area is 17 show in fig_3.6. But the proposed circuit's total cell area has reduced to 5.The difference in the area of the cell is due to subtracting the proposed circuit's cell area from AFA-1 which results in a reduction of 12. the reduction percentage is calculated using Reduction Percentage = (Reduction / Original Area) × 100, which results in (12 / 17) × 100 = 70. 59%. This shows that proposed circuit is approx. 70. and 59% more efficient compared to cell area of AFA-1.From this we can say that the rapid decrease of cell area highlights the achieved design ,which makes it more efficient. This simplification is for uses needing less hardware, improving speed, using less power, and making it easier to integrate into different digital systems. By this we can say the proposed circuit results in more optimized and resource useful and efficient solution.

Comparing Proposed circuit with AFA-2

The total cell area of AFA-2 is 12, which is displayed in Fig_3.6, on the other hand proposed circuit's total cell area is 5. Reduction of cell area is determined by subtracting the proposed circuit's cell area from the AFA-2 cell area, which gives the value of 7. Formula for calculating the reduced percentage = (Reduction / Original Area) x 100, which is equal to (7 / 12) x 100 = 58.33%. This will indicate that proposed circuit is approximately equal to 58. 33% more efficient than AFA-2 for area compared. The remarkable decrease in cell area spotlights the improved design efficiency, and makes the proposed circuit more compact and resource efficient. This part is more crucial for applications requiring minimized hardware resources, due to the better performance, reduced power consumption, and easier integration into various digital systems. Efficient use of cell area in

proposed circuit's makes it a more practical and effective solutions for modern electronic applications.

Comparing Proposed circuit with AFA-3

Area of the total cell of AFA-3 is 12, and in the illustrated figure of 3.6 and proposal, circuit of maintenance of a total cell area of five and reducing in result of 7. The percentage reduction is calculated as (7 / 12) × 100 = 58. 33%. And the indication of the proposal circuit is 70%. 59% more efficient than AFA-1 and 58. and it is more efficient by 33% and the both AFA-2 and AFA-3 of cell area. And the decreasing in significant of Celia have the optimisation in the new design achieved, and it makes more compact and more efficient, and it has many beneficial for applications and requiring very manual hardware resources, and it has better performance ensuring, and it consumes less power, the feasibility enhancement for the integration in various digital systems.

3.1.2 POWER

power.rep				
Instance	**cells**	**Leakage Power(nW)**	**Dynamic Power(nW)**	**Total Power(nW)**
AFA-1	5	51.334	444.023	495.357
AFA-2	3	36.689	218.993	255.682
AFA-3	3	36.689	218.419	255.107
proposed circuit	1	19.203	85.89	105.093

Fig_3.7 Power Usage of AFA-1, AFA-2, AFA-3, and Proposed circuit

Comparing the Proposed circuit with AFA-1

The total power consumption of AFA-1 is 495. 357nW, is illustrated in Fig_3.7, whereas the proposed circuit consumes only 105. 093nW. The reduction in power is calculated as 495. 357nW - 105. 093nW = 390. 264nW. The percentage reduction is determined using the formula: Reduction Percentage = (Reduction / Total Power) × 100, which results in (390. 264nW / 495. 357nW) × 100 = 78. 79%. This indicates that the proposed circuit is approximately 78. 79% more efficient in terms of power compared to AFA-1. The substantial reduction in power consumption makes the proposed circuit highly optimized for energy-efficient applications, reducing operational costs and enhancing overall performance in resource-sensitive environments.

Comparing Proposed circuit with AFA-2

Total power consumption of AFA-2 is 255. 682nW is displayed in Fig_3.7, on the order hand, proposed circuit consumes only 105. 093nW. The power reduction is 55. 682nW. 105. 093nW = 150. 589nW. Formula for percentage reduction is (reduction / Total Power) x 100, which is equal to (150. 589nW / 255. 682nW) x 100 = 58.89%. This shows that the proposed circuit is approximately equal to 58.89% more efficient in power when compared with AFA-2. The reduction in power consumption highlights the proposed circuit's improved energy efficiency, and making it much suitable for power sensitive applications. By reducing energy usage, circuit becomes more reliable and cost-effective solution, resulting best sustainability and performance among various digital systems.

Comparing Proposed circuit with AFA-3

Total power consumption of AFA-3 is 255. 107nW is displayed in Fig_3.7, on the order hand, proposed circuit consumes only 105. 093nW. The power reduction is 255. 107nW. 105. 093nW = 150. 014nW. Formula for percentage reduction is (reduction / Total Power) x 100, which is equal to (150. 014nW / 255. 107nW) x 100 = 58.80%. This shows that the proposed circuit is approximately equal to 58.80% more efficient in power when compared with AFA-3. Reduced power consumption focuses the efficiency of proposed design, making the solution more optimal for applications which require reduced energy consumption and enhanced performance. The improved power efficiency gives the lower operational costs and more sustainable approach to circuit design, making better adaptability in various technological implemetations.

3.1.3 TIME

timing.rep							
Circuits	Pin	Type	Fanout	Load(fF)	Slew(ps)	Delay(ps)	Arrival(ps)
AFA-1	g68/Y	AOI21XL	1	0	52	63	255R
	sum	AOI21XL				0	255R
AFA-2	g35/Y	INVXL	1	0	25	29	192R
	sum	out port				0	192R
AFA-3	g36/Y	OAI21XL	1	0	40	48	218F
	sum	out port				0	218F
Proposed circuit	g17/Y	OAI2BB1XL	1	0	30	88	88R
	sum	out port				0	88R

Fig_3.8 Time Consumption of AFA-1, AFA-2, AFA-3, and Proposed circuit

Comparing the Proposed circuit with AFA-1

The arrival time of AFA-1 is 255 units, as shown in Fig. 3.8, but the proposed circuit has a lower arrival time of 88 units. The difference in arrival time is calculated as. The reduction in arrival time is calculated as 255 - 88 = 167. The percentage reduction is determined using the formula: Reduction Percentage = (Reduction / Arrival Time of AFA-1) × 100, which results in (167 / 255) × 100 = 65. 49%. This significant 65.49% reduction of arrival time shows the efficiency of the proposed circuit when compared to AFA-1. By achieving a good decrease in arrival time, the circuit improves overall performance and responsiveness, making it a best choice for applications needing a faster processing speeds.The improvement in arrival time directly reduces delays in circuit operation, as a result gives better system efficiency and higher performance. This makes the proposed circuit a highly optimized solution for time-sensitive computing environments, in which speed and reliability are important.

Comparing the Proposed circuit with AFA-2

The proposed circuit performs much better than the AFA-2 circuit incase of arrival time. The arrival time of AFA-2 is 192, where as proposed circuit has an arrival time of 88. This gives in a decrease of 104 units in arrival time that is 192 - 88 = 104. Percentage reduction in arrival time: (104 / 192) × 100 = 53.16%. This shows the proposed circuit is 53.16% faster than AFA-2. This significant improvement improves responsiveness and speed of signal propagation. Hence making the circuit a better choice for applications that require low latency and high efficiency. More over

the decrease in arrival time gives better overall system performance, reducingprocessing delays, and helps the circuit to function more effectively in real-time computing environments. This improvement makes sure better computational efficiency, making the proposed circuit a highly suitable option for high-speed applications.important.

Comparing the Proposed circuit with AFA-3

The arrival time of the AFA-3 is 218,and whe it comes to the proposed circuit it is correctly having the arrival time of 88.The proposed circuit is faster than the AFA-3 when those both are compared to each other.The 59.63% reduction in arrival time showa that propsed circuit is more and more faster than the AFA-3.The improvement in the speed makes the circuitmore and more efficient.Mainly in the applications that needs quick signal transmissions and less delay.Though the proposed circuit processes the signals more quickly,hence it is better suited for the high-performance computing,reducing delay and increasing efficiency

CHAPTER-4

4.1 RESULTS

When it comes to image processing it comes under the part of the computer science and engineering that deals with the analyzing,understanding and changing the images. These images may be the photos,may be the medical scans,or satellite pictures,or the video frames.The main aim of these is to enhance the images,and to transform the images,or to extract the needed information from the images.There are few common tasks in the image processing which includes,the detection of the edges,to remove the noise,dividing the images into different sections,and the last one is to indentify the main features.

By using of artificial intelligence and machine learning,the image processing has been advanced more and more. Now the image processing is used in various sectors such as self-driving cars, in the facial recoginition, and in the medical diagnosis. The main aim of the image processing is to turn the raw amount of data that is more useful for the studying or displaying by using mathematics and different computer techniques.

And there is one more important technique when it comes to image processing is the image addition, which will be combining the two different images into a new image. This is mainly useful in enhancement of the image quality, panoramic images, or adding the textures. There are many ways to do it.

At first, it comes averaging it is simply known as adding the pixel values form the different images and will be taking the average for reducing the noise and making the image clear. And then comes weighted addition is also known as giving the distinct importance to the each image for highlighting the certains features or blending them smoothly.This is mainly used in the HDR(High dynamic Range) imaging,where the different of the similar scene with the distinct brightness levels will be combined for getting the better contrast and details.

In mathematically, the image addition will be working by adding the pixels of values from the distinct images. In the black-and-white images, this is to perform the small calculations on the brightness of the each and every pixel.When it comes to the colour images,the process will be done separately for each and every colour(Green, ,red and blue)to maintain correct colours.There are

more advanced methods like alpha blending,which will be helping to create smooth transitions by the adjustment of transparency levels.

In this study we have took two images “Bell pepper(Fig_4.1) and Cameraman(Fig_4.2) “ and done Image addition of these two images with Exact Full Adder(Fig_4.3_(a)), AFA-1(Fig_4.3_(b)), AFA-2(Fig_4.3_(c)), AFA-3(Fig_4.3_(d)), Proposed AFA(Fig_4.3_(e)). Got the result as shown in the Fig_4.3.

Fig_4.1 Bell pepper

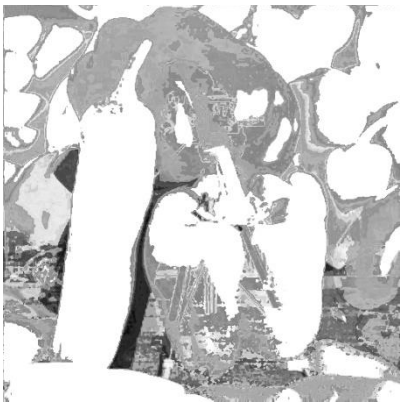
Fig_4.2 Cameraman

IMAGE ADDITION

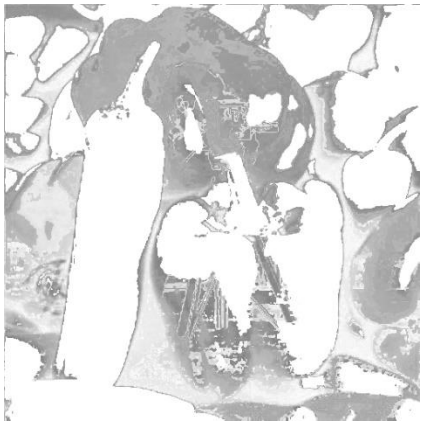
(a)

(b)

(c)



(d)



(e)

Fig_4.3 Image Addition (a) Exact Full Adder, (b) AFA-1, (c) AFA-2, (d) AFA-3, (e) Proposed AFA

MSE evaluates the average squared difference between the approximate and original values. Lesser MSE denotes higher precision or accuracy.

Formula:

MSE=$1/N \sum_{i=1}^{N} x_i - y_i$

Where, x_i denotes the original value

y_i denotes the approximated value

N denotes the total number of data points.

PSNR examines the clarity of the approximated data relative to the original. Higher PSNR values denote better clarity.

Formula:

$PSNR = 10.\ log_{10}\ (MAX_I^2/MSE)$

where MAX_I denotes the maximum possible pixel value.

SSIM estimates the perceptual similarity between the approximated and original data by seeing structure, contrast, and luminance. Values range from 0 to 1, with higher values denotes better similarity.

$$S(x,y)=F(I(x,y), C(x,y), S(x,y))$$

Circuit	MSE	PSNR (dB)	SSIM
b	12.34	33.35	0.831
c	25.36	30.44	0.554
d	36.74	29.43	0.495
e	12.79	38.92	0.791

Fig_4.4 Image parametric

MSE (Mean Squared Error in pixels²) is evaluating the average squared error between the original and Approximate values. When the value is lower it denotes better accuracy. The proposed circuit has an MSE of 12. 79, which is much lower than Fig_4.3_ (c) and Fig_4.3_(d), and only slightly higher than Fig_4.3_(b).

PSNR (Peak Signal-to-Noise Ratio in dB) is When the value is higher it denotes good image quality. The proposed circuit has the highest PSNR (38. 92 dB), it denotes that the produced results are closer to the original compared to other AFAs.

SSIM (Structural Similarity Index) is evaluates the similarity between two images, when the values is closer to 1 it indicates that a higher structural similarity. The proposed circuit gains an SSIM of 0. 791, which is better than Fig_4.3_(c) and Fig_4.3_(d), though slightly lower than Fig_4.3_(b).

The proposed circuit surpasses the existing AFAs in terms of PSNR and SSIM while supporting a relatively low MSE. This equalize suggests it offers high accuracy with minor structural deformation.

Fig_4.3_(b) has a good SSIM but lower PSNR, while Fig_4.3_(d) has the worst scores across all metrics, it denotes higher errors and more image declination.

The proposed circuit seems to impact a equalize between precision and structural fidelity, potentially it is a key candidate for operation needing both low error and high-quality output.

CHAPTER-5

FUTURE SCOPE AND CONCLUSION

5.1 FUTURE SCOPE

Approximate adders have emerged as a transformative technology with the potential to significantly reduce power consumption, minimize computational delay, and optimize hardware area while maintaining acceptable levels of precision. These benefits make them significantly capable for the wide range of operations, specially in domains where exact precision is not critical. As the necessity for lower energy consumption and high speed computing continues to grow, future study and development work should concentrate on improving the design and performance of approximate adders to further decline the replace offs between precision, delay, and power. By directing these limitations, approximate adders can open new potentialities in computing and drive creation across various fields.

One specific field concentrate is improved error correction. Designing error correction techniques that can suit the level of approximation based on the key computational necessities and error tolerance of a given application is essential. This flexibility would accept approximate adders to equalize efficiency and precision more effectively. Additionally, developing error-tolerant adder that are fundamentally robust to errors could decrease the necessity for specialized error correction methods, optimized their execution and enhancing overall reliability. These improvements would make approximate adders more adaptable and suitable to a boarder range of situations, from real-time working to large amounts of data analysis.

Next crucial domain is hardware execution and validation. Working prototyping approximate adders on Field-programmable gate array(FPGAs) and Application-specific integrated circuits(ASICs) is important to examine their real-word implementation and lower power usage. This process helps find functional limitations and opportunities for simplified. Further study into the effect of process differentiations on the accuracy and reliability of approximate adders is essential to assure their robust in various manufacturing environments. Designing methods to help these impact will improve the consistency and reliability of adders, making them more available int the markets and industrial operations.

Approximate adders also keep great promise in occurring methodologies. In the AI&ML, they can minimize the computational prices and lower power consumption. In quantum computing, integrated approximate adders into quantum circuits could enhance error tolerance and decrease fault rates, directing some of the specific limitations in this area. Neuromorphic computing, which wish to copy the low energy consumption and error tolerant nature of biological neurons, can also advantage from approximate adders by integrating them into hardware developments. Additionally, the IoT and wearable gadgets can use approximate adders to gain lower area occupancy and low-power consumption applications.

Approximate adders are utilized in many areas because they can execute calculations with lower power and less delay. In domains like Image processing, they optimize task such as improving and minimizing data. This makes the work speed without impacting the last outputs too much. In bioinformatics, they can fast up difficult works like identifying DNA sequences, supporting researchers get outputs fastly and at a low price. They are also utilize for green computing, as they decline power consumption in data centres and rechargeable battery gadgets, supporting to reliability.

Security is alternative field where approximate adders can help. They can be developed to oppose threats that try to crash into the system using errors. Cryptography system, Which saves delicate information, can advantage from these secure adders. Additionally, communication system utilizes fault tolerant adders to transfer the information more safely, even in disturbance or noisy environments.

To maintain enhancing approximate adders, enhanced tools are needed. Fundamental systems to compare various adders will support researchers to identify the better designs. ML can also guide in innovating better adders by dynamically identifying the most efficient circuits. With these tools, researchers can fast the creation of adders that are most efficient for modern techniques.

Approximate adders can also help reliable works. They can be made to manage wear and tear better, prolonging the life of electronic gadgets. This means fewer gadgets would need to be unused. deducting electronic waste. Additionally, these low-power adders can make it simpler to recycle old hardware, helping a circular economy where items are again used rather to wasted.

By Studying these operations, engineers and researchers can make the most of the approximate adders. Their capability to save power, enhance execution, and decrease waste makes them a important methodologies for the future. As technology enhances, approximate adders will play an important role in creating greener, more protected computing system and faster.

5.2 CONCLUSION

The performance analysis of approximate adders indicates that they are significantly utilized for meeting and gaining essential for fast and low-power computing. By purposely decreasing precision, they uses low power, minor delay, and take low area on the chip. This makes them ideal for works in domains like signal processing, ML, and image processing, where minor fault don't highly impact the overall outputs.

Various types of approximate adders gives specific benefits, such as low power usage, less delay, lower area occupancy. Selecting the best adder relies on the unique essentials of a work, containing how much faults allows, how many sources are present, are the desired execution goals. Each situation needs careful choosing to get the most advantages from the adders.

This research enhances the requirement of equal efficiency and output quality to increase the advantages of approximate adders. By comparing different designs and their execution in real-word operations, it shows important insights for engineers and researchers working on low-power efficient systems. They identifying also the routes for further enhancements in approximate computing, supporting its utilization in both present and future technologies

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