Computer Architecture

Pipelined implementation of MIPS architecture

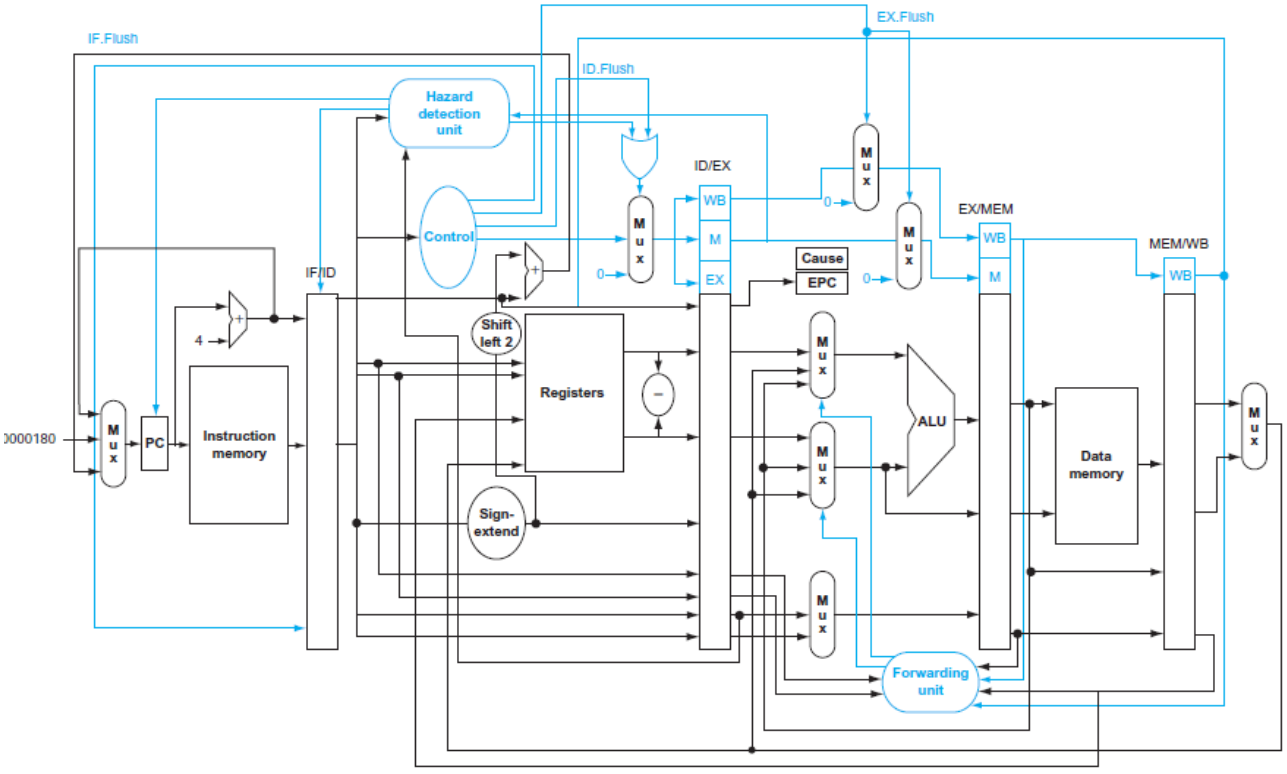
Introduction

The work done by processor is divided into the 5 main stages(pipeline stages) :

- Instruction Fetch (IF)
- Instruction Decode (ID)
- Execute (EX)
- Memory Access (MEM)
- Writeback (WB)

Development of the project was done in 2 stages mainy ,
Stage 1: Development of datapath with all pipeline register
Stage 2: Adding the Forwarding and Hazard detection unit (to add stalls whenever required)

Referred design



Forwarding unit,Hazard detection unit,control unit all are developed by referring to the textbook. Control signals are also carried at every stage through the pipeline registers. The Branch taking decision circuit is also moved to the Instruction Decode (ID) stage.

Control unit:

Instruction	Execution/address calculation stage control lines				Memory access stage control lines			Write-back stage control lines	
	RegDst	ALUOp1	ALUOp0	ALUSrc	Branch	Mem-Read	Mem-Write	Reg-Write	Memto-Reg
R-format	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	X	0	0	1	0	0	1	0	X
beq	X	0	1	0	1	0	0	0	X

Forwarding Unit:

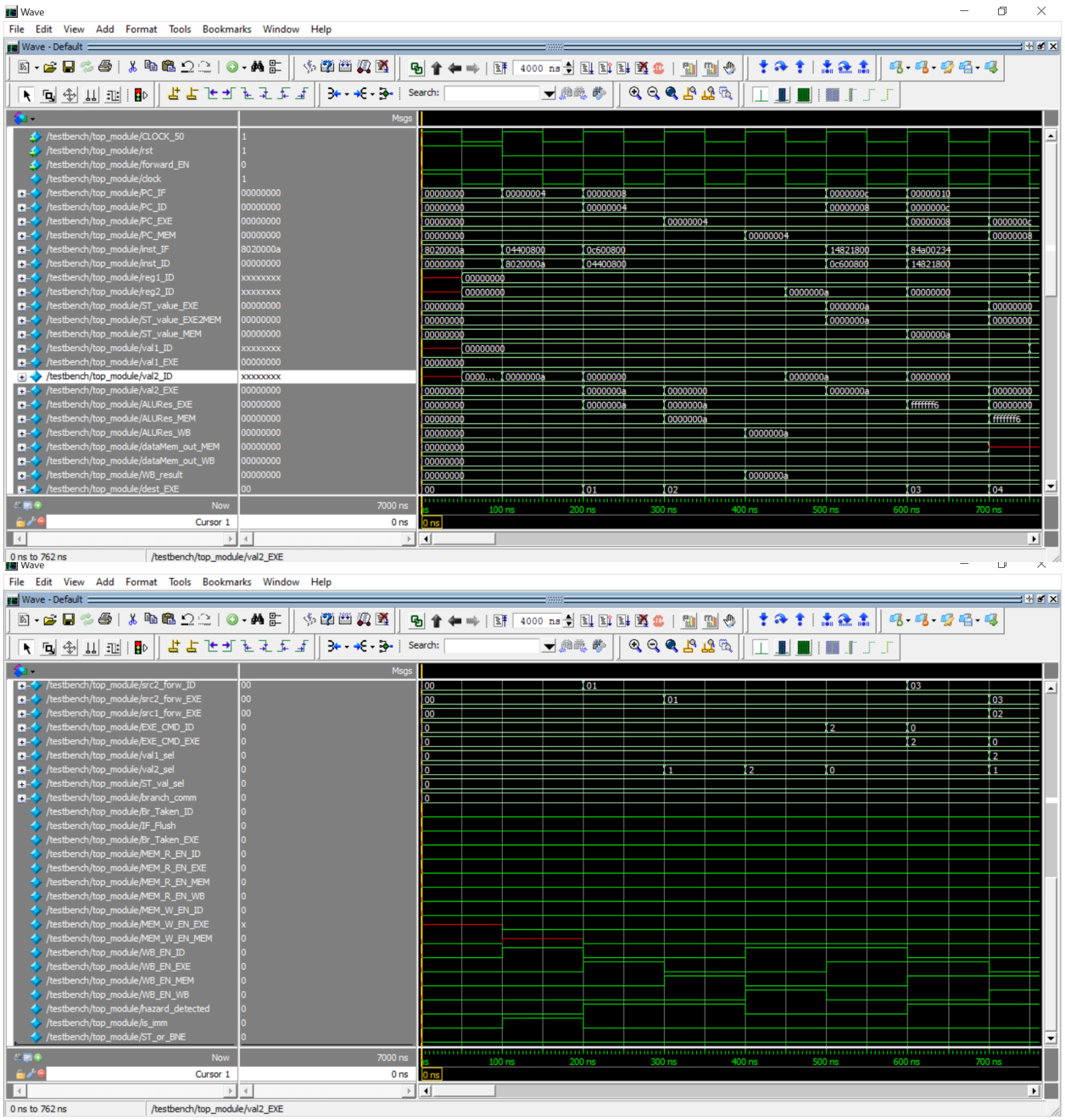
Mux control	Source	Explanation
ForwardA = 00	ID/EX	The first ALU operand comes from the register file.
ForwardA = 10	EX/MEM	The first ALU operand is forwarded from the prior ALU result.
ForwardA = 01	MEM/WB	The first ALU operand is forwarded from data memory or an earlier ALU result.
ForwardB = 00	ID/EX	The second ALU operand comes from the register file.
ForwardB = 10	EX/MEM	The second ALU operand is forwarded from the prior ALU result.
ForwardB = 01	MEM/WB	The second ALU operand is forwarded from data memory or an earlier ALU result.

Hazard detection:

Logic used is

```
if (ID/EX.MemRead and
   ((ID/EX.RegisterRt = IF/ID.RegisterRs) or
     (ID/EX.RegisterRt = IF/ID.RegisterRt)))
     stall the pipeline
```

Simulation Result



Instructions are directly written in instruction memory.
Time period for a 1 clock cycle is100ns.