IC TESTER

SUBMITTED BY GROUP 44

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CONTENTS

User Requirements & Technical Specifications

Design a Microprocessor based Tester to test the logical functioning of the following chips:

1. 7400
2. 7408
3. 7432
4. 7486
5. 747266

Technical specifications are as follows

- The IC to be tested is inserted in a 14 pin ZIF socket. The IC number is entered via a keyboard.
- The keyboard has keys 0-9, backspace, enter and test.
- The user places the IC in the ZIF socket closes it – then enters the IC No, followed by enter key.
- The IC No. is displayed on the 7-segment display.
- The testing will start once the user presses test key.
- After Test the result PASS/FAIL is displayed on the 7-segment display.

ASSUMPTIONS AND JUSTIFICATIONS

ASSUMPTIOMS

- IC that is placed in the ZIF socket should be one of the 5 chips aforementioned.
- ‘Enter’ button should be pressed before pressing the ‘Test’ button

COMPONENTS USED WITH JUSTIFICATION WHENEVER REQUIRED

- 8086 MicroProcessor (using 2-5 MHz clock)
- 74LS373 latch - 5 latches used (3 used for demultiplexing address lines and 2 used for demultiplexing data lines)
- 8255 - 3 used (One each for display, keyboard matrix , 14 pin ZIF socket)
- 74HC138 Decoder (1) used for selecting the required 8255
- **2732 ROM - 2 used - smallest ROM chip available is 4K, and as we need to have even and odd bank and ROM is required at reset address which is at $FFFF0_H$ and 00000_H - where there is the IVT**
- 6116 RAM - 2 used - Smallest RAM chip available is 2 K and we need odd and even bank. We need RAM for stack and temporary storage of data
- 7SEG-MPX6-CC - Used for displaying the result

ADDRESS MAP

- Memory Map

  ROM 00000_H - $01FFF_H$

  RAM 02000_H - $02FFF_H$

- I/O Map

  Keyboard - 8255

PortA	20_H	
Port B	22_H	
Port C	24_H	(Upper port is used for input and lower port for output)
CLRK	26_H	

  Display - 8255

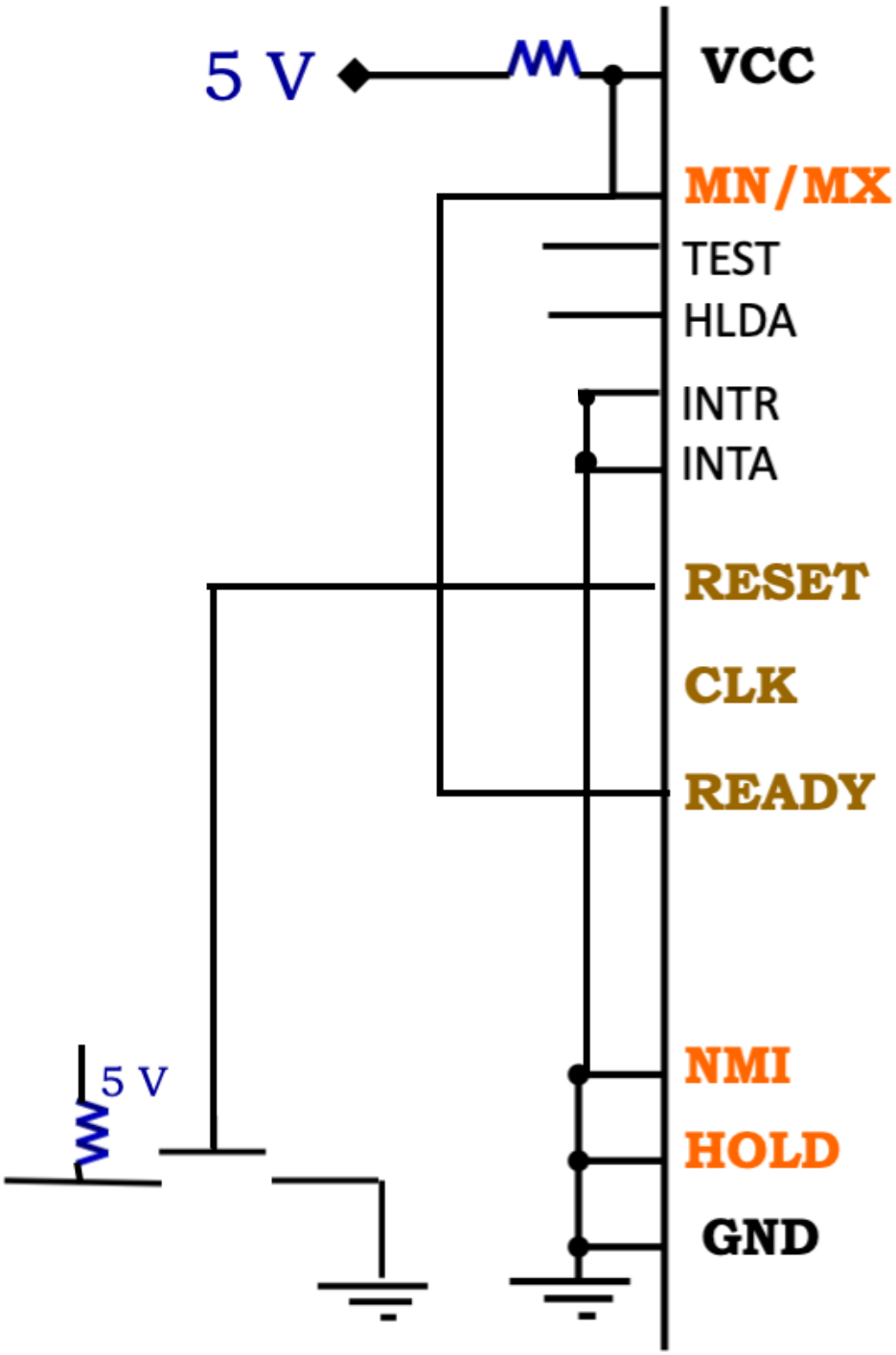
PortA	40_H	(Output)
PortB	42_H	
PortC	44_H	(Output)
CLRD	46_H	

  ZIF Socket

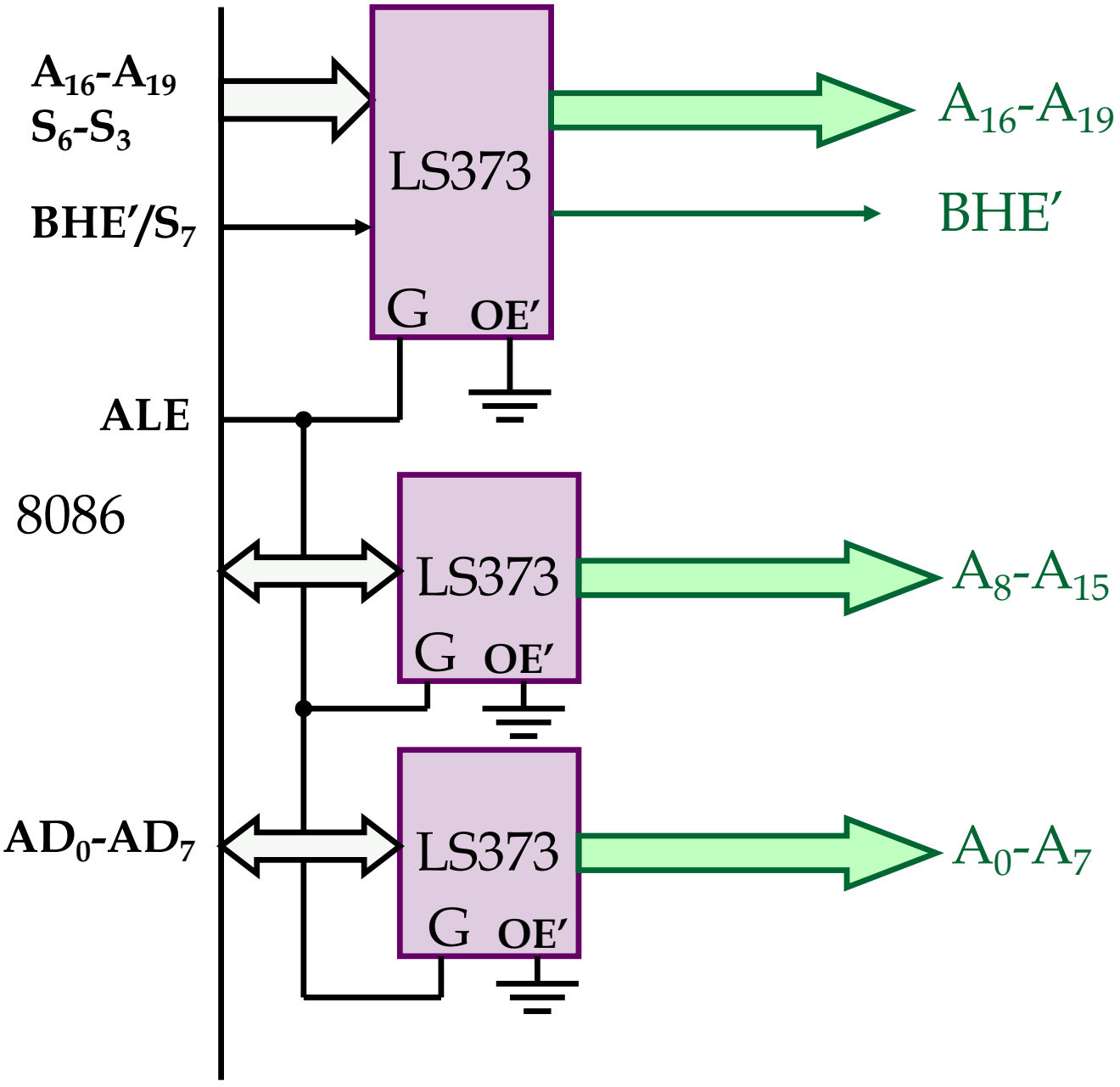
PortA	60_H	(Input)
PortB	62_H	
PortC	64_H	(Output)
CLRS	66_H	

DESIGN

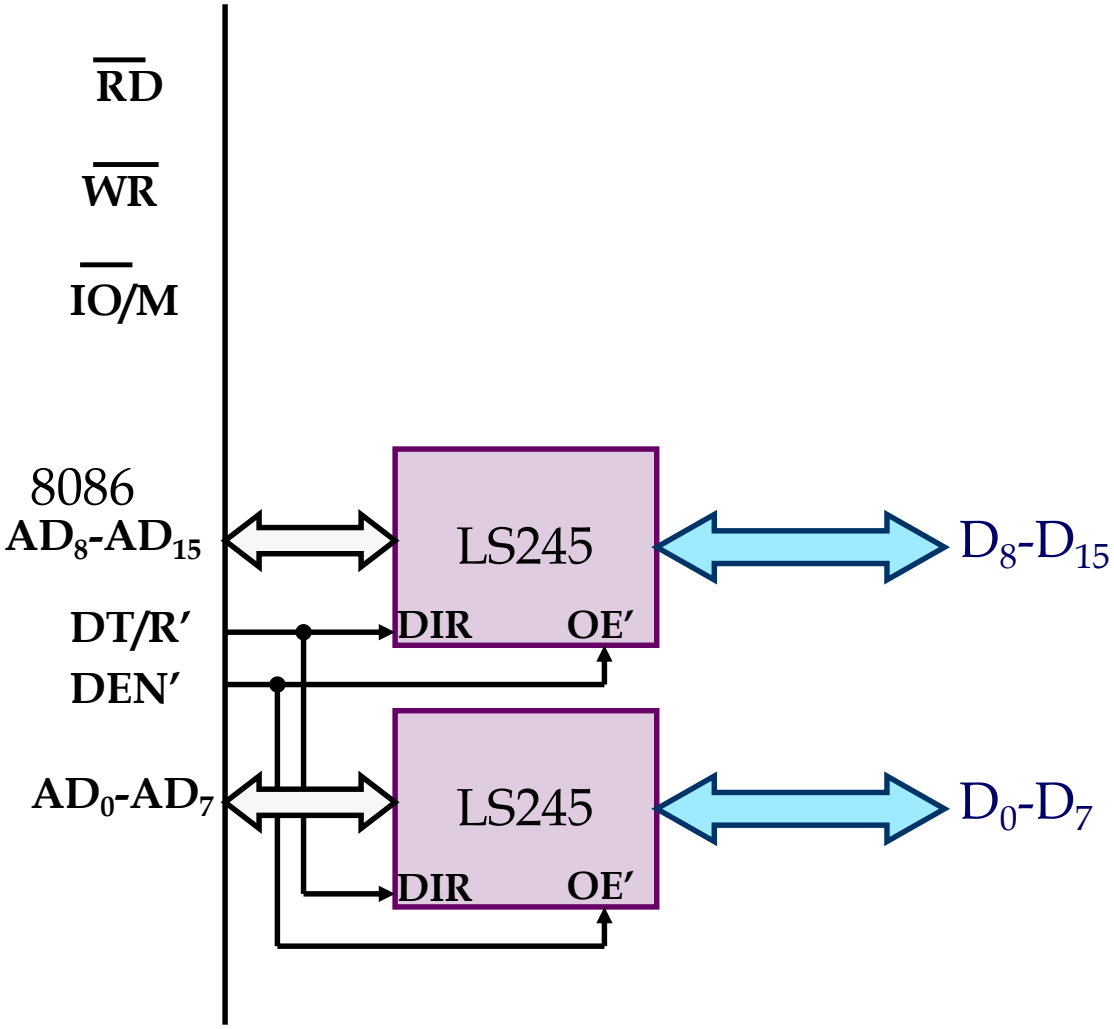
❖ 8086 INTERFACE



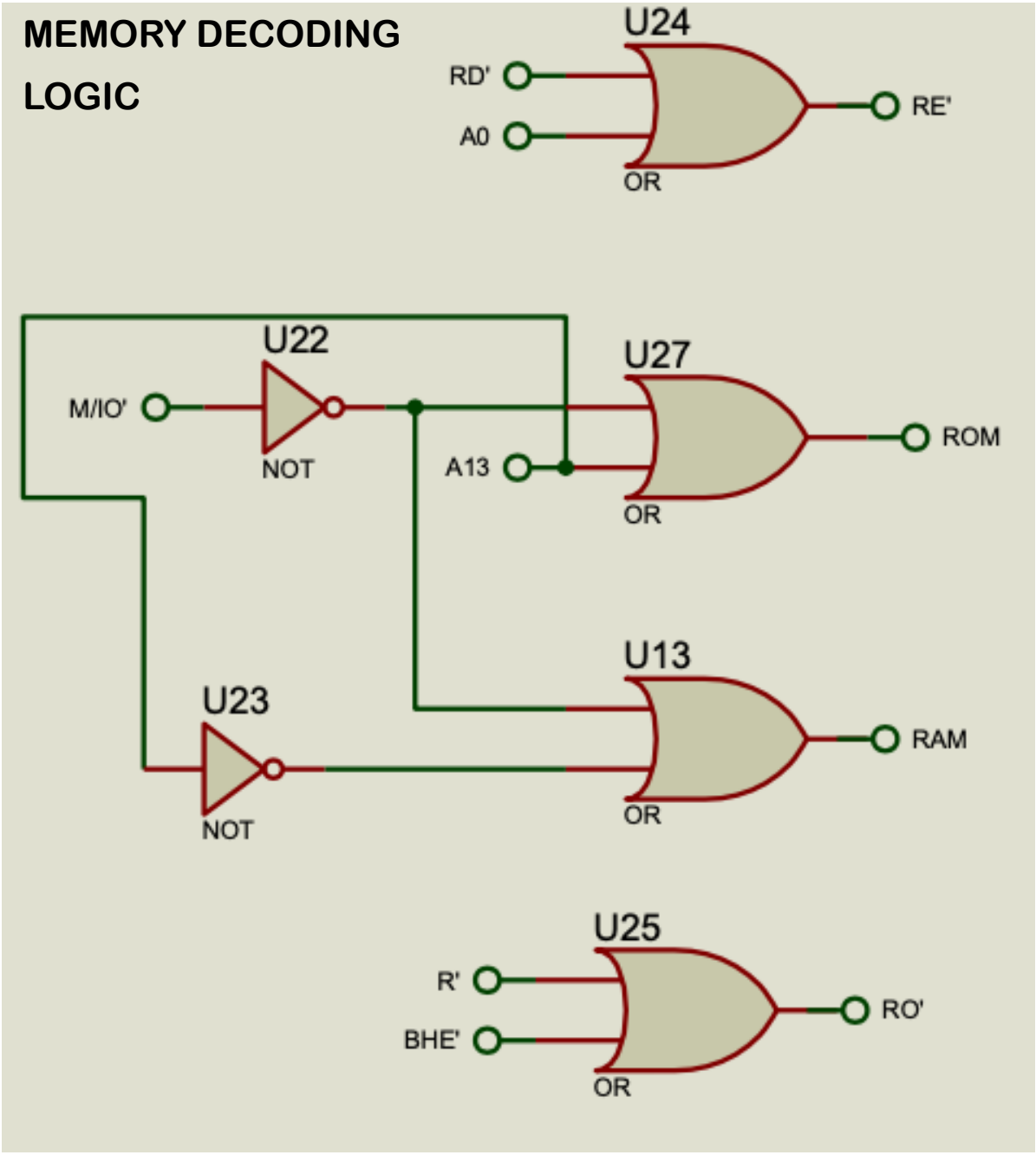
❖ SYSTEM BUS OF 8086 (ADDRESS)

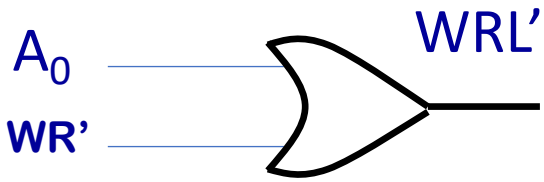


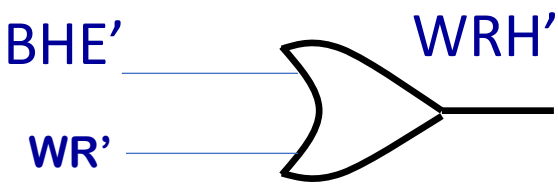
❖ SYSTEM BUS OF 8086 (DATA + CONTROL)



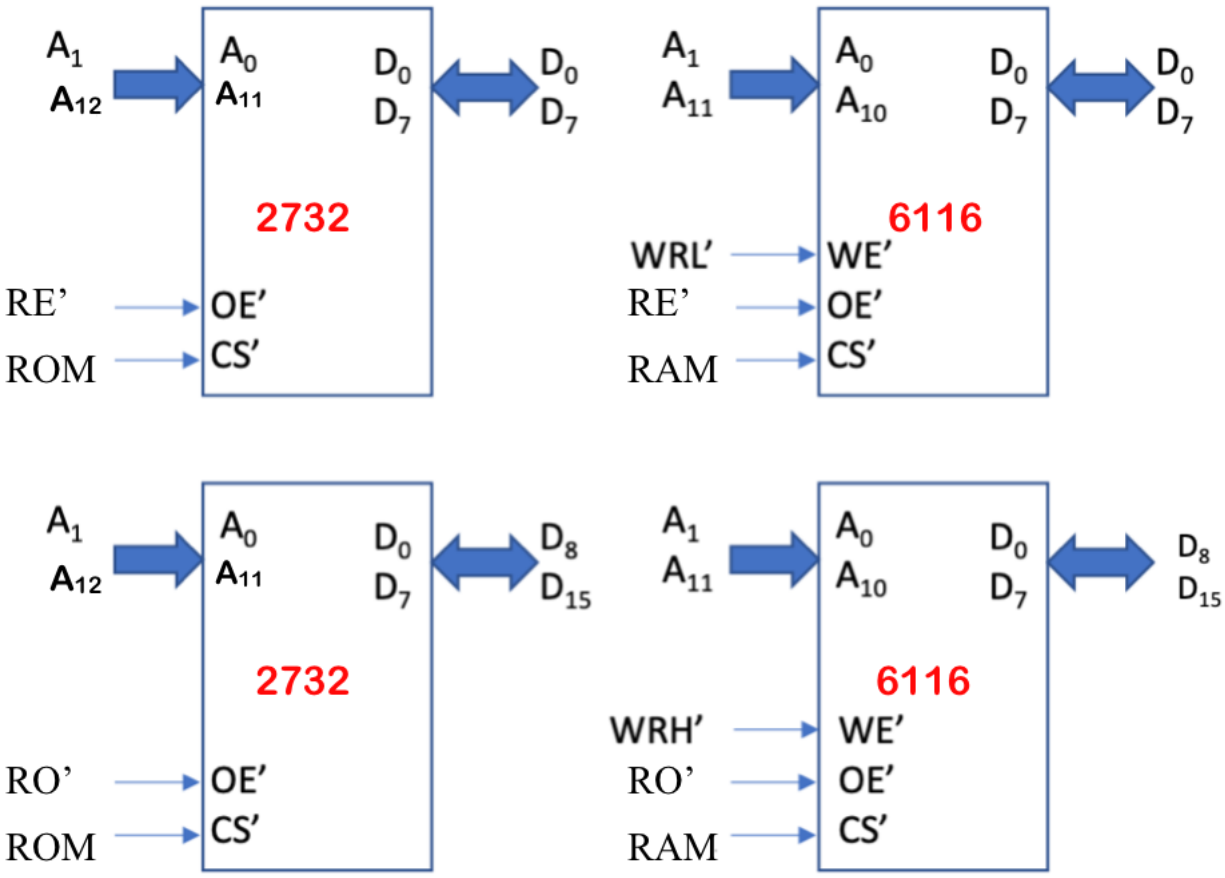
MEMORY DECODING LOGIC



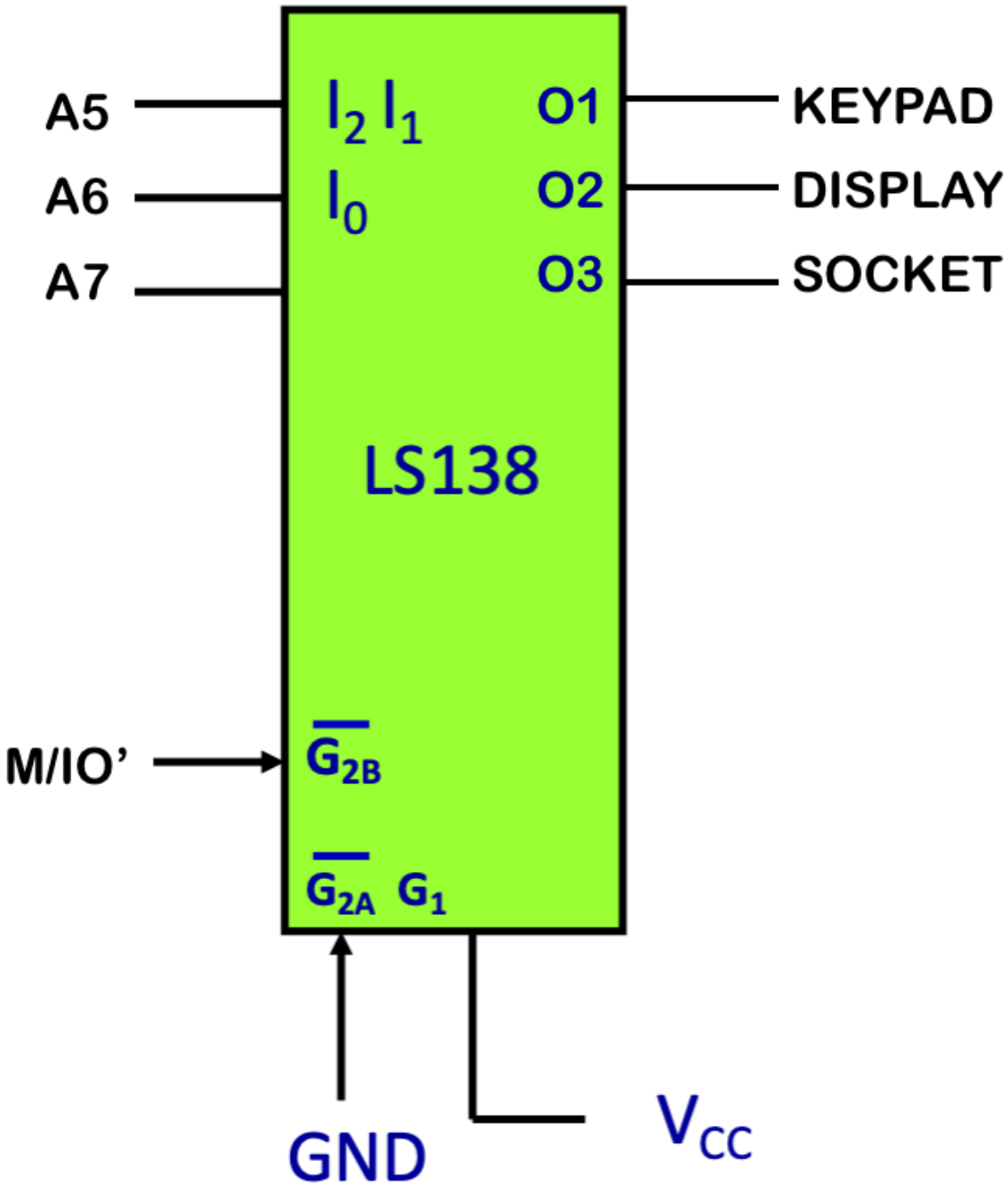




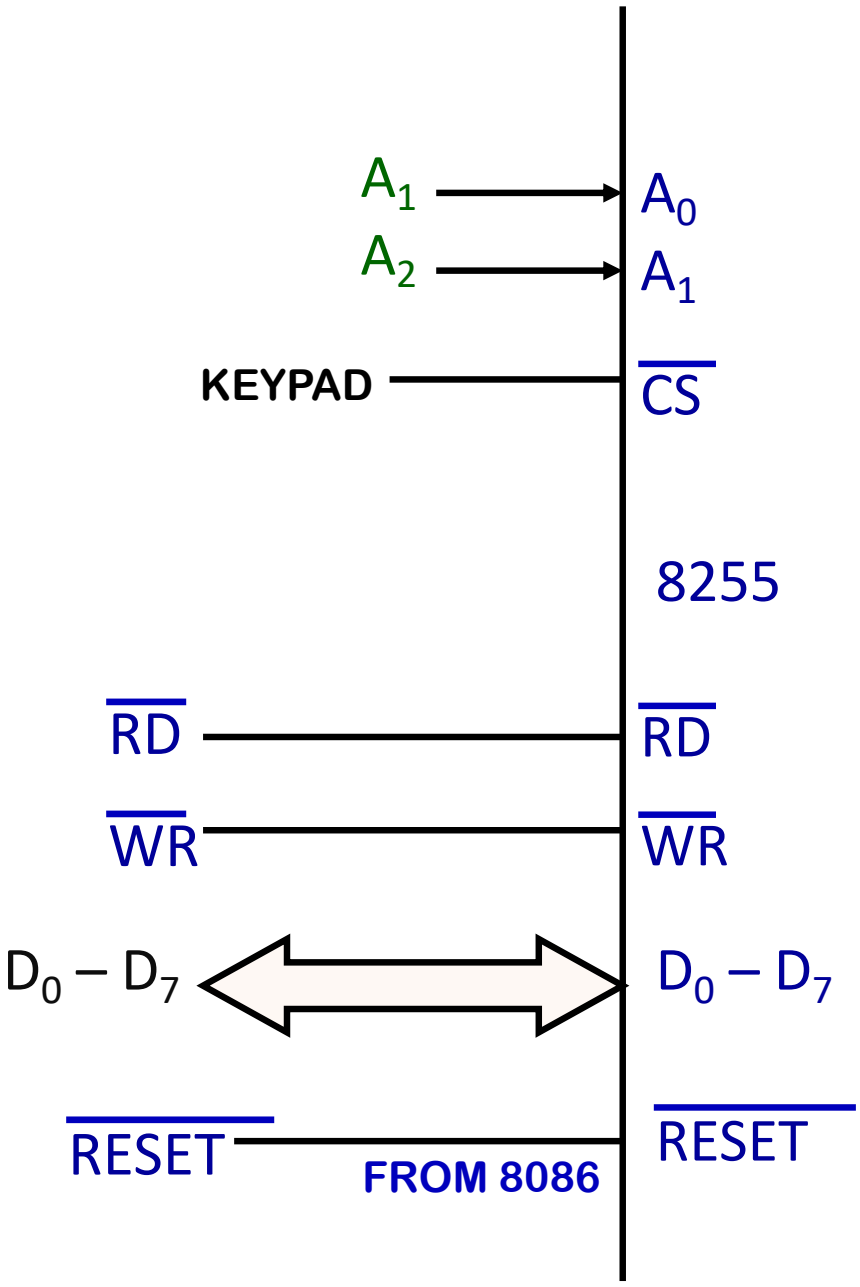
❖ MEMORY LAYOUT



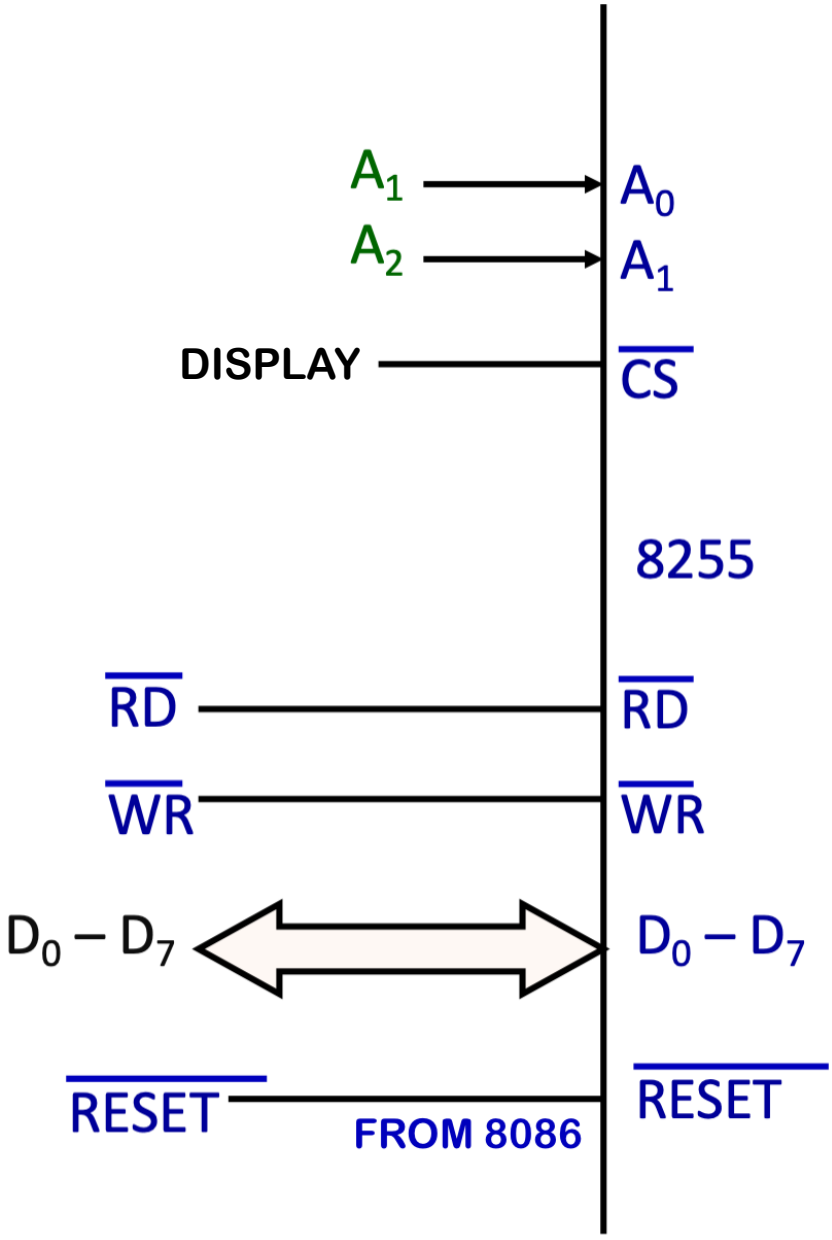
❖ I/O DECODER


A5
A6
A7
I_2 I_1
I_0
O1
O2
O3
KEYPAD
DISPLAY
SOCKET
LS138
M/IO'
$\overline{G_{2B}}$
$\overline{G_{2A}}$ G_1
GND
V_{CC}

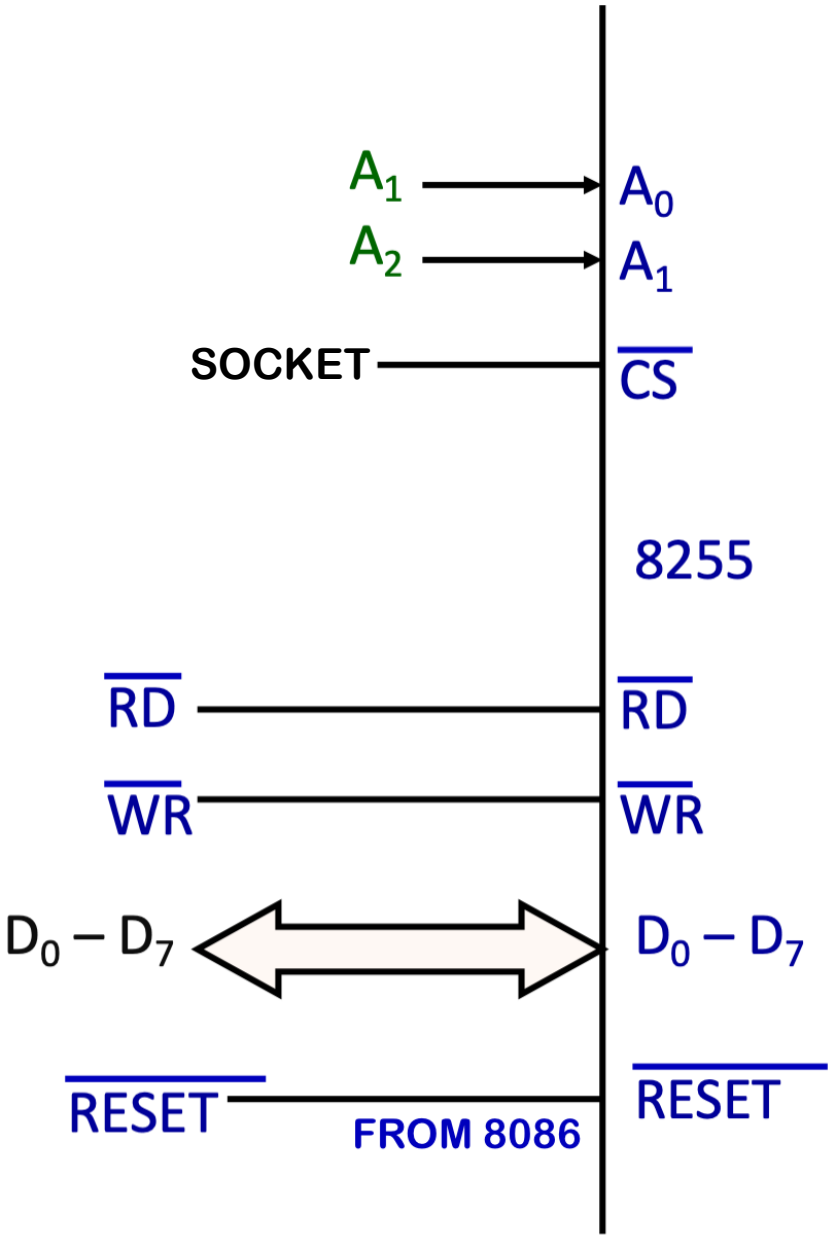
❖ KEYBOARD 8255 INTERFACE



❖ DISPLAY 8255 INTERFACE



❖ ZIF SOCKET 8255 INTERFACE



❖ KEYPAD AND 7SEG-MPX6-CC DISPLAY