NEW HORIZON
COLLEGE OF ENGINEERING
New Horizon Knowledge Park, Ring Road, Marathalli
Autonomous College Permanently Affiliated to VTU, Approved by AICTE & UGC
Accredited by NAAC with 'A' Grade, Accredited by NBA

" Enhanced Voting Machine Simulation Using VHDL"

A MINI PROJECT REPORT

Submitted by

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In partial fulfillment for the award of the degree of

BACHELOR OF ENGINEERING

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the mini project work entitled "**Enhanced Voting Machine Simulation Using VHDL**" carried out by **Nithish Kumar Reddy G (1NH18EC032),Sai Pradeep K(1NH18EC056), Praneeth Kumar D(1NH18EC028),Sankar Sai K(1NH18EC059)** bonafide students of Electronics and Communication Department, New Horizon College of Engineering, Bangalore.

The mini project report has been approved as it satisfies the academic requirements in respect of mini project work prescribed for the said degree.

Project Guide (Deepak Kumar S N)	HOD ECE (Dr. Sanjeev Sharma)
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External Viva

Name of Examiner	Signature with Date
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The satisfaction that accompany the successful completion of any task would be, but impossible without the mention of the people who made it possible, whose constant guidance and encouragement helped us succeed.

We thank **Dr. Mohan Manghnani**, Chairman of **New Horizon Educational Institution,** for providing necessary infrastructure and creating good environment.

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Abstract

Traditional paper based voting procedure was very long and time-consuming process and very much prone to errors. Polling by Electronic Voting Machine (EVM) is a simple, safe and secure method that takes minimum of time. Current Electronic Voting Machine (EVMs) used in LOK SABHA and ASSEMBLY elections accepts only one vote from each voter. But in elections such as GRAMA PANCHAYAT and COOPERATIVE SOCIETIES, where each voter casts their votes to more than one candidate, available voting machines will not work. The paper presents a PROGRAMMABLE ELECTRONIC VOTING MACHINE that accepts one or more votes depending on requirement. Mode control is included in EVM, through which it is possible to set the EVM to accept more than one vote from each voter depending on the type of elections. The main advantage of this type of EVM is to avoid the invalid votes especially in co-operative society elections where each voter has to cast vote for nine candidates.

Introduction

Elections in India are conducted almost exclusively by using electronic voting machines developed over the past two decades by a pair of govemment-owned companies. These devices, known in India as EVMs, have been praised for their simple design, ease of use, and reliability. The Electronic Voting Machine (EVM) consists of two interconnected units, the Ballot Unit where the voter casts his vote by pressing a button alongside the name of the candidate and symbol of the party for whom the person chooses to vote for and the Control Unit by which the polling official enables the Ballot Unit for the voter to cast his vote and where all related data like number of votes polled for each candidate, total number of votes cast etc. resides. EVMs reduce the time in both casting a vote and declaring the results compared to the old ballot paper system. The control unit can store the result in its memory for more than 10 years. Invalid votes can be greatly reduced by use of EVMs. Blank votes can be counted. Despite many advantages of EVMs, there are certain issues in terms of software and hardware.

In the existing voting machines, number of candidates supported is limited to around 20 only, if number of candidates exceeds to 20 we are supposed to use 2 voting machines. At present, EVMs are used only in LOK SABHA and ASSEMBLY elections (it accepts only one vote from each voter), but in elections such as GRAMA PANCHAYATH and COOPERATIVE SOCIETIES where each voter cast their votes to more than one candidate,available voting machines can not be used.

This paper presents a PROGRAMMABLE ELECTRONIC VOTING MACHINE that accepts one or more votes depending on our requirement. Here, we have included the mode contol, through this we can set the EVM to accept more than one vote from each voter (it can accept 1 or 2 or 3 .... or n votes) depending on the type ofelections.

Our Contributions are mainly in designing priority and multiple weighted based voting, where a vote for multiple persons for a positions. Weights of preferences will be used to get final vote counting

The paper is organized as follows. First, working of present EVM is discussed, with its limitations in present Voting system.Second, proposed work to overcome present EVM is discussed along with block diagram (modules) and working(in terms of state diagram).Finally, simulation results, conclusion, and future work are expected to be presented.

Introduction to VHDL

The VHSIC Hardware Description Language is an industry standard language used to describe hardware from the abstract to the concrete level. VHDL resulted from work done in the 70s and early 80s by the U.S. Department of Defence.VHDL usage has risen rapidly since its inception and is used by literally tens of thousands of engineers around the globe to create sophisticated electronic products. VHDL is a powerful language with numerous language constructs that are capable of describing very complex behaviour.

Learning all the features of VHDL is not a simple task. Complex features will be introduced in a simple form and then more complex usage will be described. In 1986, VHDL was proposed as an IEEE standard. It went through a number of revisions and changes until it was adopted as the IEEE 1076 standard in December 1987.

Entity:-All designs are expressed in terms of entities. An entity is the most basic building block in a design. The uppermost level of the design is the top-level entity. If the design is hierarchical, then the top-level description will have lower-level descriptions contained in it.These lower-level descriptions will be lower-level entities contained in the top-level entity description.

Architecture:- All entities that can be simulated have an architecture description.The architecture describes the behavior of the entity. A single entity can have multiple architectures. One architecture might be behavioural while another might be a structural description of the design

Literature Review:

1)Author and Year of Publication:Atiya Parveen,Sobia Habib,Daoud sarvar in 2003

Outcome:Worked on"Scope and Limitation of Electronic Voting System"In Paper Based Process the election workers will visit the residential addresses to ensure that those persons actually live there and as certain that they have given the correct information about themselves. After validation, identification card will be issued to the voters.

Limitations:A lot of paper work was concerned in the whole procedure.Appropriate training will be required for the staff members in charge of polling duty. At polling date, the concerned staff members are required to be present half hour prior to the opening of the polling booth/station to check that all arrangements have been done correctly.

2) Author and Year of Publication: Michael D Byrne,Kriston K Greene, Sarah P Everett in 2007

Outcome:They proposed a scheme called "Punch Card Method" based on the Votomatic system. This system uses a special cards where each possible hole is pre-scored and allowing perforations to be made by the voter pressing a stylus through a guide in the voting machine. Scoring of the punch cards was also done by hand and not by a punchcard reader.

Limitations:They do not suffer touchscreen calibration problem.

Existing System: Electronic Voting Machine (EVM)

Electronic Voting Machine (also known as EVM) is voting using electronic means to either aid or take care of the chores of casting and counting votes.An EVM is designed with two units: the control unit and the balloting unit. These units are joined together by a cable. The control unit of the EVM is kept with the presiding officer or the polling officer.

The balloting unit is kept within the voting compartment for electors to cast their votes. This is done to ensure that the polling officer verifies your identity.With the EVM, instead of issuing a ballot paper, the polling officer will press the Ballot Button which enables the voter to cast their vote.

A list of candidates names and/or symbols will be available on the machine with a blue button next to it. The voter can press the button next to the candidate's name they wish to vote for.

Problem Statement:

To clearly state that the PANCHAYAT AND CO OPERATIVE Society elections are time consuming.To overcome this problem,we are using Programmable Electronic Voting Machine (EVM).With this there will be a less chance of error.To make it more it is difficult to hack as there are thousand number of permutations and combinations.So to save time and money properly it is the best method.

Software Used: XILINX Design Suit 12.1

---Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx.Used for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli.

---It is used to configure the target device with the programmer.Xilinx ISE is a design environment for FPGA products from Xilinx.It is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.

---Xilinx's patented algorithms for synthesis allow designs to run up to 30% faster than competing programs, and allows greater logic density which reduces project time and costs.

---Also, due to the increasing complexity of FPGA fabric, including memory blocks and I/O blocks, more complex synthesis algorithms were developed that separate unrelated modules into slices, reducing post-placement errors.

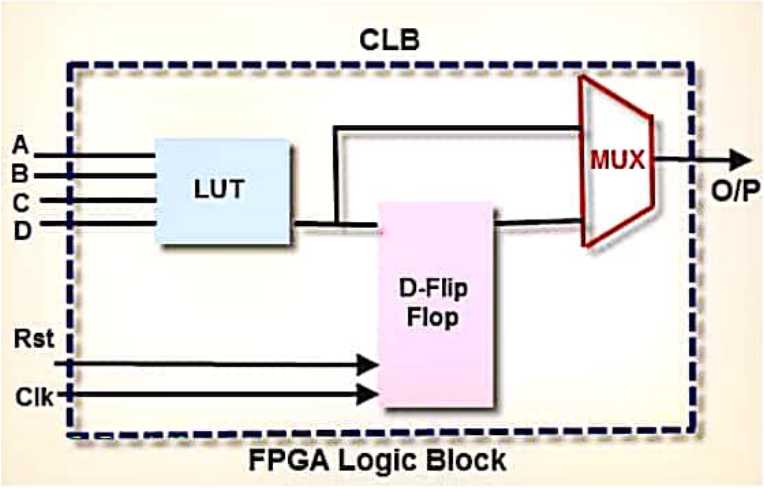
---IP Cores are offered by XILINX and other third-party vendors, to implement system-level functions such as digital signal processing (DSP), bus interfaces, networking protocols, image processing, embedded processors, and peripherals. Xilinx has been instrumental in shifting designs from ASIC based implementation to FPGA-based implementation.

Hardware: FPGA (any)

FPGA is a Field Programmable Gate Array.It is a type of devices mostly used in electronics circuits.FPGA contains programmable logic blocks and interconnection circuits.It is a semi conductor device.It can be programmable/reprogrammable to the required functionality after manufacturing.The configurable logic blocks are the basic logic unit of an FPGA.It is made up of two basic components: Flip-flops and look-up tables.

FPGAs provide benifits to designers of smart energy grids, aircraft navigation, automotive drivers assistance, medical ultrasounds and data center search engines.FPGA functionality can be changed on every power-up of the device.So,when a designer wants to change or modify anything regarding the program they can simply download a new configuration file into the device and can try out the change.Changes can be made to FPGA without replacing costly PC board.ASICs have fixed hardware functionality.So can't be changed without large amount of cost and time.This is the big difference between FPGA and ASIC.

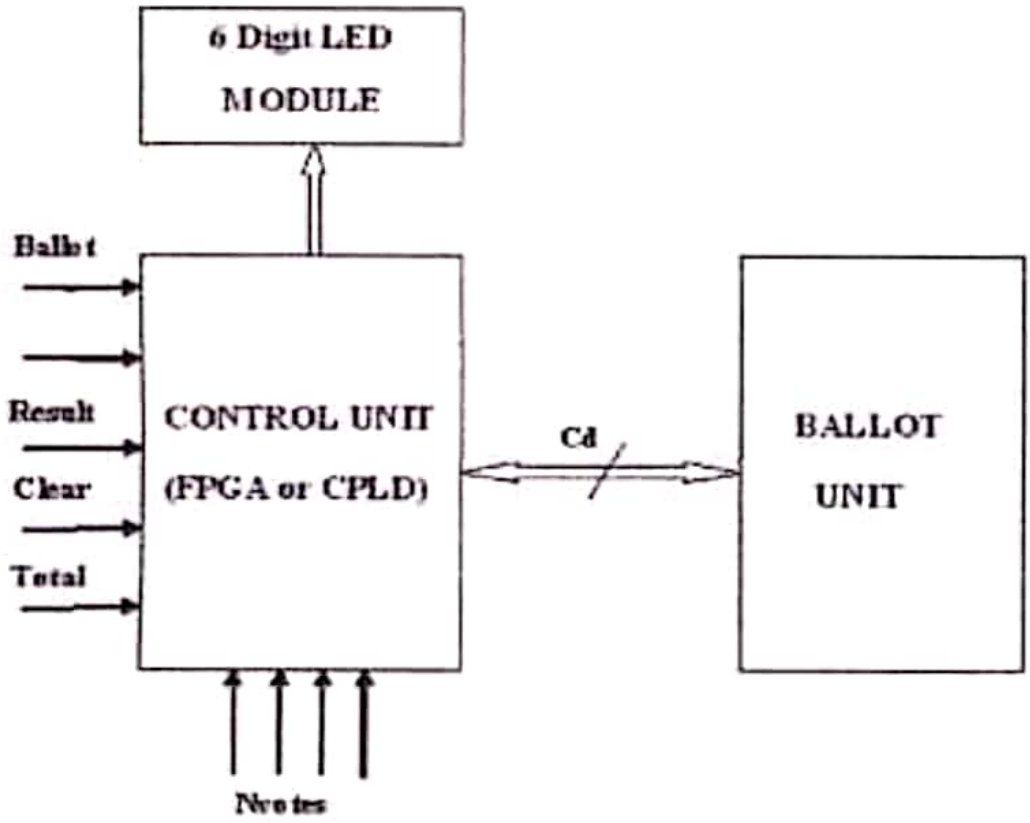
FPGAs are sold off the shell.It provides off load and acceleration functions to CPUs, effectively speeding up the entire system performance.It reduce risk, allowing prototype systems to ship to customers for field trials,while still providing the ability to make changes quickly before ramping to volume production.



Proposed System:

1)Our project is Programmable Electronic Voting Machine (EVM) Using VHDL code in XIILINX software which is later dumped into FPGA kit.
2)We already have an EVM'S for General elections.But in elections such as panchayat and co operative, each voter has to cast more than one vote.
3)Election commission is using paper ballot for such type of elections.It is time consuming.
4)Here,we are trying to make programmable EVM to cast n number of votes.
5)We are dumping the code in FPGA kit,so that we will get a hardware component of it.
6)The main advantage of it is time and money saving.

Block Diagram Of Programmable EVM:



Working:

EVM consists of mainly two interconnected units, ballot (implemented with FPGA/CPLD) and control unit (implemented with FPGA), and display module (LEDs) as given in the block diagram. In the ballot unit, voter casts his/her vote by pressing a button along side the name of the candidate and symbol of the party for whom the person chooses to vote. Control unit is given to the polling official, who enables the ballot unit for the voter to cast his vote,and all related data like number of votes polled for each candidate, total number of votes cast, etc., resides in it.

The controls such as ballot, count, result, clear, total, Nvotes, clk, and cd are used to control operations of control unit. Display module is used to display alphanumeric characters. MSB 2 digits are used to display candidate serial number and rest 4 digits are used to display the total number of votes casted for corresponding candidate.

The process of voting is as follows. Once the validity of the voter has been ensured, the polling official enables the ballot unit and the voter is asked to go to the area where the ballot unit is placed. Then, the voter scrutinizes the names of the candidates or parties displayed on the ballot unit and cast his vote by pressing the blue (any) button beside the chosen candidate's name or symbol. The corresponding LED is lit and an audible beep is heard confirming the registration of vote in the system. This process is repeated for the next voter.

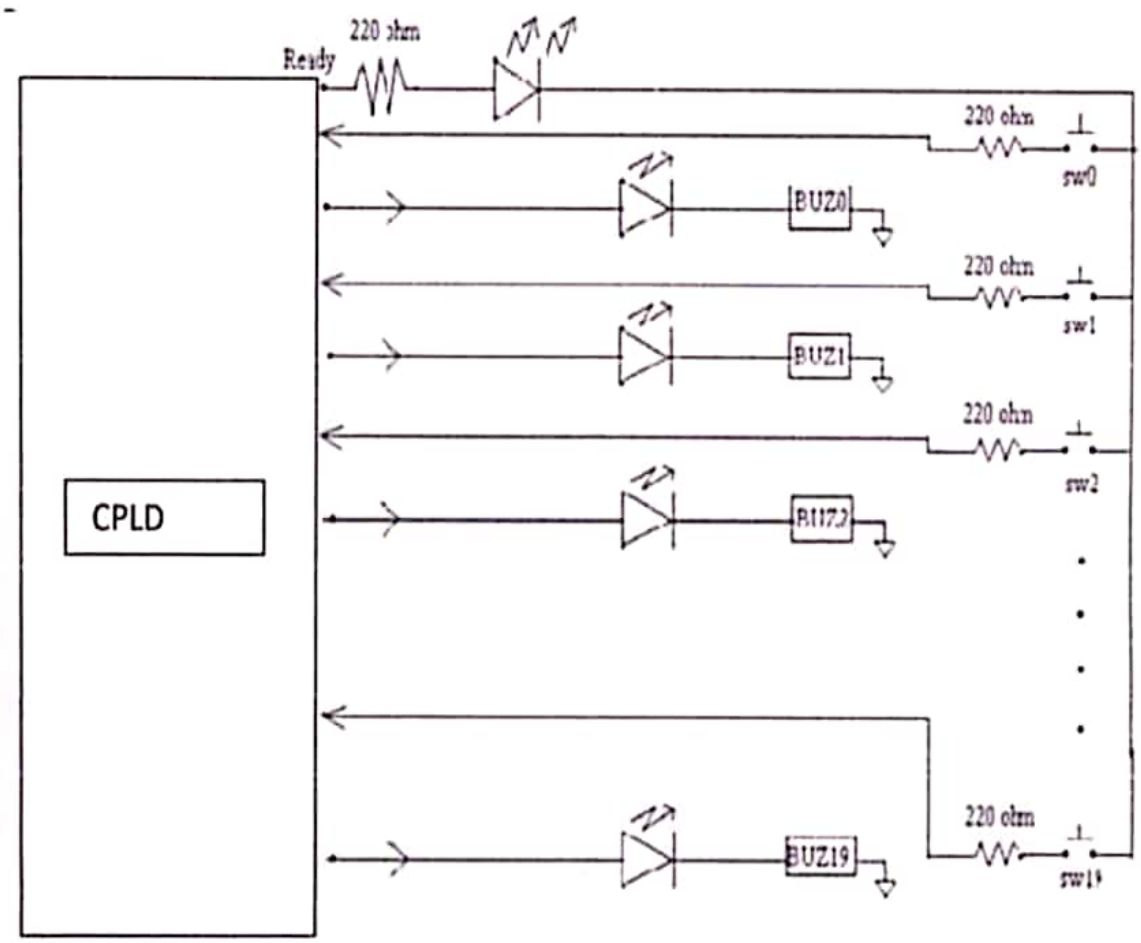
On operation of the "Result" button of the Control Unit, the display indicates the results of the poll including total number of votes cast and the number of votes polled for each candidate.

Ballot unit:

The Circuit diagram of ballot unit shows the internal block diagram of the ballot unit of the Programmable EVM. It consists of LEDs and push to on switches corresponding to the number of candidates on the ballot unit along with 220 ohms resistors in series used to drive the push to on switches, with the power supply of +5v .

The operation is as follows when the voter presses the blue button (one of swO to sw19) to cast the vote for his chosen candidate, the corresponding push to on switch gets closed, and a high signal is sent to the contol unit, if this signal is enabled, then the counter gets incremented indicating the registration of the vote and the conformation is done when the red LED glows (corresponding to pressed switch) and a beep sound is heard.

Circuit Diagram Of Ballot Unit:

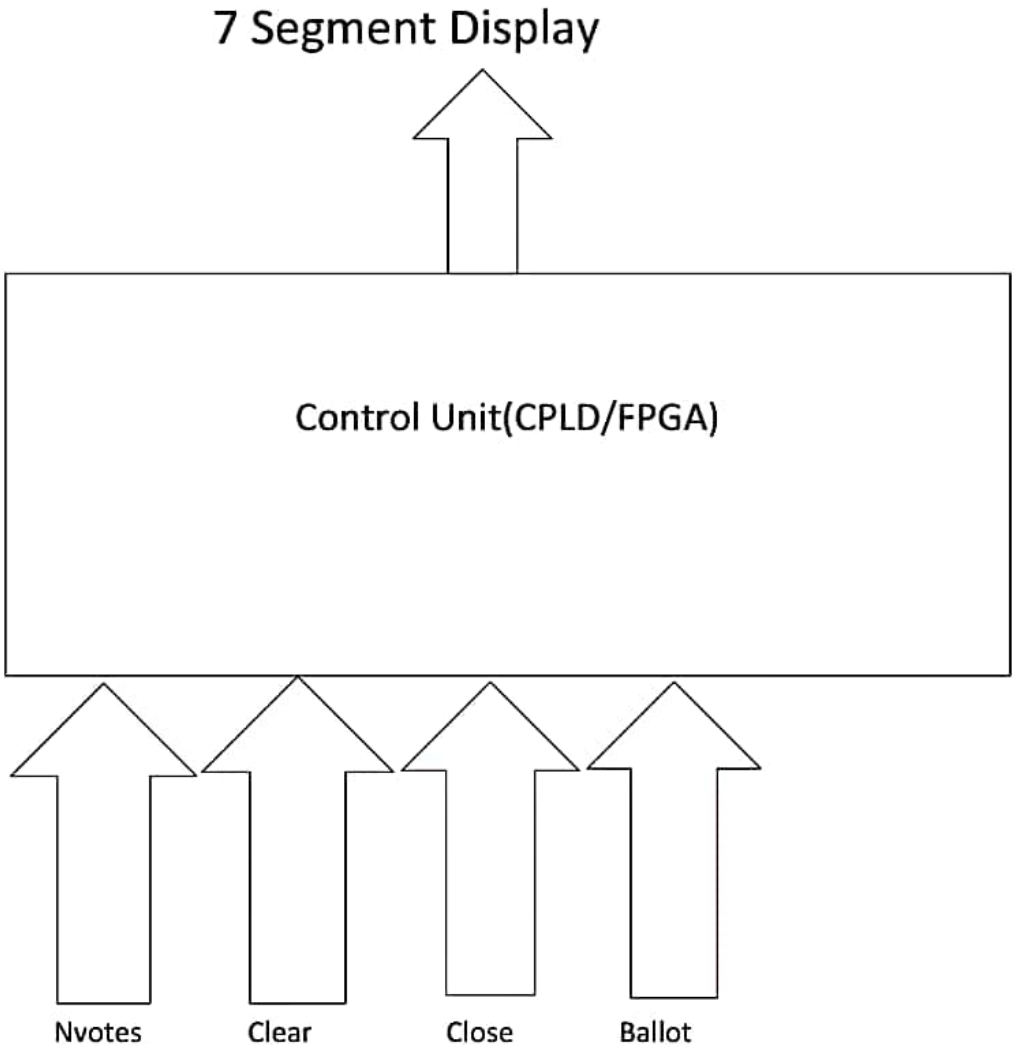


Control Unit:

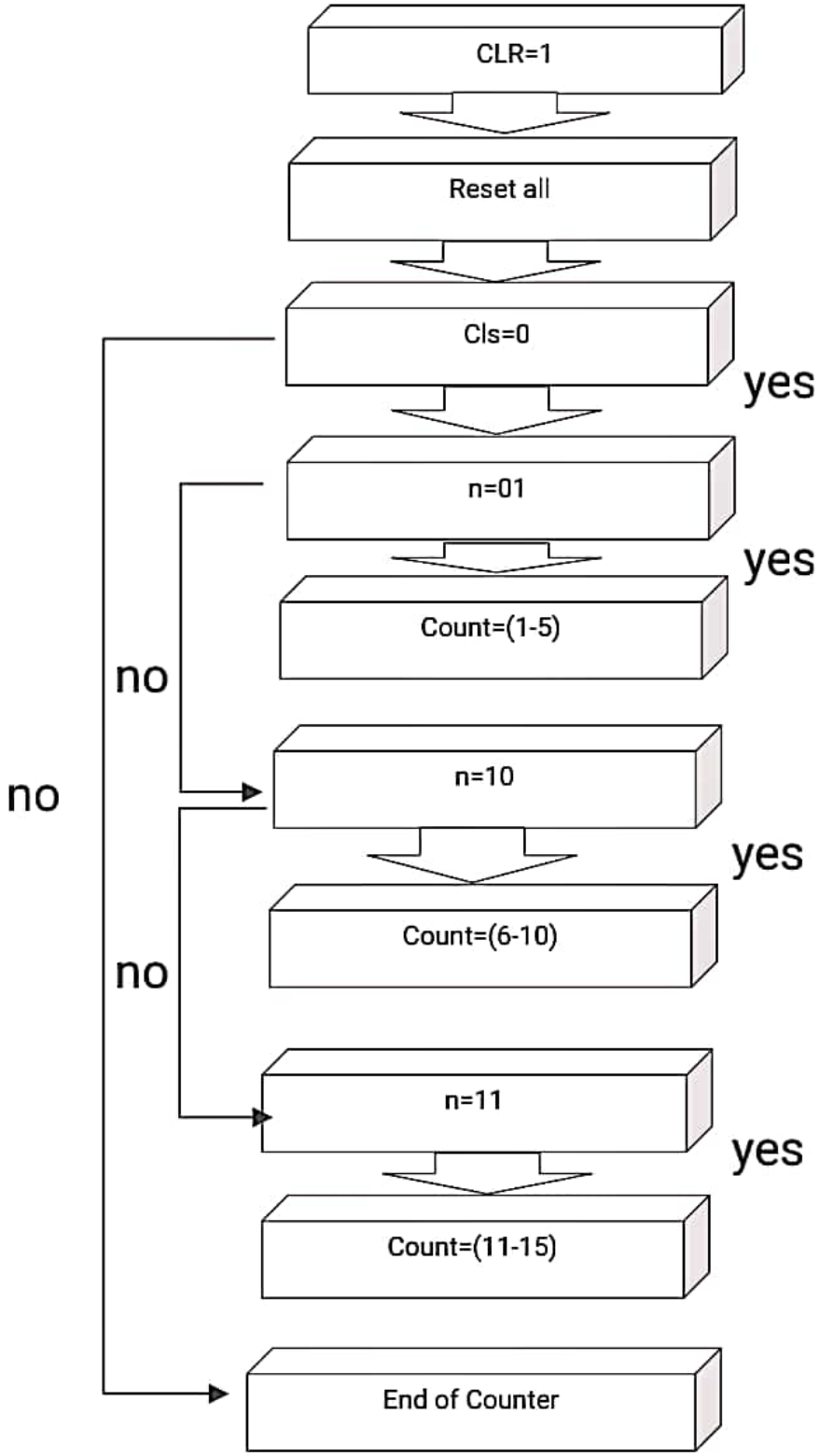
The 'Nvotes' is set by the presiding officer, which indicates the number of votes to be accepted from individual voters. 'Ballot' is also under the cotrol of presiding officer, which is set to accept votes from voter.

'Clear' is set in order to store the votes registered for individual candidate in to FPGA ROM. When 'Result' is set high the number of votes accepted for each candidate, which is stored in ROM is displayed on multiplexed seven segment LED display provided.It is shown in the block diagram of Control unit.

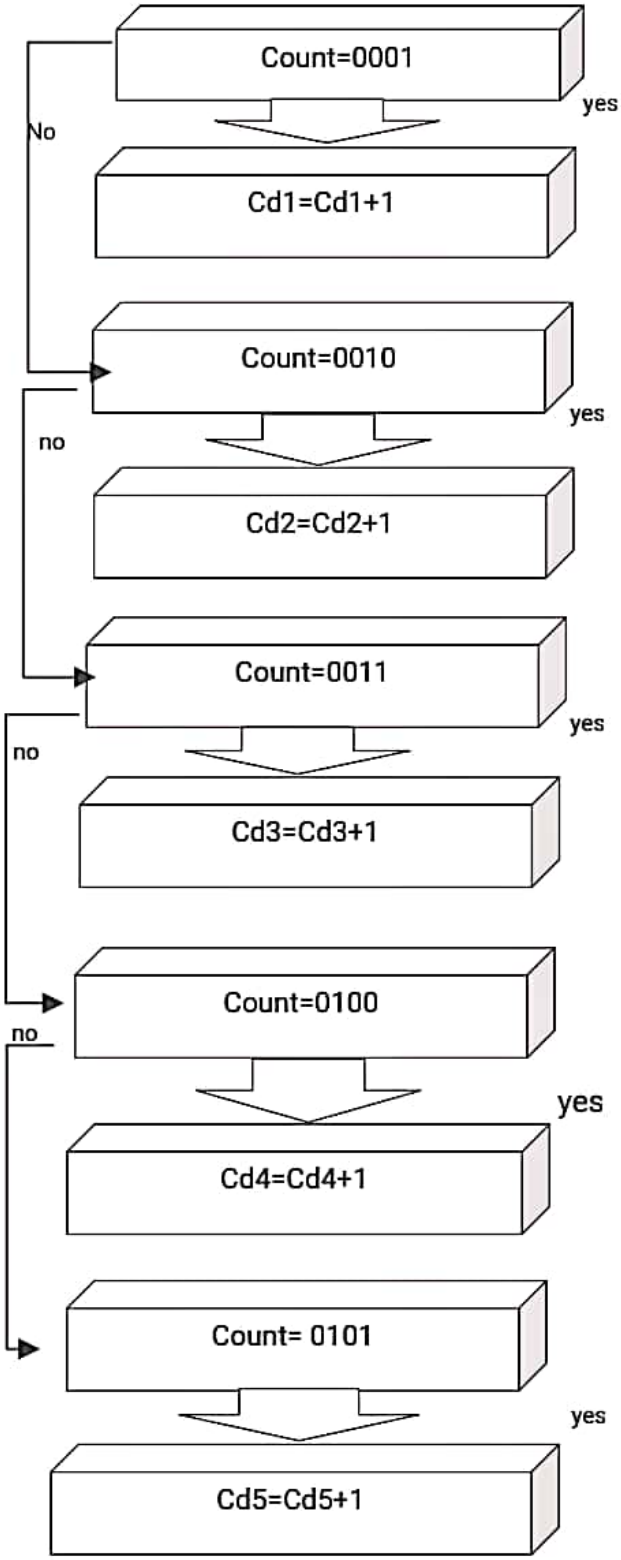
Block Diagram Of Control Unit:



Flow diagram of EVM:



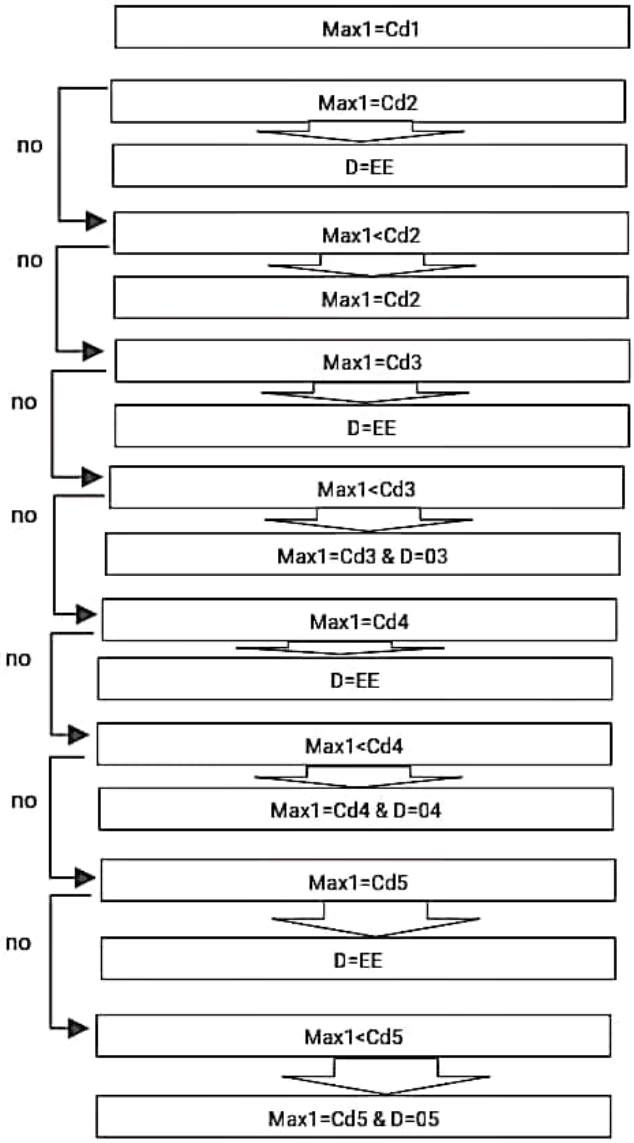
Design of Counter:



Counter is designed for incrementing the number of votes of each candidate after a voter cast his/her vote to a particular candidate.

Design of Comparator:

The Control unit Compares the total votes of each candidate no. having maximum vote in the seven segment display.



ADVANTAGES OF ELECTRONIC VOTING:

One of the advantages of electronic voting is that, in most cases, most ballots will be tabulated into the results. Paper-based voting machines can actually miss ballots because of human error in placing the paper-based ballot in the machine.

Another advantage is obviously the ease of tabulating the results. All counting and ordering is done by a machine, quickly and efficiently, and without human error.

Direct Recording Electronic(DRE) voting machines also have the advantage of never running out of paper ballots at a polling center, since the computer can count an unlimited number of ballots. They also can provide multiple languages to users who may not have English as a first language. This cannot be achieved through a paper-based system.

There are also advantages when dealing with people with disabilities, such as blindness.Electronic voting machines can provide headphones to read off instructions to the blind user.Also other tools can be added to these electronic voting machines to help with other disabilities such as people with limited mobility or the elderly.

DISADVANTAGES OF ELECTRONIC VOTING:

Also, besides tampering with the machines electronically, machines couid be tampered physically, with foreign software being uploaded into the machine by someone trying to corrupt the election results.

Another disadvantage of electronic voting systems could be the overall costs. Software, machines, installations, proper software protection, and validation of results could be expensive; even more expensive than paper-based machines.

There could also be just a general error in the system, without any outsider tampering. computer software and systems can have problems that may delay or even halt voting, or may cause errors in calculations.

Future Enhancement:

Enhancement of this project involves the security section of the EVM. The security section of the EVM is one of the main parts of the project where each voter will hold an individual voting card and his/her finger print will be the password.The computer will scan the identity of the voter and then the polling officer will allow the voter to cast his/her vote if found illegible.

Conclusion:

In earlier elections we as a voter, casted vote to our favourite candidate by putting the stamp against his/her name and then folding the ballot paper as per a prescribed method before putting it in the Ballot box. This. is a long, time-consuming process and very much prone to errors. Polling by Electionic Voting Machine(EVM) is a simple,safe and secure method that takes minimum of time. In this article, programmable EVM that accepts more than one vote from individual voter, depending on type of elections,is presented.This voting machine has an advantage that it can be used in all kinds of elections like gram panchayat,Co-operative societies, General assembly elections etc,.It can also consider priority as weightage when voter has capability to provide multiple preferences.

Discussion:

1)As we have seen, since these days politicians are arguing that voting machines are hackable and we have seen 'In an US Expo,a below10 year old kid hacked and put his name as winner in the board.
2) So we have choosen this project to make it unhackable ie through programming of EVM
3) We have observed that there are thousands of permutations and combinations,so it is not a simple task to hack

Result:

As of now still we are in the middle of the project,so still hands-on experience on hardware components should go on, simulation results are pending.So it will take some time to get a netlist,RTL schematic and test bench waveforms.

Reference:

1)Basic VLSI Design by Douglas A.Puncknell & Kamran Eshraghian

2)http:/www.xilinx.com/itp/xilinx10/books/docs/qst/qst.pdf

3)www.xilinx.com ISE Tutorial in Depth Chapter 2,Chapter 3

4)www.xilinx.com ISE Tutorial in Depth Chapter 4,Chapter 5,Chapter 6

5)http//www.ece.wpi.edu/spartan3_Tutorial.pdf, accessed date- Mar 5 2013

6)http://www.bellindia.com/BELWebsite/images/EVM_Features. pdf

Appendix

Program for Electronic Voting Machine

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

---Uncomment the following library declaration if instantiating
---any Xilinx primitives in this code.
---linrary UNISM;
--use UNISM.VComponents.all;

entity evm is
port(clk:in std_logic;
        clr:in std_logic;
          cls:in std_logic;
          count:in std_logic_vector(3 downto 0);
          max1,max2,max3:inout std_logic_vector(9 downto 0);
          d1,d2,d3,d4,d5,d6:out std_logic_vector(6 downto 0);
          n:in std_logic_vector(1 down 0);

cd1,cd2,cd3,cd4,cd5,cd6,cd7,cd8,cd9,cd10,cd11,cd12,cd13,cd14,cd15:inout
std_logic_vector(9 downto 0));
end evm;
```

```
architecture behavioural of evm is


begin

process(clk,clr,count,n,cls,cd1,cd2,cd3,cd4,cd5,cd6,cd7,cd8,cd9,cd10,cd11,cd12,c
d13,cd14,cd15,max1,max2,max3)

begin

if(clk='1' and clk'event) then

    if(clr='1') then

        cd1<="0000000000";cd2<="0000000000";cd3<="0000000000";

        cd4<="0000000000";cd5<="0000000000";cd6<="0000000000";

        cd7<="0000000000";cd8<="0000000000";cd9<="0000000000";

        cd10<="0000000000";cd11<="0000000000";cd12<="0000000000";


        cd13<="0000000000";cd14<="0000000000";cd15<="0000000000";

        max1<="0000000000";max2<="0000000000";max3<="0000000000";

        d1<="0000000";d2<="0000000";d3<="0000000";

        d4<="0000000";d5<="0000000";d6<="0000000";

  end if;


if(cls='0')


    if(n="01") then

        if(count="0001") then

                cd1<=cd1+1;
```

```
        elsif(count="0010") then
                cd2<=cd2+1;
        elsif(count="0011") then
                cd3<=cd3+1;
        elsif(count="0100") then
                cd4<=cd4+1;
        elsif(count="0101") then
                cd5<=cd5+1;
      end if;


  elsif(n="10") then
  if(count="0110") then
                cd6<=cd6+1;
       elsif(count="0111") then
                cd7<=cd7+1;
       elsif(count="1000")then;
            cd8<=cd8+1;
       elsif(count="1001") then
            cd9<=cd9+1;
       elsif(count="1010") then
            cd10<=cd10+1;
  end if;

elsif(n="11") then
```

```
    if(count="1011") then
            cd11<=cd11+1;
    elsif(count="1100") then
            cd12<=cd12+1;
    elsif(count="1101") then
            cd13<=cd13+1;
    elsif(count="1110") then
            cd14<=cd14+1;
    elsif(count="1111") then
            cd15=cd15+1;
     end if;
  end if;
end if;

if(n="01") then

    max1<=cd1;
            d1<="0000000";
            d2<="0110000";

    if(max1=cd2) then
            d1<="1001111";
             d2<="1001111";
    elsif(max1<cd2) then
              max1<=cd2;
```

```
            d1<="0000000";
             d2<="1101101";

elsif(max1=cd3) then
        d1<="1001111";
        d2<="1001111";
elsif(max1<cd3) then
       max1<=cd3;
       d1<="0000000";
       d2<="1111001";


elsif(max1=cd4) then
        d1<="1001111";
        d2<="1001111";
elsif(max1<cd4) then
        max1<=cd4;
        d1<="0000000";
        d2<="0110011";

elsif(max1=cd5) then
        d1<="1001111";
        d2<="1001111";
  elsif(max1<cd5) then
            max1<=cd5;
```

```
            d1<="0000000";
            d2<="1011011";

   end if;
end if;

if(n="10") then
             max2<=cd6;
             d3<="0000000";
            d4<="1011111";

      if(max2=cd7) then
            d3<="1001111";
           d4<="1001111";
     elsif(max2<cd7) then
            max2<=cd7;
            d3<="0000000";
            d4<="1110000";

elsif(max2=cd8) then
            d3<="1001111";
            d4<="1001111";
     elsif(max2<cd8) then
            max2<=cd8;
            d3<="0000000";
```

```
            d4<="1111111";

    elsif(max2=cd9) then
            d3<="1001111";
            d4<="1001111";
     elsif(max2<cd9) then
          max2<=cd9;
           d3<="0000000";
           d4<="1111011";

    elsif(max2=cd10) then
          d3<="1001111";
          d4<="1001111";
    elsif(max2<cd10) then
          max2<=cd10;
          d3<="0110000";
          d4<="0000000";
  end if;
end if;

if(n="11") then
          max3<=cd11;
          d5<="0110000";
          d6<="0110000";
```

```
if(max3=cd12) then
        d5<="1001111";
        d6<="1001111";
    elsif(max3<cd12) then
         max3<=cd12;
         d5<="0110000";
         d6<="1101101";

elsif(max3=cd13) then
        d5<="1001111";
        d6<="1001111";
    elsif(max3<cd13) then
         max3<=cd13;
         d5<="0110000";
         d6<="1111001";

    elsif(max3=cd14) then
         d5<="1001111";
         d6<="1001111";
    elsif(max3<cd14) then
         max3<=cd14;
         d5<="0110000";
         d6<="0110011";

    elsif(max3=cd15) then
```

```
            d5<="1001111";
            d6<="1001111";
      elsif(max3<cd15) then
              max3<=cd15;
            d5<="0110000";
            d6<="1011011";
    end if;
end if;
end if;
end process;

end behavioural;
```