

74LS283
Adder

4-Bit Full Adder With Fast Carry
Product Specification

Logic Products

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry lookahead

DESCRIPTION

The '283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$\begin{aligned} &C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) \\ &\quad + 4(A_3 + B_3) + 8(A_4 + B_4) \\ &= \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT} \end{aligned}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic) - see Function Table. In case of all active LOW operands the results $\Sigma_1 - \Sigma_4$ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---------|---------------------------|--------------------------------|
| 74LS283 | 13ns | 20mA |

ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$ |
|---------------|--|
| Plastic DIP | N74LS283N |
| Plastic SO-16 | N74LS283D |

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

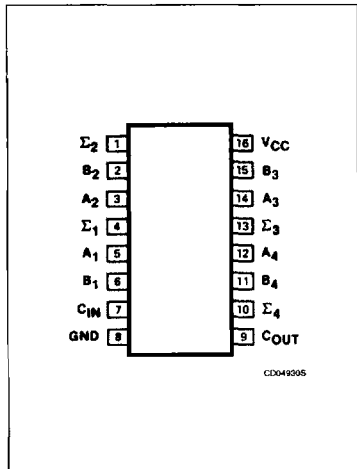
| PINS | DESCRIPTION | 74LS |
|----------|-------------|--------|
| A, B | Inputs | 2LSul |
| C_{IN} | Input | 1LSul |
| All | Outputs | 10LSul |

NOTE:

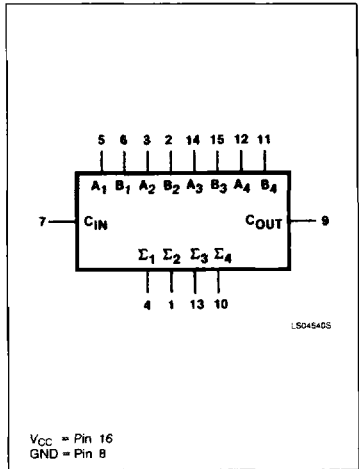
A 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

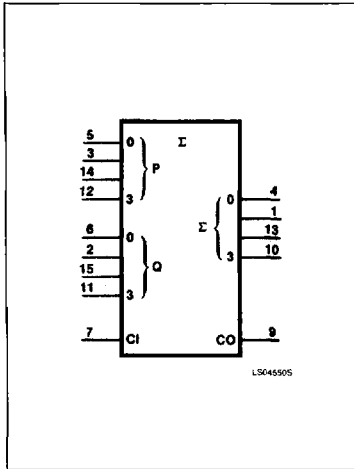
PIN CONFIGURATION



LOGIC SYMBOL



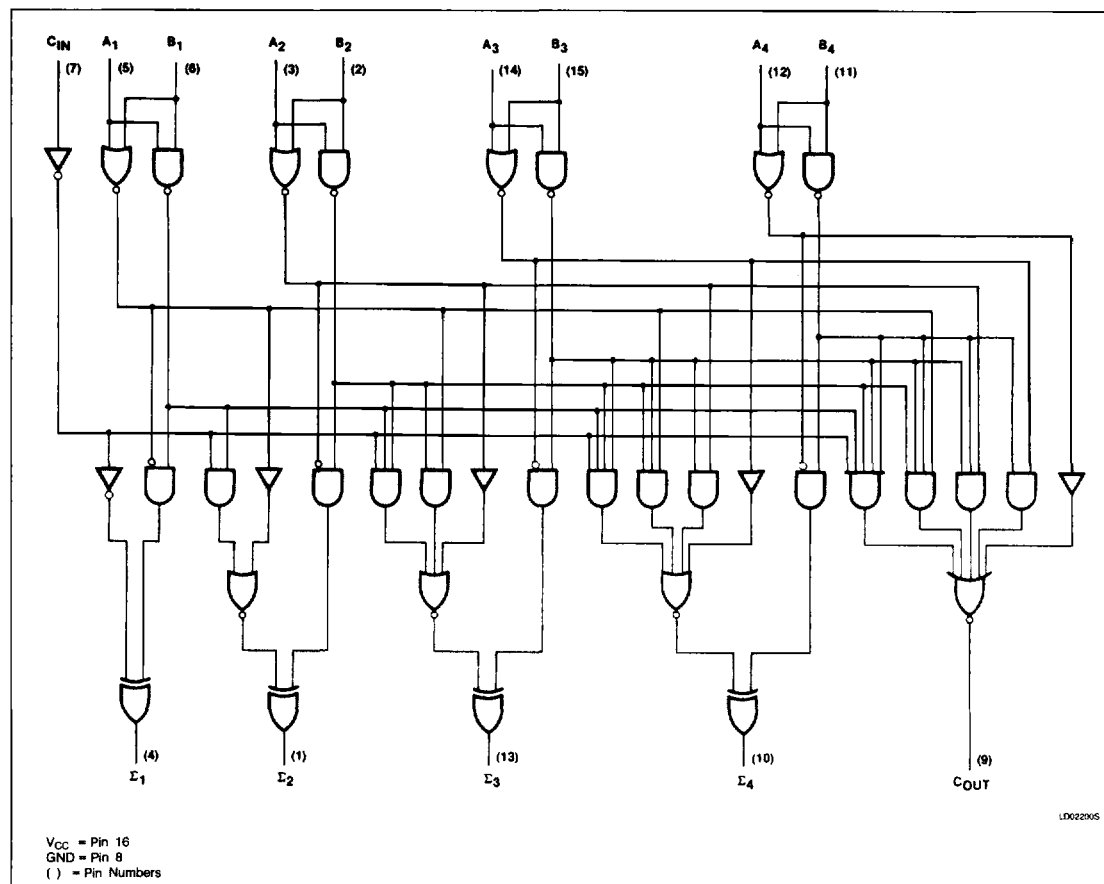
LOGIC SYMBOL (IEEE/IEC)



Adder

74LS283

LOGIC DIAGRAM



FUNCTION TABLE

| PINS | C_{IN} | A_1 | A_2 | A_3 | A_4 | B_1 | B_2 | B_3 | B_4 | Σ_1 | Σ_2 | Σ_3 | Σ_4 | C_{OUT} |
|--------------|----------|-------|-------|-------|-------|-------|-------|-------|-------|------------|------------|------------|------------|-----------|
| Logic levels | L | L | H | L | H | H | L | L | H | H | H | L | L | H |
| Active HIGH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Active LOW | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

H = HIGH voltage level

L = LOW voltage level

Example:

 1001
 1010

 10011
 (10 + 9 = 19)
 (carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | 74LS | UNIT |
|--|--------------------|------|
| V_{CC} Supply voltage | 7.0 | V |
| V_{IN} Input voltage | -0.5 to +7.0 | V |
| I_{IN} Input current | -30 to +1 | mA |
| V_{OUT} Voltage applied to output in HIGH output state | -0.5 to + V_{CC} | V |
| T_A Operating free-air temperature range | 0 to 70 | °C |

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RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | UNIT |
|-----------------|--------------------------------|------|-----|------|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| V _{IH} | HIGH-level input voltage | 2.0 | | | V |
| V _{IL} | LOW-level input voltage | | | +0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | HIGH-level output current | | | -400 | μA |
| I _{OL} | LOW-level output current | | | 8 | mA |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

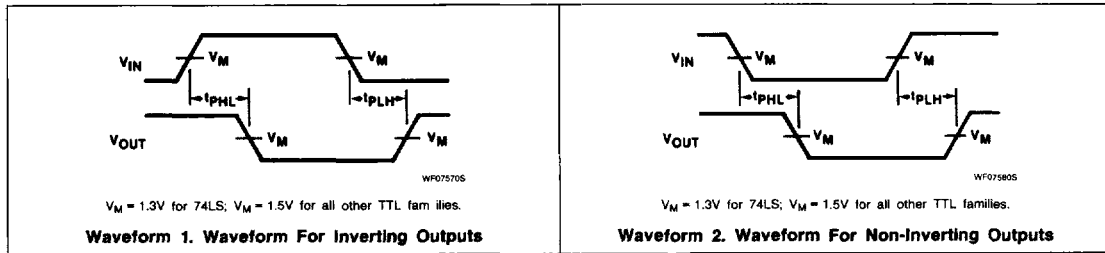
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| PARAMETER | | TEST CONDITIONS ¹ | 74LS283 | | | UNIT |
|-----------------|---|--|---------|------------------|------|------|
| | | | Min | Typ ² | Max | |
| V _{OH} | HIGH-level output voltage | V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX | 2.7 | 3.4 | | V |
| V _{OL} | LOW-level output voltage | V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX | | 0.35 | 0.5 | V |
| | | V _{IL} = MAX, I _{OL} = 4mA (74LS) | | 0.25 | 0.4 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | | -1.5 | V |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7.0V | | | 0.2 | mA |
| | | A, B inputs | | | 0.1 | mA |
| I _{IH} | HIGH-level input current | V _{CC} = MAX, V _I = 2.7V | | | 40 | μA |
| | | C _{IN} input | | | 20 | μA |
| I _{IL} | LOW-level input current | V _{CC} = MAX, V _I = 0.4V | | | -0.8 | mA |
| | | C _{IN} input | | | -0.4 | mA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | -20 | | -100 | mA |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = MAX | | 22 | 39 | mA |
| | | Condition 2 | | 19 | 34 | mA |
| | | Condition 3 | | 19 | 34 | mA |

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} should be measured with all outputs open and the following conditions:
Condition 1: All inputs grounded.
Condition 2: All B inputs LOW, other inputs at 4.5V.
Condition 3: All inputs at 4.5V.

AC WAVEFORMS



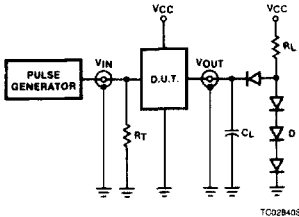
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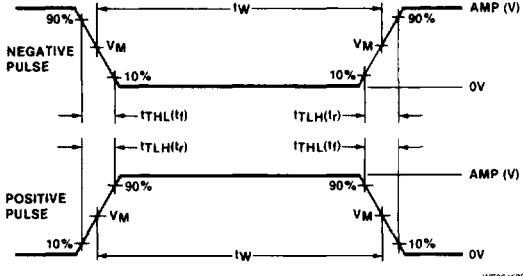
AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

| PARAMETER | | TEST CONDITIONS | 74LS | | UNIT |
|------------------------|---|-----------------|---|----------|------|
| | | | $C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$ | | |
| | | | Min | Max | |
| t_{PLH} t_{PHL} | Propagation delay C_{IN} to Σ_1 | Waveforms 1 & 2 | | 24 24 | ns |
| t_{PLH} t_{PHL} | Propagation delay C_{IN} to Σ_2 | Waveforms 1 & 2 | | 24 24 | ns |
| t_{PLH} t_{PHL} | Propagation delay C_{IN} to Σ_3 | Waveforms 1 & 2 | | 24 24 | ns |
| t_{PLH} t_{PHL} | Propagation delay C_{IN} to Σ_4 | Waveforms 1 & 2 | | 24 24 | ns |
| t_{PLH} t_{PHL} | Propagation delay A_i or B_i to Σ_i | Waveforms 1 & 2 | | 24 24 | ns |
| t_{PLH} t_{PHL} | Propagation delay C_{IN} to C_{OUT} | Waveform 2 | | 17 22 | ns |
| t_{PLH} t_{PHL} | Propagation delay A_i or B_i to C_{OUT} | Waveforms 1 & 2 | | 17 17 | ns |

TEST CIRCUITS AND WAVEFORMS



TC02B40S



WF36450S

$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|-------------|-----------|-----------|
| | Amplitude | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 74 | 3.0V | 1MHz | 500ns | 7ns | 7ns |
| 74LS | 3.0V | 1MHz | 500ns | 15ns | 6ns |
| 74S | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |