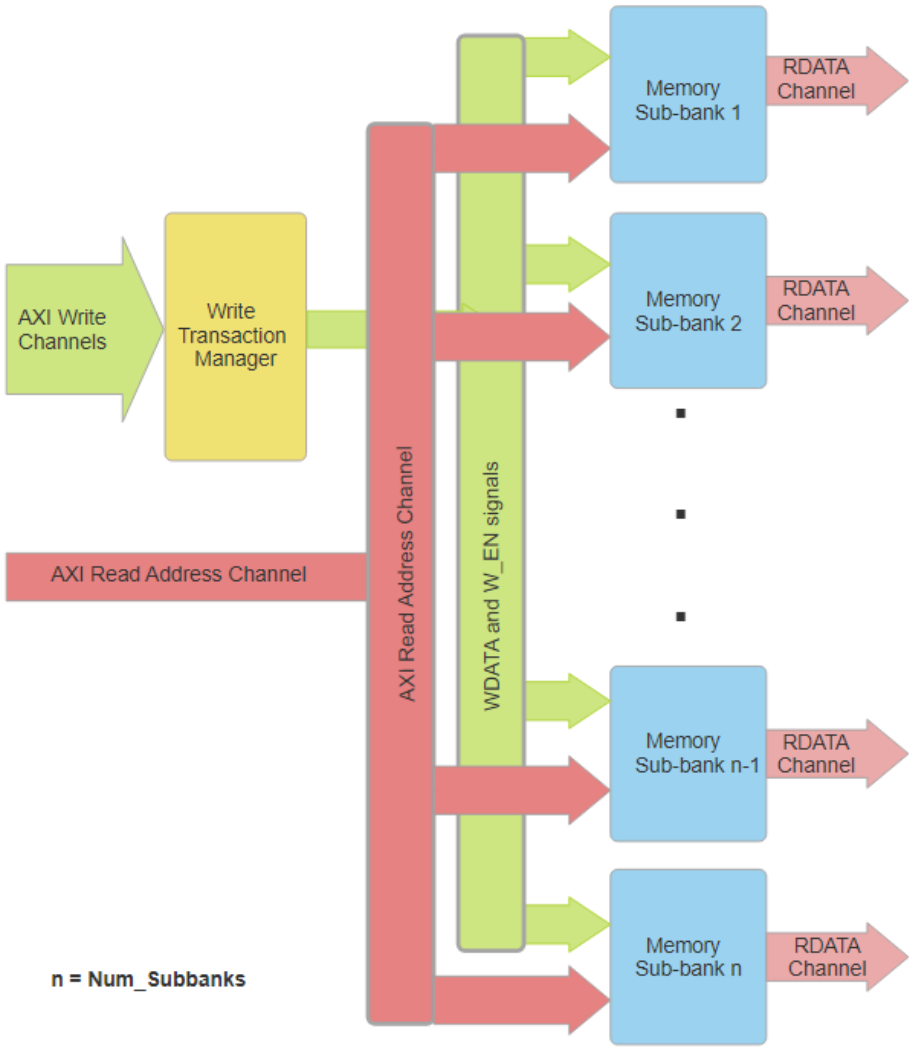
Understanding Multi-Addressable AXI Memory

(by **Praneeth KSS)**

This document provides information about the Multi-Addressable AXI memory module designed in SystemVerilog. The module interfaces with AXI protocols and is highly parameterizable.

'multirport_axi_memory' module

This is the top-level module of the multi-port AXI memory system, consisting of multiple sub-memory banks (**axi_memory**), each handling AXI transactions.



Parameters

- **Num_Subbanks:** Number of sub-memory banks (default: 32)
- **Subbank_size:** Size of each sub-memory bank (default: 32 words)
- **word_size:** Word size in bits (default: 32 bits)
- **R_ADDR_WIDTH:** Read address width (default: 5 bits)
- **W_ADDR_WIDTH:** Write address width (default: 10 bits)
- **DATA_WIDTH:** Data width (default: 32 bits)

Ports

- **Global Signals**: ACLK (Clock signal), ARESETn (Active low reset)
- **Control Signals**: W_EN (Write enable), R_EN (Read enable)
- **Write Address Channel Signals**: AWVALID, AWREADY, AWADDR, AWBURST, AWLEN
- **Write Data Channel Signals**: WVALID, WREADY, WDATA, WLAST
- **Write Response Channel Signals**: BVALID, BREADY, BRESP
- **Read Address Channel Signals**: ARVALID, ARREADY, ARADDR (Common for all Sub-banks)
- **Read Data Channel Signals**: RVALID, RREADY, RDATA, RRESP (One per each Sub-bank)

Functional Description

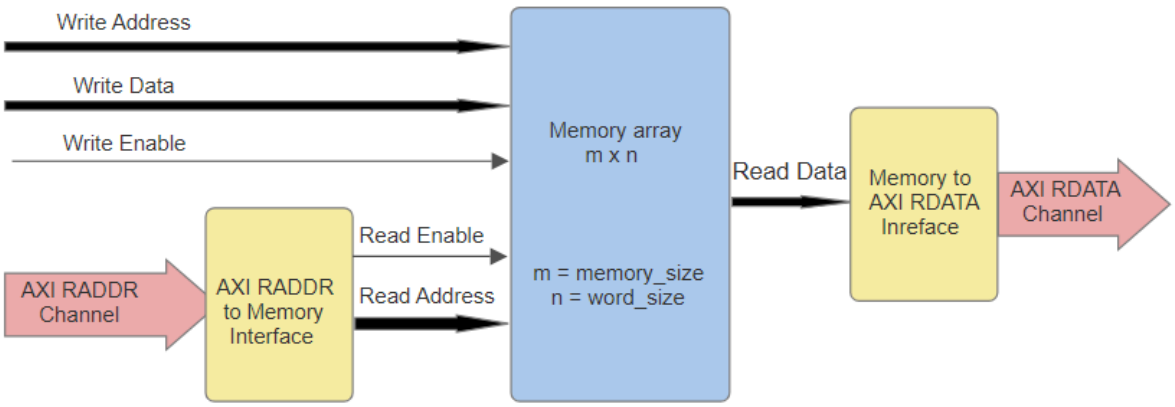
The **multirport_axi_memory** module manages multiple read ports and a single write port across several sub-memory banks. During write operations, when AWVALID and WVALID are asserted, it processes the address and data phases, distributing the write enable signal to the appropriate subbank based on the address. Each subbank has its own AXI read channels, allowing concurrent read operations, with ARVALID signaling the read address phase and RREADY handling the data phase. The write response is generated collectively for all subbanks, ensuring a unified response signal. The module's design supports both fixed and incremental burst types for write operations, enhancing its flexibility and performance.

Additional Notes

- Each subbank has its own AXI read channels but does not support individual AXI write operations. The AXI write is implemented as a whole for all the subbanks.

‘axi_memory’ module

This module represents a single sub-memory bank capable of handling AXI read transactions.



Parameters

- **word_size:** Word size in bits (default: 32 bits)
- **memory_size:** Memory size in words (default: 32 words)
- **ADDR_WIDTH:** Address width (default: 5 bits)
- **DATA_WIDTH:** Data width (default: 32 bits)

Ports

- **Global Signals**: ACLK (Clock signal), ARESETn (Active low reset)
- **Control Signals**: R_EN (Read enable), W_EN (Write enable)
- **Write Address Channel Signals**: AWADDR
- **Write Data Channel Signals**: WDATA
- **AXI Read Address Channel Signals**: ARVALID, ARREADY, ARADDR
- **AXI Read Data Channel Signals**: RVALID, RREADY, RDATA, RRESP

Functional Description

The **axi_memory** module supports AXI read transactions and traditional write transaction and is sub-memory bank. When W_EN is high, data from WDATA is written to the memory at the address specified by AWADDR on the negative clock edge. During read operations, the module processes the address phase when ARVALID is asserted, then reads data from the memory at ARADDR, and outputs it on RDATA when RREADY is asserted. The module ensures that valid signals and response codes are generated for each read transaction, handling errors if the address is out of bounds.