EEE 4134

VLSI I Laboratory

COMPARATIVE ANALYSIS OF FULL ADDERS USING 9, 10, 14 AND 16 TRANSISTORS IN CADENCE® VIRTUOSO®

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Section: A

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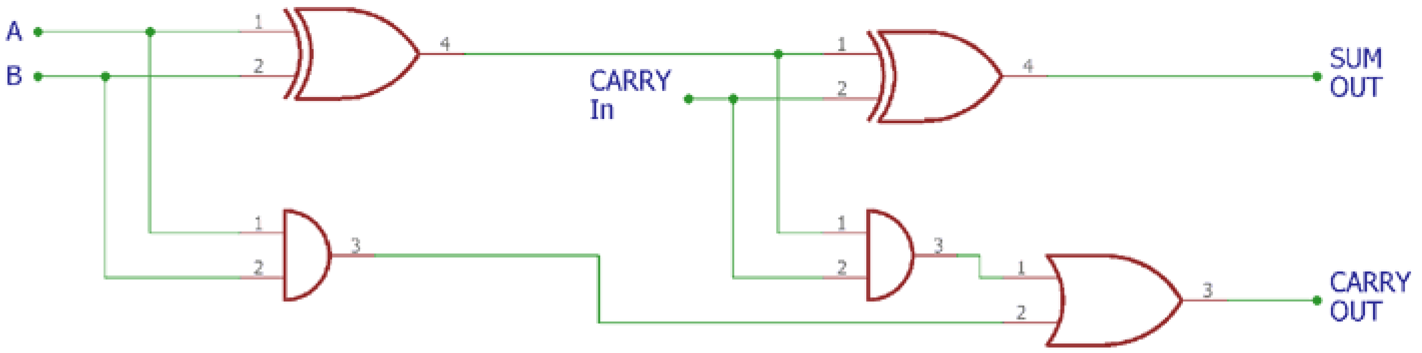
INTRODUCTION

Full Adders are the foundational unit of Arithmetic VLSI circuits found in every processors and microcontroller inside Arithmetic and Logic units (ALU).

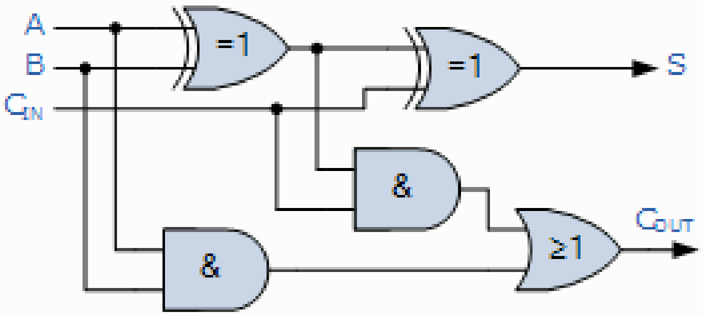
PRINCIPLE OF FULL ADDER



Full-Adder Circuit

TRUTH TABLE OF FULL ADDER

Sum S=(A XOR B)XOR C
C_{out}=A AND B OR (A XOR B)

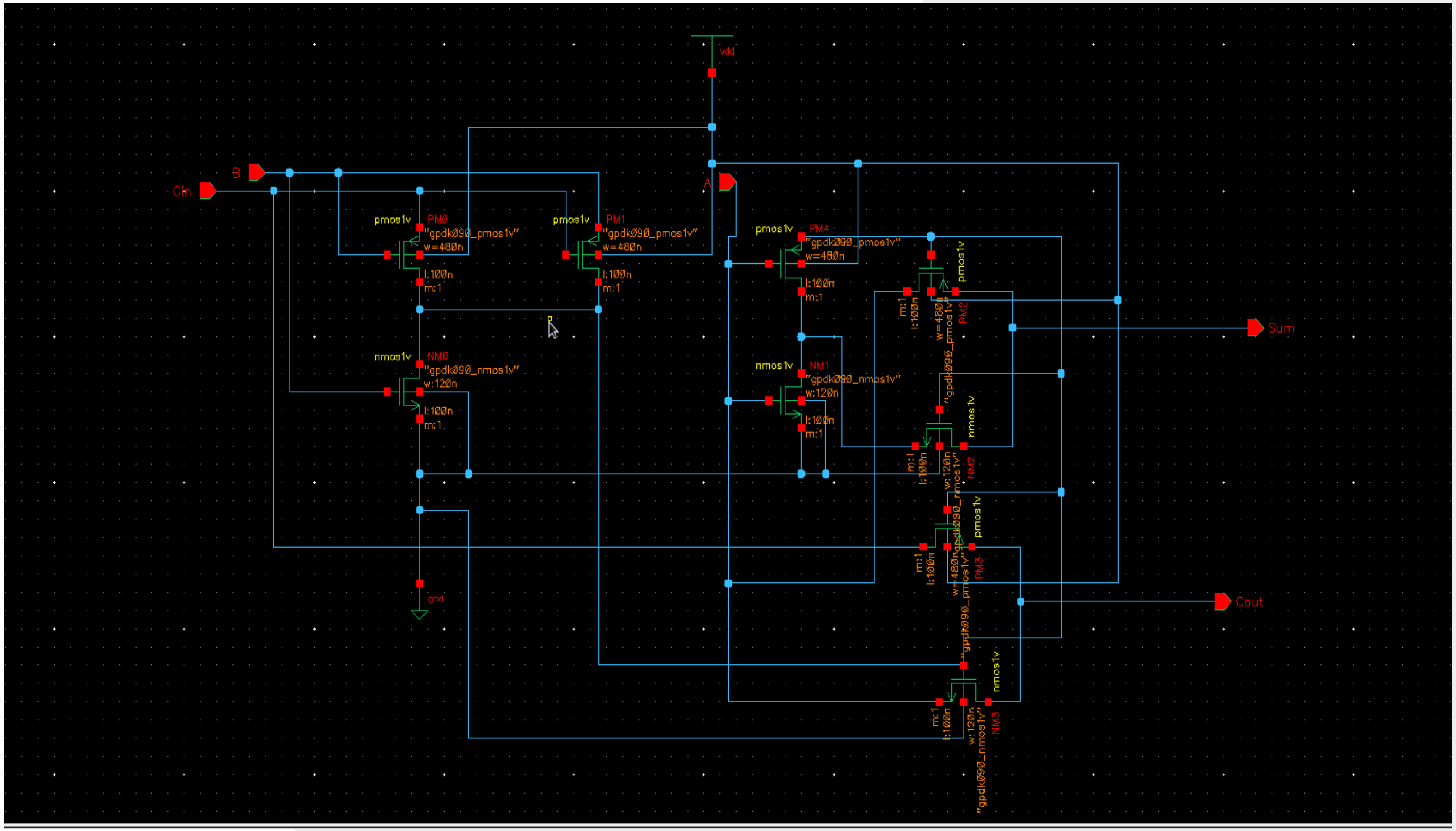


Symbol	Truth Table				
	C-in	B	A	Sum	C-out
	0	0	0	0	0
	0	0	1	1	0
	0	1	0	1	0
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	1
	1	1	0	0	1
	1	1	1	1	1

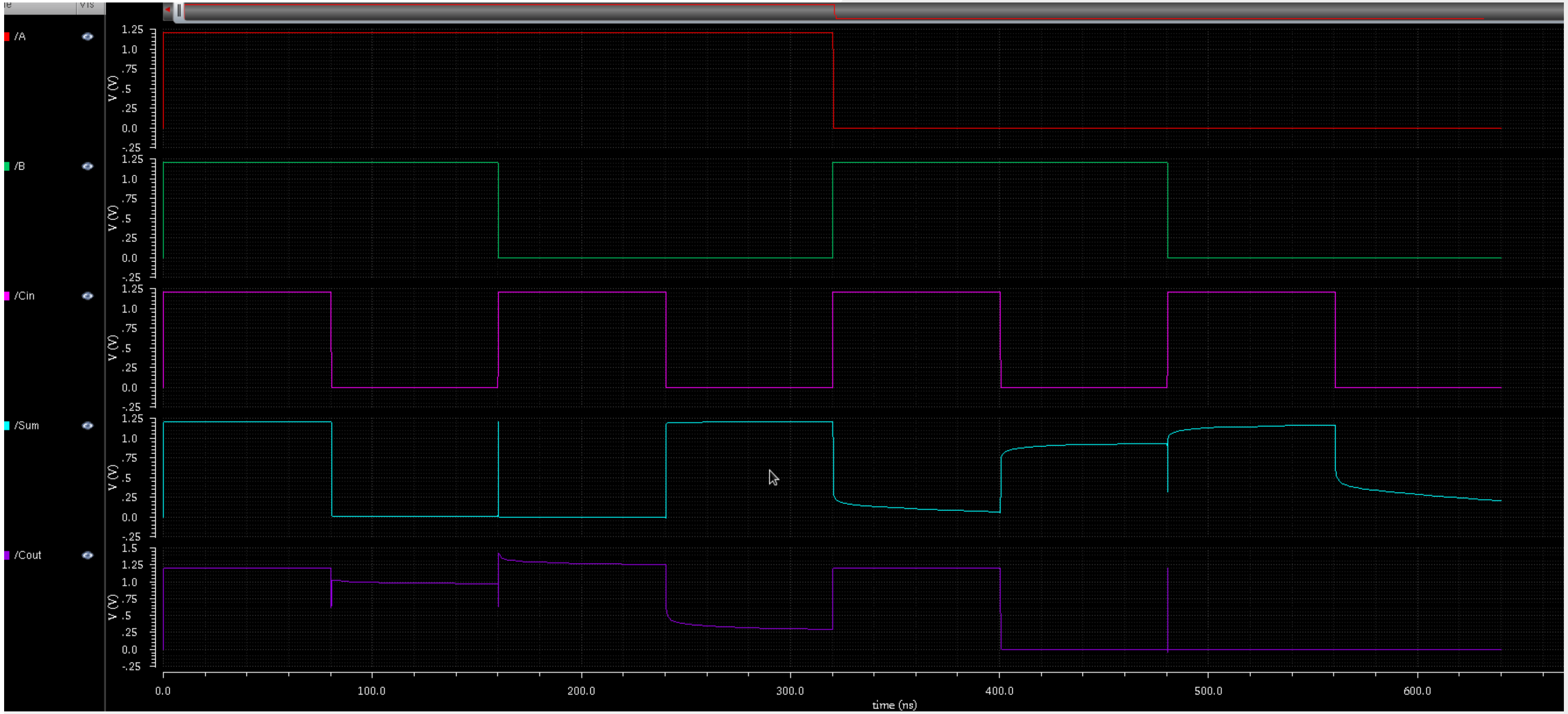
DIFFERENT TECHNIQUES OF FULL ADDER

- 9T Full Adder
- 10T Full Adder
- 14T Full Adder
- 16T Full Adder

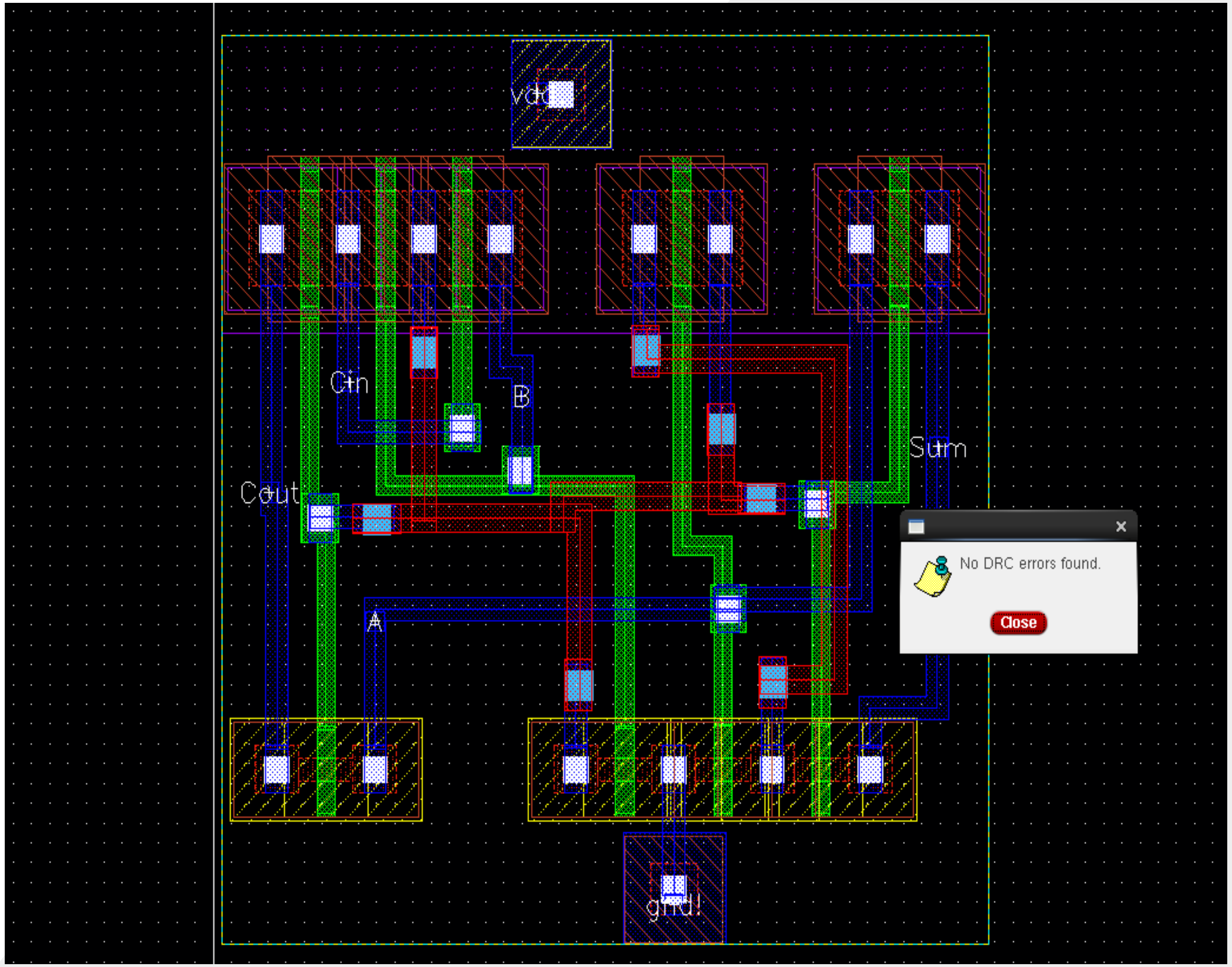
9T FULL ADDER



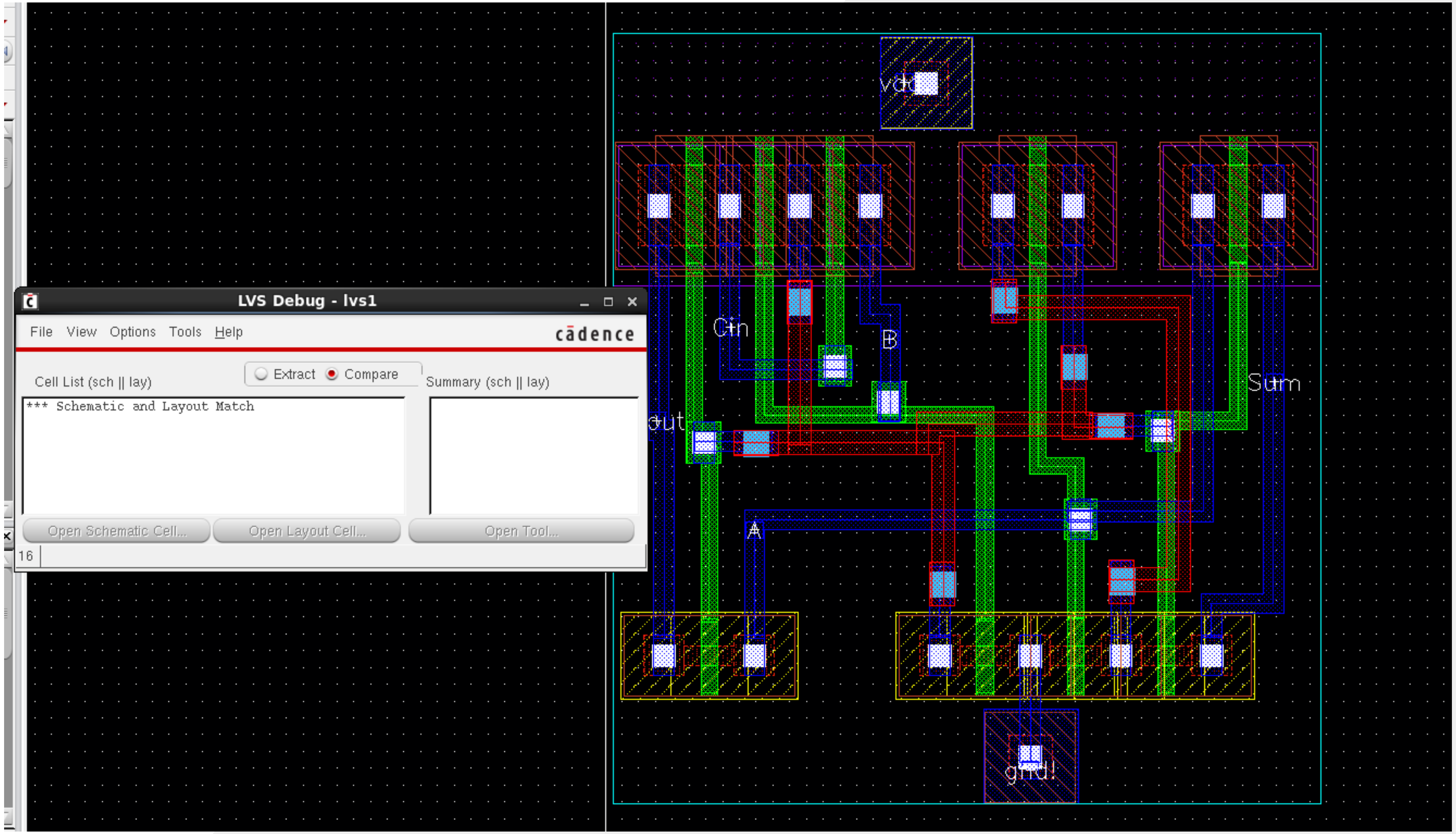
9T FULL ADDER



9T FULL ADDER



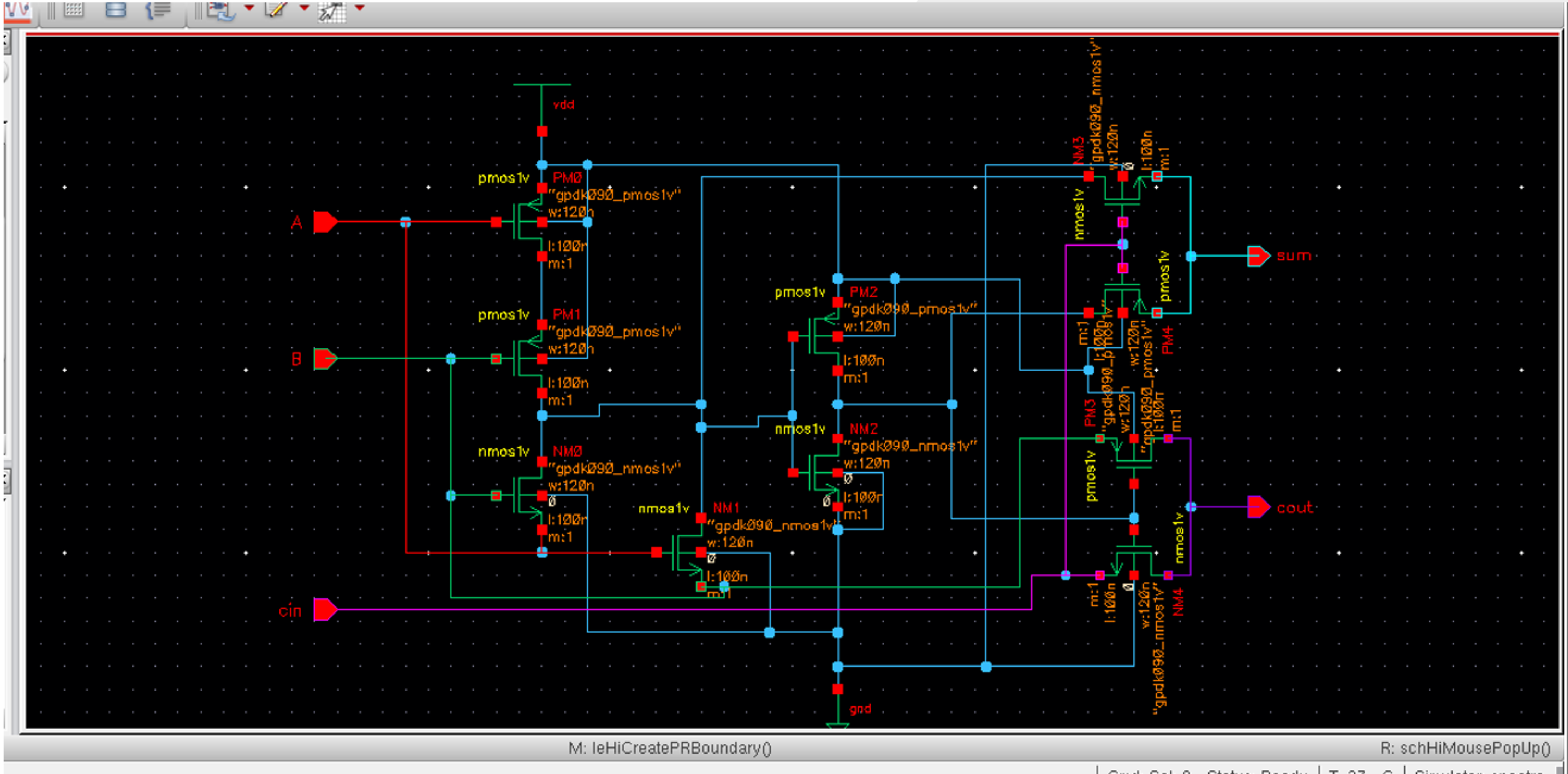
9T FULL ADDER



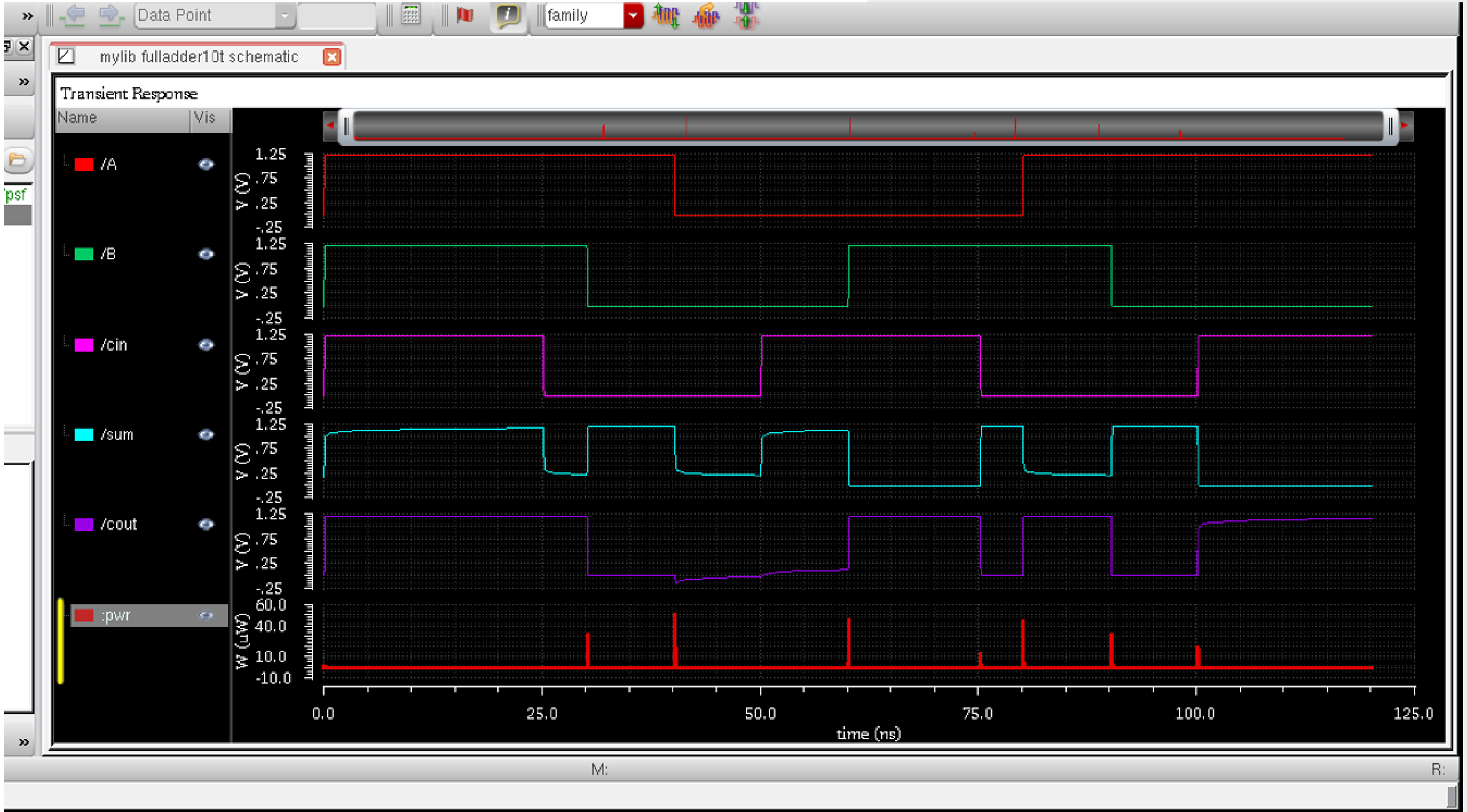
9T FULL ADDER

Method	Propagation delay(s)	Average Power(watt)	Power Delay Product	Cell Area (um)^2	No of Transistor	No. of DRC Error	No. of LVS Error
1	24.37E-12	31.17E-6	2.65E-20	17.87	9	No	No

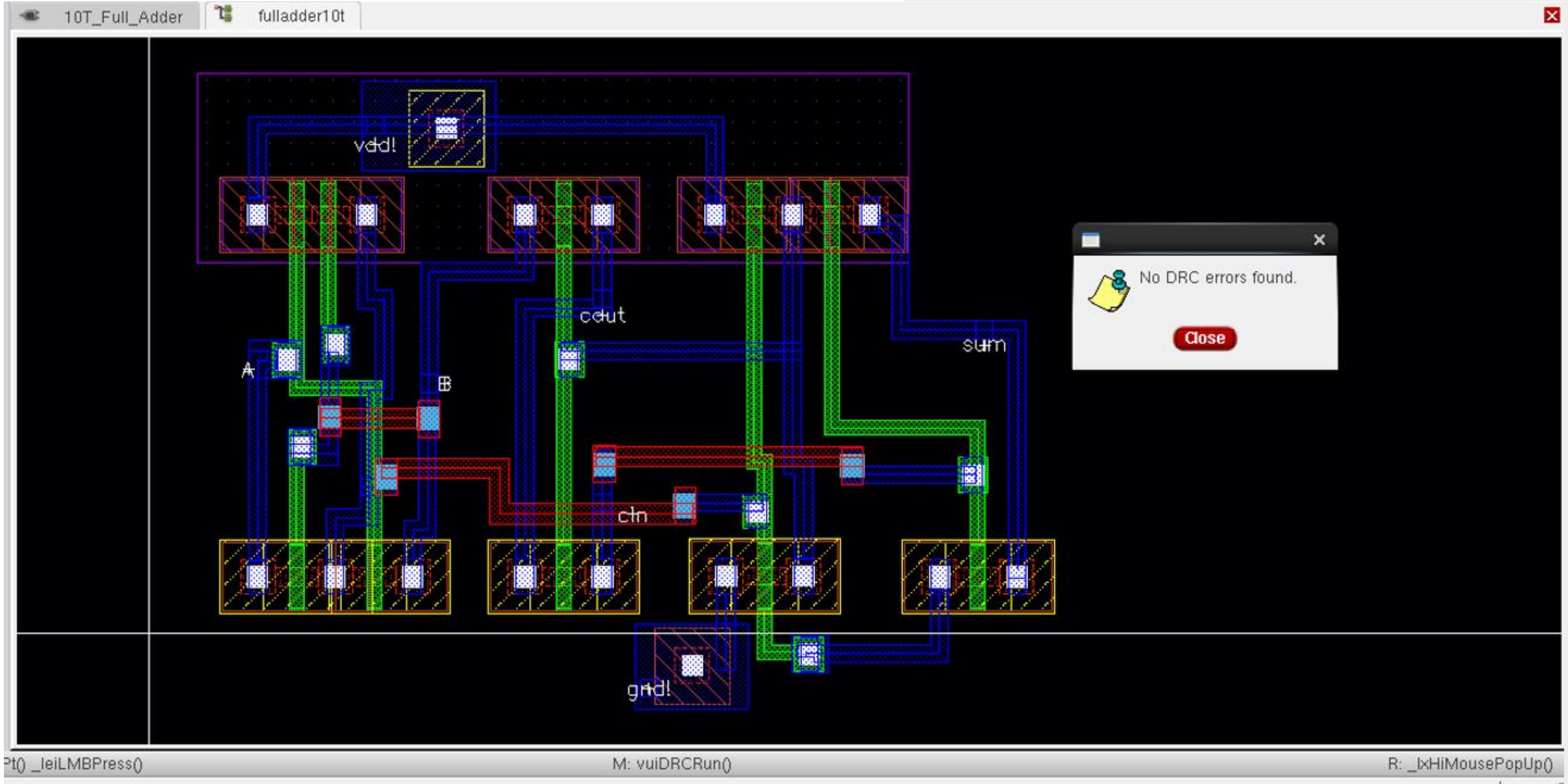
10T FULL ADDER



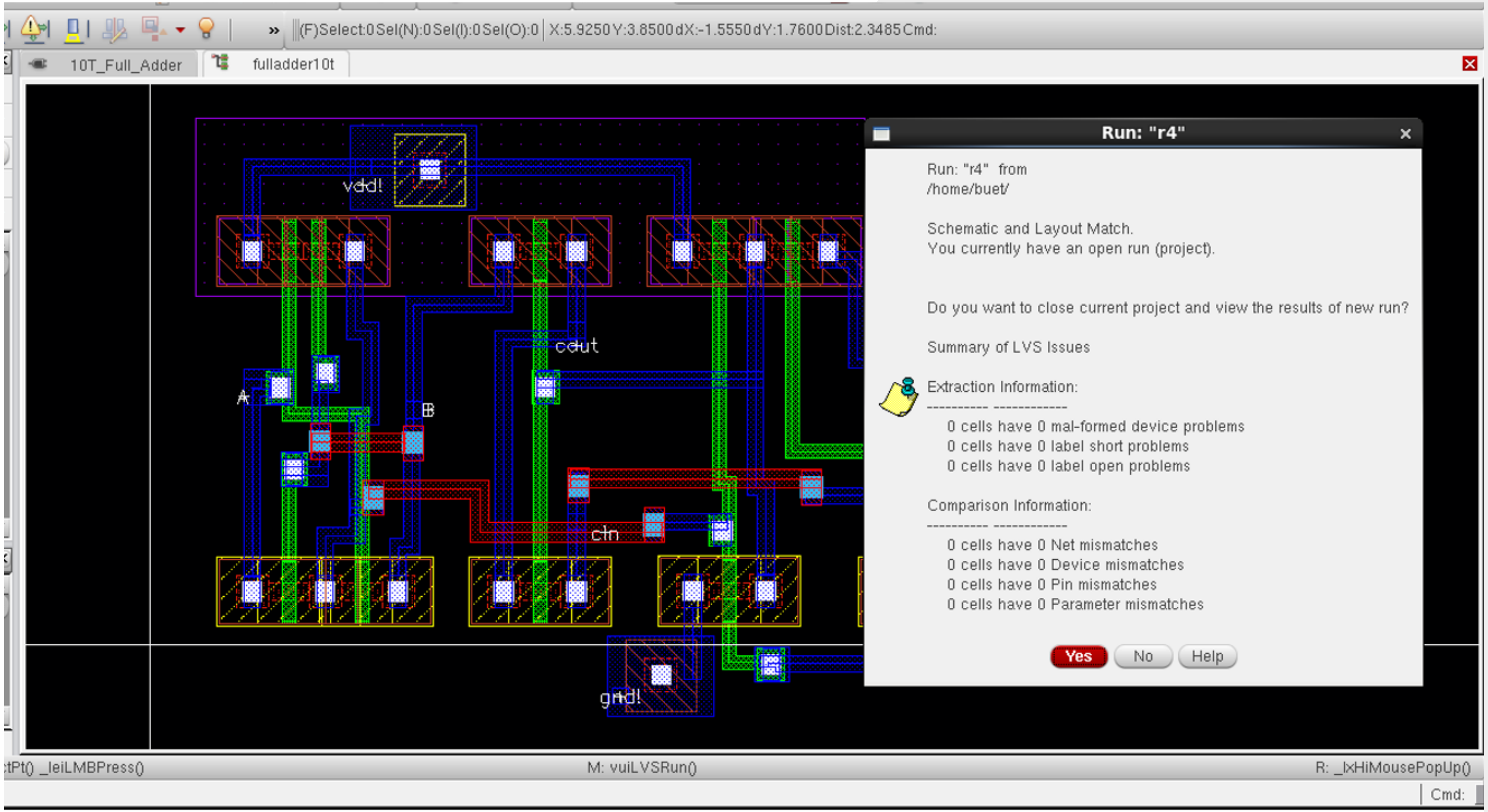
10T FULL ADDER



10T FULL ADDER



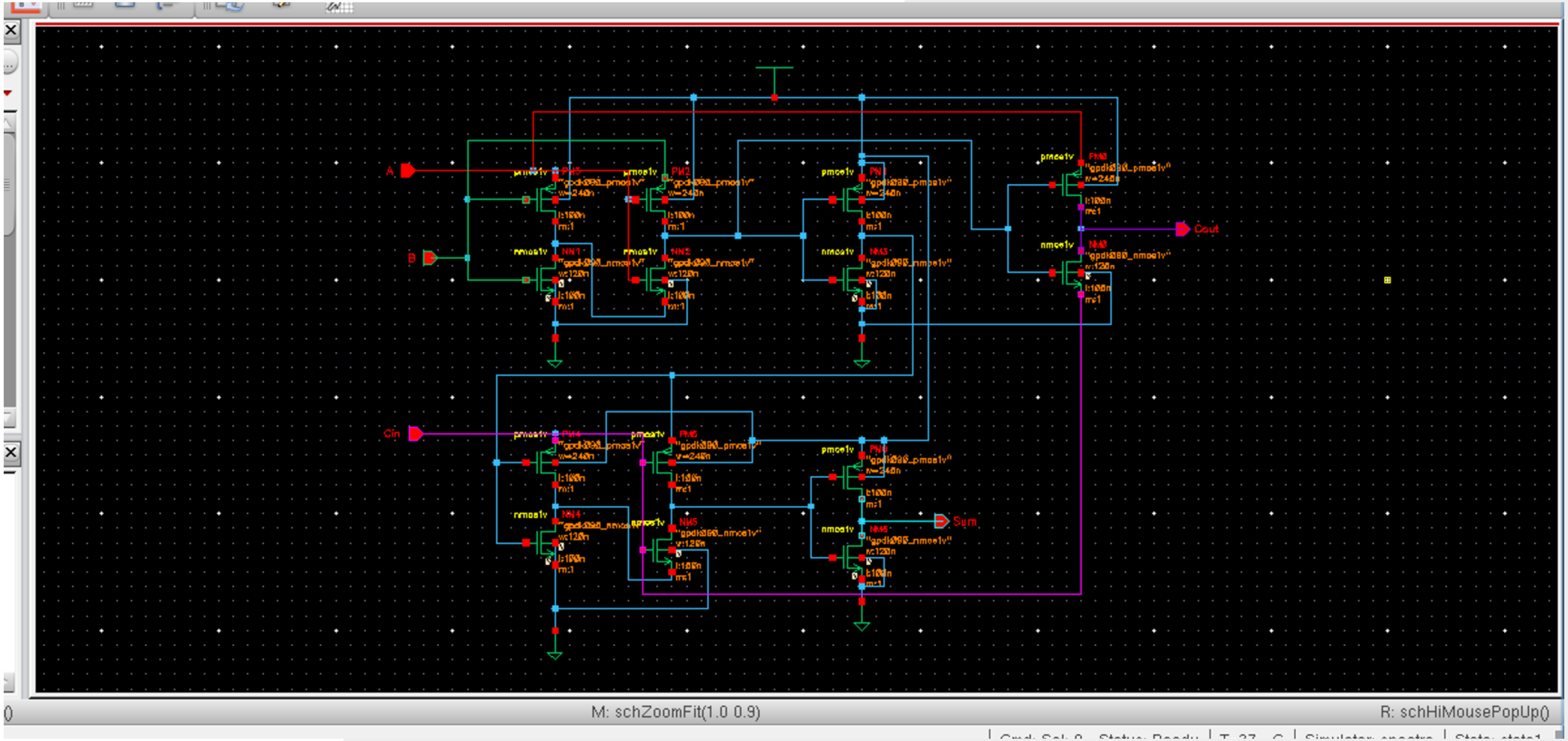
10T FULL ADDER



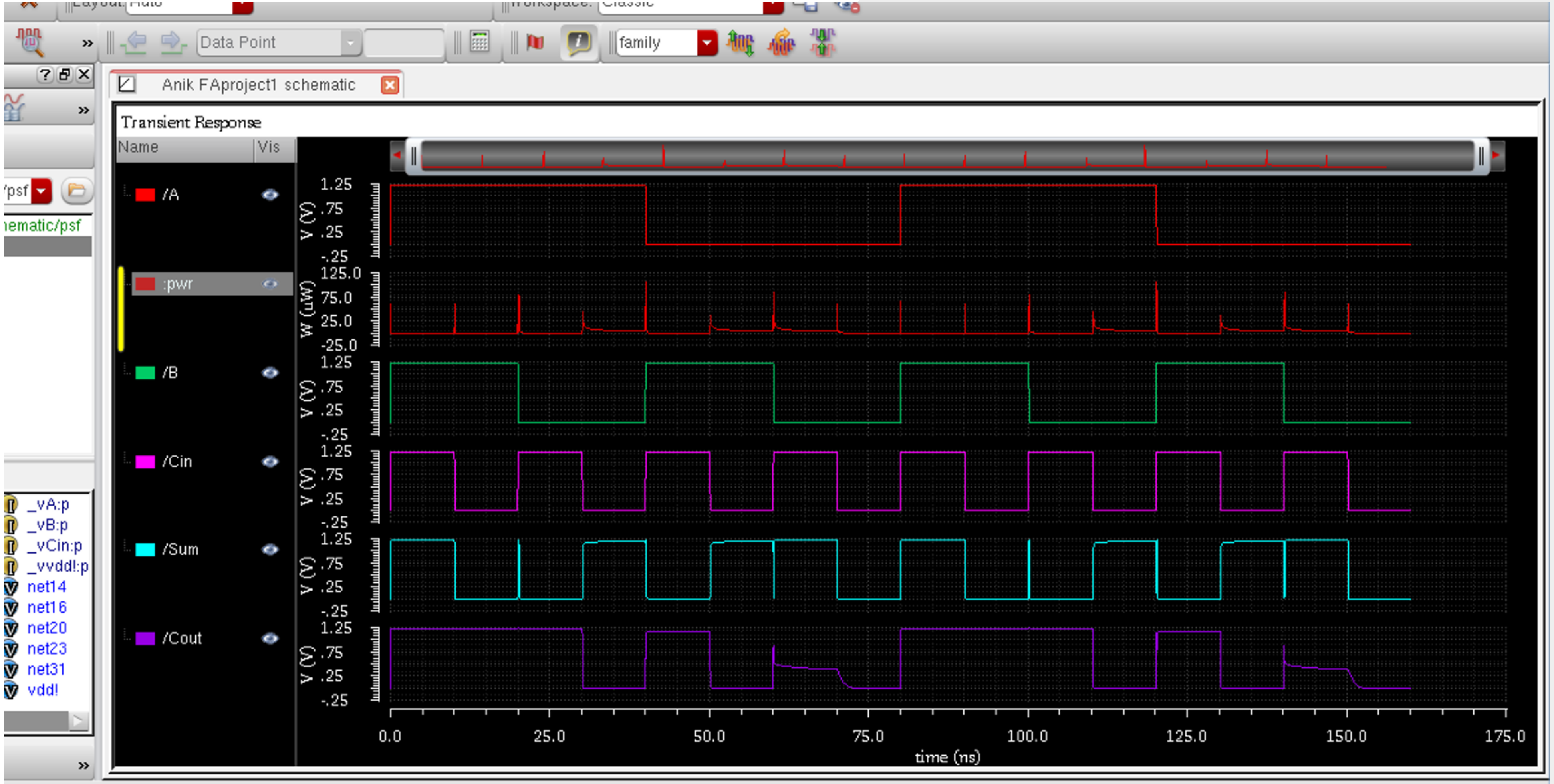
10T FULL ADDER

Method	Propagation delay(s)	Average Power(watt)	Power Delay Product	Cell Area (um)^2	No of Transisto r	No. of DRC Error	No. of LVS Error
2	52.63E-12	193.1E-6	1.140E-14	26.98	10	No	No

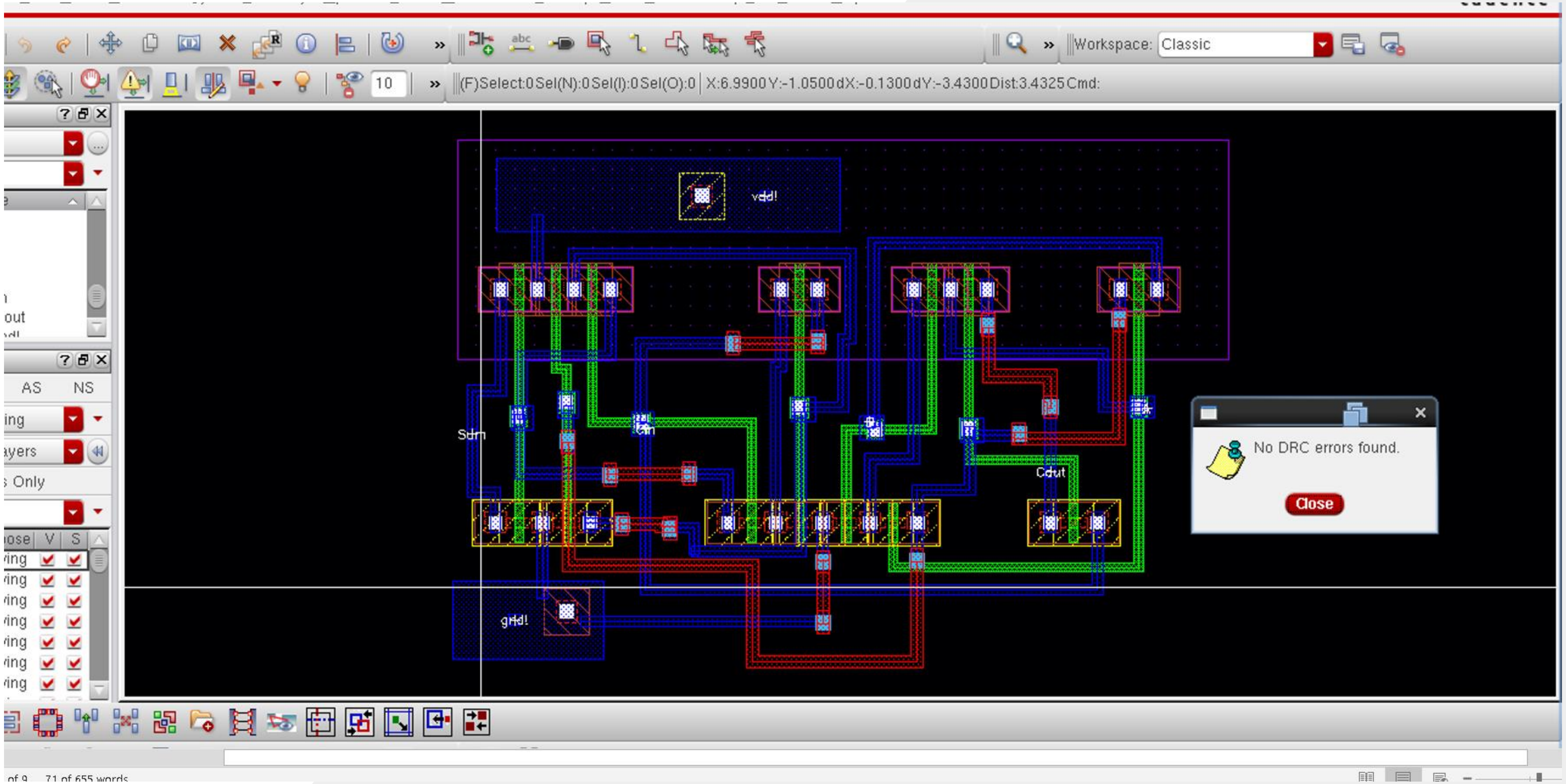
10T FULL ADDER



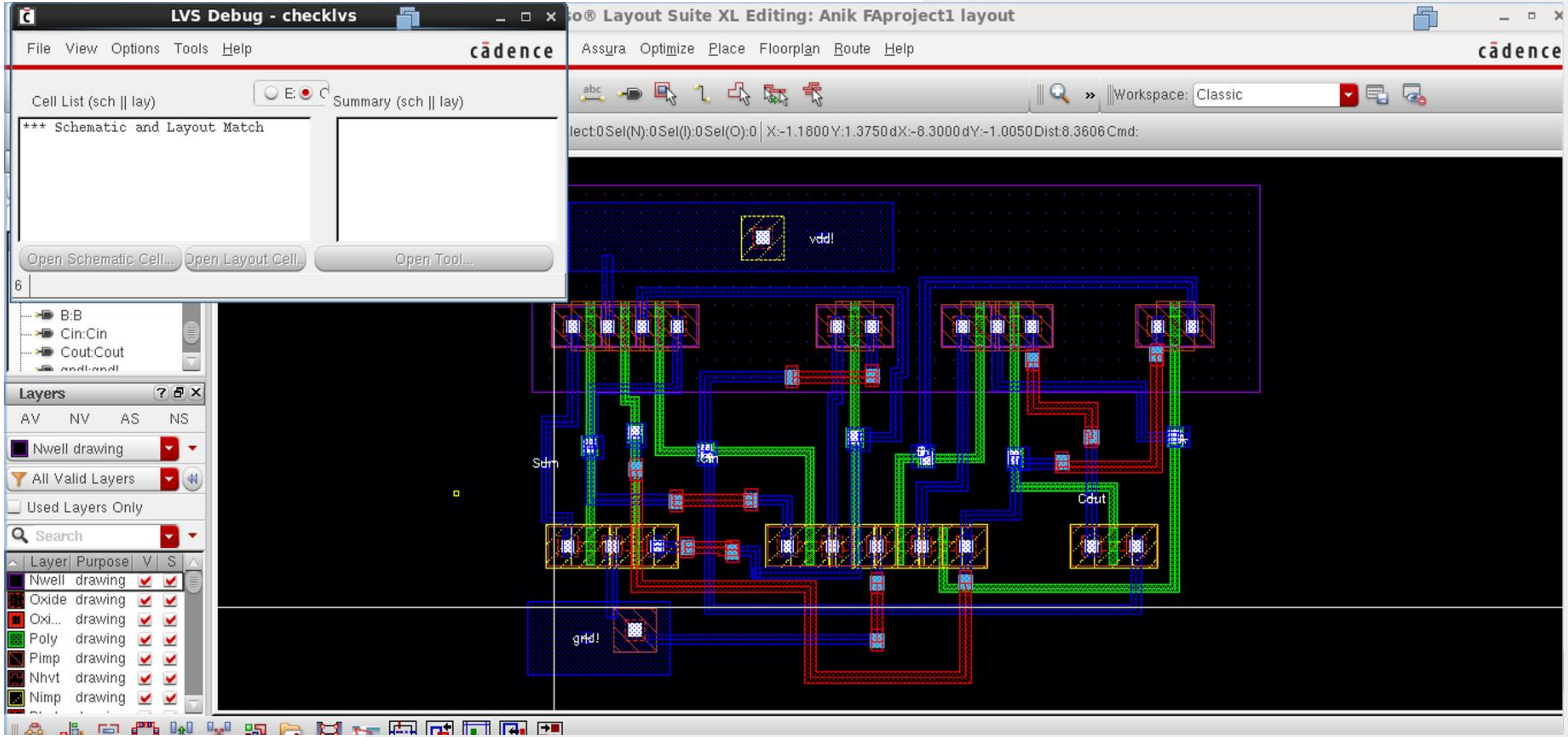
14T FULL ADDER



14T FULL ADDER



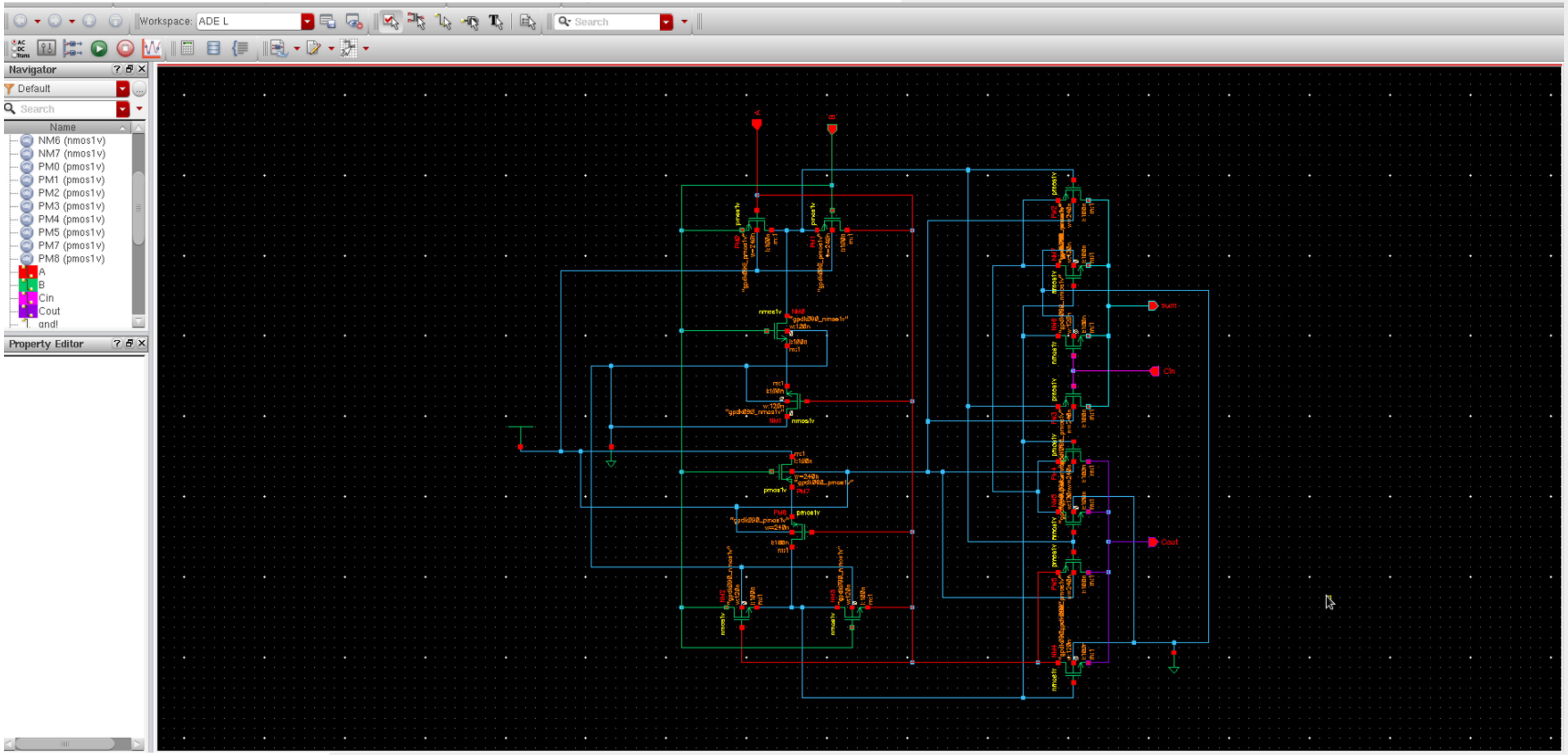
14T FULL ADDER



14T FULL ADDER

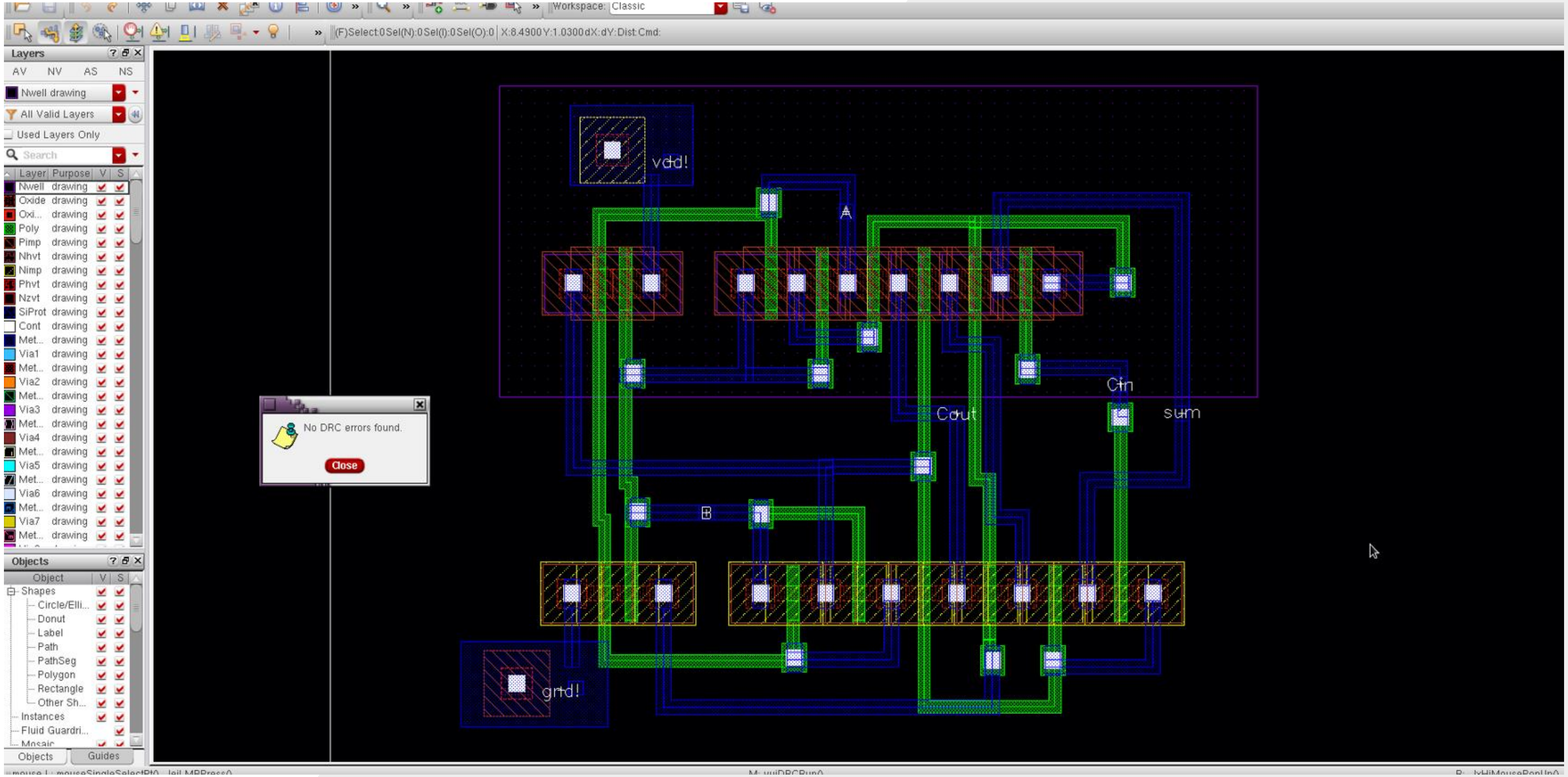
Method	Propagation delay(s)	Average Power(watt)	Power Delay Product	Cell Area (um)^2	No of Transistor	No. of DRC Error	No. of LVS Error
3	35.17E-12	3.241E-6	1.140E-16	53.05	14	No	No

16T FULL ADDER

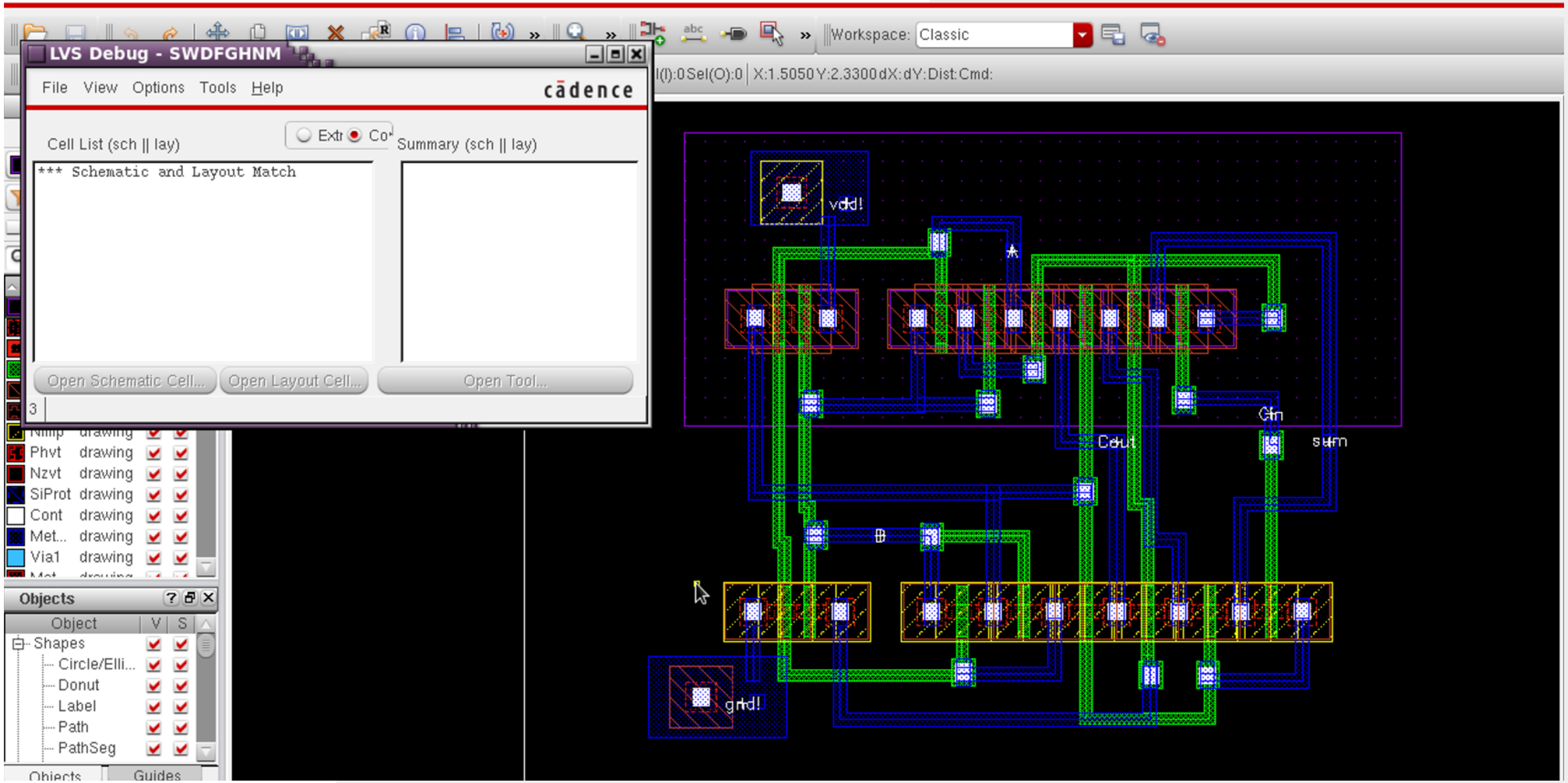


16T FULL ADDER

16T FULL ADDER



16T FULL ADDER



16T FULL ADDER

Method	Propagation delay(s)	Average Power(watt)	Power Delay Product	Cell Area (um)^2	No of Transistor	No. of DRC Error	No. of LVS Error
4	122.6E-12	0.5717E-6	3.96E-15	32.31	16	No	No

COMPARISON

Method	Propagation delay(s)	Average Power(watt)	Power Delay Product	Cell Area (um)^2	No of Transisto r	No. of DRC Error	No. of LVS Error
1	24.37E-12	31.17E-6	2.65E-20	17.87	9	No	No
2	52.63E-12	193.1E-6	1.140E-14	26.98	10	No	No
3	35.17E-12	3.241E-6	1.140E-16	53.05	14	No	No
4	122.6E-12	0.5717E-6	3.96E-15	32.31	16	No	No

MERITS AND DEMERITS

	Merits	Demerits
9T	• Low power and high-performance Full Adder • Power & Delay can be minimized by optimizing transistor size	• Loss threshold voltage in transistor. • It lacks driving
10T	• Requires less area compared to higher gate count • Lower Power Consumption and operating voltage.	• Very poor driving capacity. • Voltage drop occurs.
14T	• Delay decrease faster with the supply voltage.	• It has voltage Swing.
16T	• Low transistor count • Low surface area • Less power consumption	• High input impedance. • Very low driving capacity.

FUTURE ASPECTS

The future aspects of full adder circuits might include various advancements and improvements to their design structure and functionality. Some possible future developments in this area could involve the following:

Increased performance

- Reduction in power consumption
- Integration with other circuits
- Implementation in new technologies
- Development of new types of adders

CONCLUSION

To conclude, the above discussion all the variations and size shrinking of single bit full adders are done to improve the power consumption of the cell so that it can be better useful for convenient applications. The delay got decreased for some circuits and the speed of the full adder circuit is increased. As technology advances further, the arithmetic unit of the processor will also be capable of delivering faster results.

Thank You