PRANIL JOSHI

Webpage* ◇ pranil.j20@gmail.com ◇ pranil.joshi@iitb.ac.in

CAREER OBJECTIVE

My research interests lie in the areas of hardware design, computer architecture and relevant fields in EECS. I wish to work in the industry at the forefront of novel research that has a positive impact on people's lives.

EDUCATION

Bachelor of Technology | Indian Institute of Technology, Bombay *[Jul '16 - Present]*

Major degree in Electrical Engineering, complemented by a Minor degree in Computer Science and Engineering

Cumulative Performance Index : 9.58 / 10.0
Ranked 9th academically amongst a total of 140+ students in the program

RESEARCH EXPERIENCE

Secure Utility-based Cache-Partitioning Protocol *[Aug '19 - Present]*

Guide : Prof. Virendra Singh | Computer Architecture and Dependable Systems Lab, IIT-B

Considerable research has been devoted to prevention of cache-based side-channel attacks on cryptographic programs. We are exploring numerous ways to secure popular algorithms with minimal impact to performance.

- Explored procedures of security breaches in modern hardware and state-of-the-art solutions for them
- Implementing new techniques to prevent potent cache-based attacks, in particular on the Utility-based Cache-partitioning protocol, which leaves the cache vulnerable at the time of cache-line reallocation

Knowledge-sharing between cross-domain machine-learning agents *[May '19 - Jul '19]*

Tech Research Intern | Adobe Research Lab, India

Leveraging the knowledge gained by pre-trained existing black-box models has not been explored in prior work. We demonstrated the use case of training conversational agents in similar domains as proof of concept.

- Used a generalizable workflow to leveraged knowledge of a **black-box knowledge-source** trained in one domain to generate 'noisy' training data in the second (target) domain to train a new model
- Trained a chatbot for **intent-identification** and **slot-filling** in a data-scarce setting by consulting a source agent from a different domain, and showed improved performance in natural language understanding
- Utilized **noise-robust** architectures and loss functions to learn from noisy annotations with Keras library
- Proposed a new **Dynamic Sample Re-weighting Algorithm** to model degree of noise in training samples, based on how each sample in a training batch affects the loss over a fixed validation set

*This project has resulted in a **paper** (currently under review for **ACL 2020**) and a **patent** filed through USPTO.*

Performance assessment of TDMA networks *[May '18 - Jul '18]*

Visiting Scholar at the Ohio State University | Guide: Prof. Ness Shroff, ECE Department

This work studied the characteristics of individual queues in a practical TDMA system when using various scheduling policies. It employed EMANE, an emulator developed by the US Naval Research Department.

- Studied the performance of a one-hop TDMA network configuration by modifying critical parameters like the data rate, slot duration and number of slots in the schedule, and the pathloss on every link
- Tested the **Maximum-Weight Scheduling Algorithm** and actualized its expected benefits of higher throughput, lower delay and lower average buffer occupancy against traditional first-in-first-out schedules

KEY PROJECTS

Digitally Programmable Analog Computer *[Jan '19 - May '19]*

Guide : Prof. Mukul Chandorkar | Electrical Engineering Department, IIT-B

Analog methods of solving multi-state differential systems are extremely fast. Unlike digital systems, however, they are inaccurate, noisy and lack mathematical flexibility. A hybrid solution presents the best of both worlds.

- Implemented a hybrid system to solve non-linear differential equations in up to eight state variables
- Designed an **analog module** using integrator blocks for fast computations over a wide frequency range
- Interfaced it with a **digital module** consisting of a fast microcontroller to compute non-linear expressions

*I recommend viewing my latest CV on my webpage at https://pranilj.github.io/

IITB-Proc Processor Design

Guide : Prof. Virendra Singh | Electrical Engineering Department, IIT-B

As a way to directly apply our theoretical knowledge, we implemented and tested successively more advanced general-purpose processor designs having an instruction set architecture with 16 diverse instructions using VHDL.

- **Pipelined RISC Processor Implementation** : *[Oct '18 - Nov '18]*
  Employed sophisticated branch prediction, hazard mitigation and operand forwarding techniques to design a 6-stage execution pipeline and synthesized it on an Altera DE0 Nano FPGA operating at 60MHz
- **Superscalar Processor Implementation** : *[Mar '19 - Apr '19]*
  Designed an out-of-order execution engine consisting of specialized pipelines assisted by a reservation station, a re-order buffer, register renaming and branch prediction to extract instruction-level parallelism

Automatic Disease Detection in Plants *[Feb '19 - Mar '19]*

Guide : Prof. V. M. Gadre | Electrical Engineering Department, IIT-B

We employed state-of-the-art image processing and deep learning techniques to diagnose plant diseases having visible symptoms, and demonstrated the algorithm for avoiding epidemics in the specific use case of jute plants.

- Performed **de-noising** followed by **hue-based segmentation** of an image of jute plant stem to extract thirteen features that can be used as input to a classifier model to identify four varieties of crop diseases
- Presented to an audience of 150+ at the **'Make In India' Workshop** under the 'Knowledge Incubation Initiative' conceptualized by the Ministry of Human Resource Development of the Government of India

SCHOLASTIC ACHIEVEMENTS

- Secured **All India Rank 296** in JEE (Advanced) examination amongst 1.5 lakh aspiring candidates *[2016]*
- Achieved **All India Rank 233** in JEE (Mains) examination amongst 12 lakh aspiring candidates *[2016]*
- Secured **Maharashtra State Rank 38** in MHT Common Entrance Test amongst 4 lakh candidates *[2016]*
- Awarded a prestigious medal for excellence in the **Homi Bhabha Young Scientist Examination** *[2013]*
- Received the distinguished **High School Scholarship** conferred by the state of Maharashtra *[2011]*

COURSES UNDERTAKEN

Electrical Engineering	:	Advanced Computer Architecture, Algorithmic Digital Design, Processor Design, Digital Signal Processing, Communication, Control systems, Power Electronics, Analog and Digital Systems and accompanying laboratory courses
Computer Science	:	Machine Learning, Data Structures and Algorithms, Digital Image Processing, Computer Networks, Computer and Network Security, Operating Systems
Mathematics, Statistics	:	Probability and Random Processes, Differential Equations, Complex Analysis

TECHNICAL SKILLS

Programming Languages	:	Python (with TensorFlow, Keras), C++, Embedded C, VHDL, Assembly, LaTeX
Software and Tools	:	MATLAB, Quartus, Vivado, Gem5, Sniper, Keil, NGSpice, AutoCAD, SolidWorks

POSITIONS OF RESPONSIBILITY

Editor | Insight, IIT-B *[Apr '18 - Mar '19]*

Insight, IIT Bombay's student media body, regularly releases articles and videos centered around student issues

- Spearheaded the **Summer Internship Blog 2018**, publishing testimonials written by 25 student interns
- Published a detailed review of the provisions for **fire safety** in the institute, aimed at raising awareness
- Authored an editorial piece about an alleged case of **student misconduct** in the institute, that had a reach of **11k+** readers and enabled the students' concerns and suggestions to reach the administration

Institute Student Mentor, Department Academic Mentor | SMP, IIT-B *[Apr '18 - Mar '19]*

Student Mentorship Program was initiated by IIT-B to appoint model students to act as role models for juniors

- One of only **11** mentors in their third year, selected via a rigorous process of interviews and peer reviews
- Personally guided **6** sophomores and **12** freshmen to excel in **academic and co-curricular** endeavours