PRANIL JOSHI

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My research interests lie in the areas of hardware design and computer architecture, and I would love to explore the application of these disciplines in related fields of Electrical and Computer Engineering. I wish to eventually work in the industry at the forefront of cutting-edge research that has a positive impact on people's lives.

EDUCATION

Bachelor of Technology | Indian Institute of Technology, Bombay *[Jul '16 - Present]*

Major degree in Electrical Engineering, complemented by a Minor degree in Computer Science and Engineering

Cumulative Performance Index : 9.58 / 10.0
Ranked 9th academically amongst a total of 140+ students in the program

RESEARCH EXPERIENCE

Secure Utility-based Cache-Partitioning Protocol *[Aug '19 - Present]*

Guide : Prof. Virendra Singh | Computer Architecture and Dependable Systems Lab, IIT-B

Along with performance improvement, hardware security has increasingly come into the spotlight of research. Considerable research has been devoted to prevention of cache-based side-channel attacks on cryptographic programs. We are exploring numerous ways to secure popular algorithms with minimal impact to performance.

- Exploring procedures of security breaches in modern hardware and state-of-the-art solutions for them
- Proposing techniques to prevent potent cache-based attacks, in particular on the renowned Utility-based Cache-partitioning protocol, which leaves the cache vulnerable at the time of cache-line reallocation

Knowledge-sharing between cross-domain machine-learning agents *[May '19 - Jul '19]*

Tech Research Intern | Adobe Research Lab, India

Since training deep-learning models is a long, computationally expensive process, it is wise to extract the knowledge gained by pre-trained models. Learning from existing black-box models has not been explored in prior work. We demonstrate the use case of conversational agents in different domains as proof of concept.

- Used a generalizable workflow to leveraged knowledge of a **black-box knowledge-source** trained in one domain to generate 'noisy' training data in the second (target) domain to train a new model
- Trained a chatbot for **intent-identification** and **slot-filling** in a data-scarce setting by consulting a source agent from a different domain, showing improved performance in natural language understanding
- Utilized **noise-robust** architectures and loss functions to learn from noisy annotations with Keras library
- Proposed a new **Dynamic Sample Re-weighting Algorithm** to model degree of noise in training samples, based on how each sample in a training batch affects the loss over a fixed validation set

Performance assessment of TDMA networks *[May '18 - Jul '18]*

Visiting Scholar at the Ohio State University | Guide: Prof. Ness Shroff, ECE Department

This work studied the characteristics of individual queues in a practical TDMA system when using various scheduling policies. It employed EMANE, an emulator developed by the US Naval Research Department.

- Studied the performance of a one-hop TDMA network configuration by modifying critical parameters like the data rate, slot duration and number of slots in the schedule, and the pathloss on every link
- Tested the **Maximum-Weight Scheduling Algorithm** and actualized its expected benefits of higher throughput, lower delay and lower average buffer occupancy against traditional first-in-first-out schedules

KEY PROJECTS

Digitally Programmable Analog Computer *[Jan '19 - May '19]*

Guide : Prof. Mukul Chandorkar | Electrical Engineering Department, IIT-B

Numerous engineering problems can be modelled as a non-linear multi-state differential system. Analog methods of solving them are extremely fast. Unlike digital systems, however, they are inaccurate, susceptible to noise and lack mathematical flexibility to express non-linearities. A hybrid computer presents the best of both worlds.

- Implemented a hybrid system to solve non-linear differential equations in up to eight state variables
- Designed an **analog module** using integrator blocks for fast computations over a wide frequency range
- Interfaced it with a **digital module** consisting of a fast microcontroller to compute non-linear expressions
- Implemented on a stand-alone two-layer printed circuit board (**PCB**) with on-board power management

IITB-Proc Processor Design

Guide : Prof. Virendra Singh | Electrical Engineering Department, IIT-B

As a way to directly apply our theoretical knowledge, we implemented successively more advanced general-purpose processor designs having an instruction set architecture with 16 diverse instructions using VHDL.

- **Pipelined RISC Processor Implementation** : *[Oct '18 - Nov '18]*
  Employed sophisticated branch prediction, hazard mitigation and operand forwarding techniques to design a 6-stage execution pipeline and synthesized it on an Altera DE0 Nano FPGA operating at 60MHz
- **Superscalar Processor Implementation** : *[Mar '19 - Apr '19]*
  Designed an out-of-order execution engine consisting of specialized pipelines assisted by a reservation station, a re-order buffer, register renaming and branch prediction to extract instruction-level parallelism

Automatic Disease Detection in Plants *[Feb '19 - Mar '19]*

Guide : Prof. V. M. Gadre | Electrical Engineering Department, IIT-B

We employ state-of-the-art image processing and deep learning to diagnose plant diseases having visible symptoms, and we demonstrate the algorithm for the use-case of jute plants. The end goal is to develop a smartphone application to enable farmers to take timely action and thereby prevent agricultural epidemics.

- Performed **de-noising** followed by **hue-based segmentation** on an image of jute plant stem to extract thirteen features that can be used as input to a classifier model to identify four varieties of crop diseases
- Presented to an audience of 150+ at the **'Make In India' Workshop** under the 'Knowledge Incubation Initiative' conceptualized by the Ministry of Human Resource Development of the Government of India

Hardware Accelerator for Graphics Computation *[Aug '19 - Sep '19]*

Guide : Prof. M. P. Desai | Electrical Engineering Department, IIT-B

The goal of this project was to design an accelerator by maximizing performance as well as hardware utilization.

- Implemented a highly optimized pipelined digital system that can convolve an image with a kernel
- Parallelized the design to employ multiple engines that can resolve contentious memory accesses via independent pipes so as to minimize the computational time and utilize the entire memory bandwidth

Semiconductor Device Parameter Extraction *[Dec '17 - Jan '18]*

Guide : Prof. M. B. Patil | Electrical Engineering Department, IIT-B

We explored the use of accurate and consistent methods to extract device parameters for circuit modeling.

- Studied how tuning the SPICE parameters of a bipolar junction transistor affects its device characteristics
- Developed an generalizable iterative method based on **Particle Swarm Optimization** to determine model parameters of a device like the BJT from its device characteristics accurately in a short convergence time

Laser Hockey *[May '17 - Jun '17]*

A revamped version of the Air Hockey using a hockey puck made from diffused laser, this game was a project made as part of Institute Technical Summer Project program, organized by Institute Technical Council of IIT-B.

- Designed and built laser-triggered hand mallets using SolidWorks controlled by a central **Arduino Uno**
- Used light-dependent resistors (**LDRs**), **photodiodes** and **motion sensors** to control motion of puck

SCHOLASTIC ACHIEVEMENTS

- Ranked **7th** academically in the Electrical Engineering Program amongst a total of 79 students *[2019]*
- Secured **All India Rank 296** in JEE (Advanced) examination amongst 1.5 lakh aspiring candidates *[2016]*
- Achieved **All India Rank 233** in JEE (Mains) examination amongst 12 lakh aspiring candidates *[2016]*
- Secured **Maharashtra State Rank 38** in MHT Common Entrance Test amongst 4 lakh candidates *[2016]*
- Awarded a prestigious medal for excellence in the **Homi Bhabha Young Scientist Examination** *[2013]*
- Achieved **Maharashtra State Rank 10** in Unified International English Olympiad *[2013]*
- Secured **Maharashtra State Rank 14** in the prestigious High School Scholarship Examination *[2011]*

COURSES UNDERTAKEN

Electrical Engineering : Advanced Computer Architecture, Algorithmic Digital Design, Processor Design, Digital Signal Processing, Communication, Control systems, Power Electronics, Analog and Digital Systems and accompanying laboratory courses

Computer Science : Machine Learning, Data Structures and Algorithms, Digital Image Processing, Computer Networks, Computer and Network Security, Operating Systems

Mathematics, Statistics : Probability and Random Processes, Differential Equations, Complex Analysis

TECHNICAL SKILLS

Programming Languages : Python (with TensorFlow, Keras), C++, Embedded C, VHDL, Assembly, LaTeX

Software and Tools : MATLAB, Quartus, Vivado, Gem5, Sniper, Keil, NGSpice, AutoCAD, SolidWorks

POSITIONS OF RESPONSIBILITY

Editor | Insight, IIT-B *[Apr '18 - Mar '19]*

Insight, IIT Bombay's student media body, regularly releases articles and videos centered around student issues

- Spearheaded the **Summer Internship Blog 2018**, publishing testimonials written by 25 student interns
- Published a detailed review of the provisions for **fire safety** in the institute, aimed at raising awareness
- Authored an editorial piece about an alleged case of **student misconduct** in the institute, that had a reach of **11k+** readers and enabled the students' concerns and suggestions to reach the administration

Institute Student Mentor, Department Academic Mentor | SMP, IIT-B *[Apr '18 - Mar '19]*

Student Mentorship Program was initiated by IIT-B to appoint model students to act as role models for juniors

- One of only **11** mentors in their third year, selected via a rigorous process of interviews and peer reviews
- Personally guided **6** sophomores and **12** freshmen to excel in **academic and co-curricular** endeavours

Cultural and Events Coordinator | Mood Indigo, IIT-B *[Jun '17 - Dec '17]*

Mood Indigo is Asia's largest college cultural festival with a footfall of 141000+ people and over 210 events

- Ideated, structured and executed 'Eloquence', the highly acclaimed **Literature Festival** of Mood Indigo
- Led a team of **15+** organizers to host renowned artists and celebrities and to execute **6** flagship events

EXTRACURRICULAR ACTIVITIES

Volunteer | National Service Scheme of India *[Jul '16 - Mar '17]*

NSS is a 3.8 million strong body that aims to bring about positive social change through numerous initiatives

- Worked in the '**Vikas**' department, to explore new avenues of promoting **sustainable social development**
- Was a founding member and active contributor of **'Tarang': the Sustainability Club** of IIT Bombay
- Presented a lecture on '**Best From Waste**' for an audience of inquisitive kids in the NGO 'Aasha'