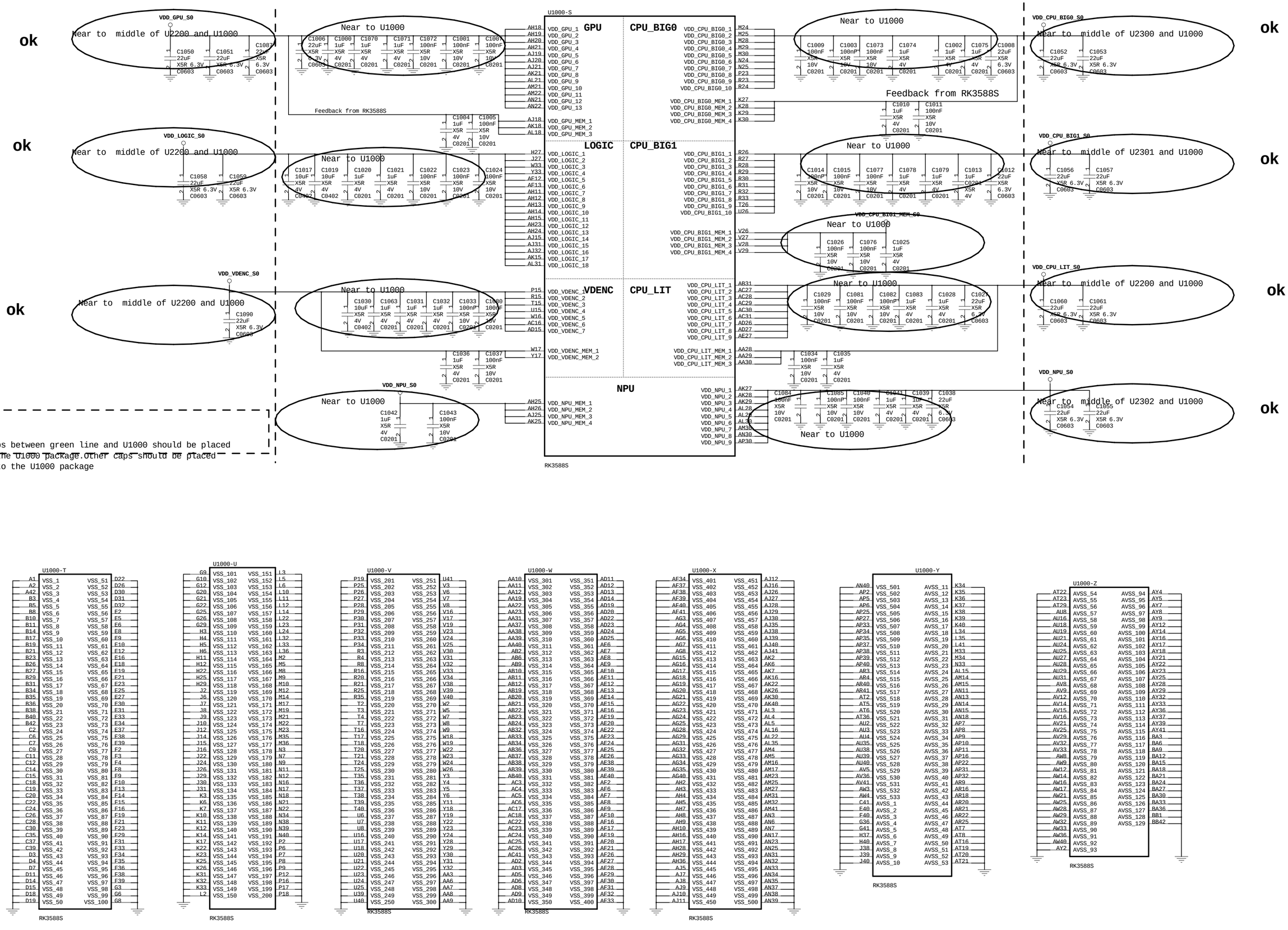
RK3588S(Power&Gnd)



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Designed by:	Joseph
Reviewed by:	<Checker>
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RK3588S(OSC/PLL/PMUIO1)

ok

Note:

Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the ~~crystal that is recommended by~~ the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:

The Caps between green line and U1000 should be ~~placed under the U1000 package.Other caps should~~ be placed close to the U1000 package

U1000-E RK3588S

OSC

R1100 22R 5% R0402 — XOUT — T42 — XOUT_24M

Y1100 24MHz (X1, GND, X2, GND) CRY4_3R20X2R50X0R80
C1111 15pF C0G 50V C0402
R1102 510K 1% R0402
XIN — T41 — XIN_24M
C1112 15pF C0G 50V C0402

VCCA_1V8_S0
C1100 100nF X5R 10V C0201
N35 — OSC_1V8_1
N36 — OSC_1V8_2

PLL

VDDA_0V75_S0
C1113 1uF C0402 X5R 6.3V
C1103 100nF X5R 10V C0201
Y26 — PLL_DVDD0V75

VCCA_1V8_S0
C1114 1uF C0402 X5R 6.3V
C1104 100nF X5R 10V C0201
AB25 — PLL_AVDD1V8

AA26 — PLL_AVSS

PMUIO1 Domain
Operating Voltage=1.8V Only

NPOR — V42
C1110 100nF X5R 10V C0201
RESET_L
RESET_L
TSADC_SHUT
R1104 0R 5% R0402
TVSS — V41

		REFCLK_OUT	/ GPIO0_A0_D	W38	WIFI_WAKE_HOST_H
	TSADC_SHUT_ORG /	TSADC_SHUT_M0	/ GPIO0_A1_Z	AC39	TSADC_SHUT
		PMIC_SLEEP1	/ GPIO0_A2_D	W41	SLEEP1_RESET1_DEVOFF1_VSEL1
		PMIC_SLEEP2	/ GPIO0_A3_D	AD39	VSEL2
		SDMMC_DET	/ GPIO0_A4_U	AC38	SDMMC_DET_L
	PMU_DEBUG / SDMMC_PWREN /	SPI2_CLK_M2	/ GPIO0_A5_D	Y39	SPI2_CLK_M2 R1115 22R 5% R0402 — PMIC_SPI_CLK
	I2C0_SDA_M0 /	SPI2_MOSI_M2	/ GPIO0_A6_Z	W39	SPI2_MOSI_M2 R1116 22R 5% R0402 — PMIC_SPI_MOSI
		PMIC_INT_L	/ GPIO0_A7_U	W42	PMIC_INT_L
	UART0_RX_M1 / I2C1_SCL_M1 /	SPI2_CS1_M2	/ GPIO0_B0_Z	AC37	RTC_INT_L
PWM5_M0 /	UART0_TX_M1 / I2C1_SDA_M1 /	SPI2_CS0_M2	/ GPIO0_B1_Z	W40	PMIC_SPI_CS
	CLK32K_OUT0	CLK32K_IN	/ GPIO0_B2_U	AD38	RTC_32K_IN
	I2C0_SCL_M0 /	SPI2_MISO_M2	/ GPIO0_B3_Z	Y38	

VCC1V8_PMU_DDR_S3
PMUIO1_1V8_1 — N37
PMUIO1_1V8_2 — R36
C1101 100nF X5R 10V C0201

PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V

VDD_0V75_S3
PMU_0V75_1 — AJ36
PMU_0V75_2 — AJ37
C1105 100nF X5R 10V C0201
C1125 1uF X5R 4V C0201

U1000-F RK3588S

RK3588S(PMUIO2)

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

	/ PCIE20X1_1_CLKREQN_M0	/ I2S1_MCLK_M1	/ I2C1_SCL_M0	/	/ UART2_TX_M0	/ JTAG_TCK_M2	/ GPIO0_B5_D	AH39 — UART2_TX_M0
	/ PCIE20X1_1_WAKEN_M0 /	/ I2S1_SCLK_M1	/ I2C1_SDA_M0	/	/ UART2_RX_M0	/ JTAG_TMS_M2	/ GPIO0_B6_D	AH40 — UART2_RX_M0
	/ PCIE20X1_1_PERSTN_M0 /	SPI0_CS1_M0 / I2S1_LRCK_M1	/ I2C2_SCL_M0	/	/ CAN0_TX_M0	/ PWM0_M0	/ GPIO0_B7_D	AK39 — I2C2_SCL_M0
	/	/ SPI0_MOSI_M0 /	/ I2C2_SDA_M0	/ PDM0_CLK0_M1	/ CAN0_RX_M0	/ PWM1_M0	/ GPIO0_C0_D	AM40 — I2C2_SDA_M0
	/	/	/	/	/	/ PMIC_SLEEP3	/ GPIO0_C1_D	AM38 — VSEL3
	/	/	/	/	/	/ PMIC_SLEEP4	/ GPIO0_C2_D	AG36 — VSEL4
	/	/	/	/	/	/ PMIC_SLEEP5	/ GPIO0_C3_D	AH38 — VSEL5
DP0_HPDIN_M1 /	/	/	/ I2C4_SDA_M2	/ PDM0_CLK1_M1	/ UART0_RX_M0	/ PWM2_M0	/ GPIO0_C4_D	AL38 — CC_INT0_L
	/	/	/ I2S1_SDI0_M1	/ I2C4_SCL_M2 / PWM4_M0	/ UART0_TX_M0	/ GPU_AVS	/ GPIO0_C5_U	AG38 — BT_WAKE_HOST_H
SATA_CP_POD /	/ SPI0_CLK_M0 /	I2S1_SDI1_M1	/	/ PWM5_M1	/ UART0_RTSN	/ NPU_AVS	/ GPIO0_C6_U	AH42 — HOST_WAKE_BT_H
	/	/ SPI0_MISO_M0 /	I2S1_SDI2_M1	/ I2C6_SDA_M0	/ PDM0_SDI0_M1	/ UART1_RTSN_M2	/ PWM6_M0	/ GPIO0_C7_D AL40 — WIFI_REG_ON_H
	/	/ SPI3_MISO_M2 /	I2S1_SDI3_M1	/ I2C6_SCL_M0	/ PDM0_SDI1_M1	/ UART1_CTSN_M2	/ PWM7_IR_M0	/ GPIO0_D0_D AG39 — GPIO0_D0_1_8V
	/ HDMI_TX0_CEC_M1	/ SPI0_CS0_M0 /	I2S1_SDO0_M1	/ I2C0_SCL_M2	/ UART0_CTSN	/ UART1_TX_M2	/ CPU_BIG0_AVS	/ GPIO0_D1_U AH41 — I2C0_SCL_M2
	/	/ SPI3_MOSI_M2 /	I2S1_SDO1_M1	/ I2C0_SDA_M2 /		/ UART1_RX_M2	/	/ GPIO0_D2_U AG41 — I2C0_SDA_M2
	/	/ SPI3_CLK_M2 /		/	/	/	/ LITCPU_AVS	/ GPIO0_D3_U AG37 — GPIO0_D3_1_8V
SATA_CPDET	/ HDMI_TX0_SDA_M1	/ SPI3_CS0_M2 /	I2S1_SDO2_M1	/ I2C1_SCL_M2	/ PDM0_SDI2_M1	/ CAN2_RX_M1	/ PWM3_IR_M0	/ GPIO0_D4_U AL39 — BT_REG_ON_H
SATA_MP_SWITCH /	HDMI_TX0_SCL_M1	/ SPI3_CS1_M2 /	I2S1_SDO3_M1	/ I2C1_SDA_M2 /		/ CAN2_TX_M1	/ CPU_BIG1_AVS	/ GPIO0_D5_U AM39 — TP_INT_L
	/	/	/	/ PDM0_SDI3_M1 /		/	PMIC_SLEEP6	/ GPIO0_D6_D AG42 — VSEL6

VCC1V8_PMU_DDR_S3
PMUIO2_1V8_1 — V37
PMUIO2_1V8_2 — Y37
C1106 100nF X5R 10V C0201

VCC1V8_PMU_DDR_S3
PMUIO2_1 — V35
PMUIO2_2 — V36
C1107 100nF X5R 10V C0201

VCC1V8_PMU_DDR_S3
R1113 2.2K 5% R0402
R1114 2.2K 5% R0402
I2C2_SCL_M0
I2C2_SDA_M0

VCC1V8_PMU_DDR_S3
R1111 2.2K 5% R0402
R1112 2.2K 5% R0402
I2C0_SCL_M2
I2C0_SDA_M2

CRY4_3R20X2R50X0R80

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RK3588S(DDR PHY)

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DDR_CH0_DQ0_A	AJ2	DDR_CH0_DQ0_A	
DDR_CH0_DQ1_A	AB4	DDR_CH0_DQ1_A	
DDR_CH0_DQ2_A	AJ1	DDR_CH0_DQ2_A	
DDR_CH0_DQ3_A	AB3	DDR_CH0_DQ3_A	
DDR_CH0_DQ4_A	AB5	DDR_CH0_DQ4_A	
DDR_CH0_DQ5_A	AE5	DDR_CH0_DQ5_A	
DDR_CH0_DQ6_A	AE2	DDR_CH0_DQ6_A	
DDR_CH0_DQ7_A	AF3	DDR_CH0_DQ7_A	
DDR_CH0_DQ8_A	AK5	DDR_CH0_DQ8_A	
DDR_CH0_DQ9_A	AN5	DDR_CH0_DQ9_A	
DDR_CH0_DQ10_A	AN4	DDR_CH0_DQ10_A	
DDR_CH0_DQ11_A	AJ6	DDR_CH0_DQ11_A	
DDR_CH0_DQ12_A	AJ3	DDR_CH0_DQ12_A	
DDR_CH0_DQ13_A	AK3	DDR_CH0_DQ13_A	
DDR_CH0_DQ14_A	AF4	DDR_CH0_DQ14_A	
DDR_CH0_DQ15_A	AF5	DDR_CH0_DQ15_A	
DDR_CH0_DM0_A	AE1	DDR_CH0_DM0_A	
DDR_CH0_DM1_A	AK4	DDR_CH0_DM1_A	
DDR_CH0_DQS0P_A	AN1	DDR_CH0_DQS0P_A	
DDR_CH0_DQS0N_A	AN2	DDR_CH0_DQS0N_A	
DDR_CH0_DQS1P_A	AV4	DDR_CH0_DQS1P_A	
DDR_CH0_DQS1N_A	AV3	DDR_CH0_DQS1N_A	
	AR6	DDR_CH0_WCK0P_A	
	AR5	DDR_CH0_WCK0N_A	
	AT4	DDR_CH0_WCK1P_A	
	AT3	DDR_CH0_WCK1N_A	
DDR_CH0_CLKP_A	AA2	DDR_CH0_CK_A	
DDR_CH0_CLKN_A	AA1	DDR_CH0_CKB_A	
DDR_CH0_A0_A	U1	DDR_CH0_A0_A	
DDR_CH0_A1_A	AC2	DDR_CH0_A1_A	
DDR_CH0_A2_A	AF1	DDR_CH0_A2_A	
DDR_CH0_A3_A	AL2	DDR_CH0_A3_A	
DDR_CH0_A4_A	Y1	DDR_CH0_A4_A	
DDR_CH0_A5_A	AG2	DDR_CH0_A5_A	
	AM2	DDR_CH0_A6_A	
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	AK1	DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	AD1	DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	
DDR_CH0_LP4/4X_CS0_A	Y2	DDR_CH0_LP4/4X_CS0_A	
DDR_CH0_LP4/4X_CS1_A	AC1	DDR_CH0_LP4/4X_CS1_A	
DDR_RESET	AG1	DDR_CH0_RESET_A	
VDDQ_DDR_S0 R1200 240R R0201 1%	AM1	DDR_CH0_ZQ_A	

DDR_CH0_DQ0_B	U3	DDR_CH0_DQ0_B	DDR_CH0_DQ0_B
DDR_CH0_DQ1_B	AA5	DDR_CH0_DQ1_B	DDR_CH0_DQ1_B
DDR_CH0_DQ2_B	N1	DDR_CH0_DQ2_B	DDR_CH0_DQ2_B
DDR_CH0_DQ3_B	U5	DDR_CH0_DQ3_B	DDR_CH0_DQ3_B
DDR_CH0_DQ4_B	P4	DDR_CH0_DQ4_B	DDR_CH0_DQ4_B
DDR_CH0_DQ5_B	P3	DDR_CH0_DQ5_B	DDR_CH0_DQ5_B
DDR_CH0_DQ6_B	U4	DDR_CH0_DQ6_B	DDR_CH0_DQ6_B
DDR_CH0_DQ7_B	P5	DDR_CH0_DQ7_B	DDR_CH0_DQ7_B
DDR_CH0_DQ8_B	G5	DDR_CH0_DQ8_B	DDR_CH0_DQ8_B
DDR_CH0_DQ9_B	J3	DDR_CH0_DQ9_B	DDR_CH0_DQ9_B
DDR_CH0_DQ10_B	G4	DDR_CH0_DQ10_B	DDR_CH0_DQ10_B
DDR_CH0_DQ11_B	J4	DDR_CH0_DQ11_B	DDR_CH0_DQ11_B
DDR_CH0_DQ12_B	N5	DDR_CH0_DQ12_B	DDR_CH0_DQ12_B
DDR_CH0_DQ13_B	N2	DDR_CH0_DQ13_B	DDR_CH0_DQ13_B
DDR_CH0_DQ14_B	J5	DDR_CH0_DQ14_B	DDR_CH0_DQ14_B
DDR_CH0_DQ15_B	N6	DDR_CH0_DQ15_B	DDR_CH0_DQ15_B
DDR_CH0_DM0_B	V5	DDR_CH0_DM0_B	DDR_CH0_DM0_B
DDR_CH0_DM1_B	G2	DDR_CH0_DM1_B	DDR_CH0_DM1_B
DDR_CH0_DQS0P_B	B2	DDR_CH0_DQS0P_B	DDR_CH0_DQS0P_B
DDR_CH0_DQS0N_B	B1	DDR_CH0_DQS0N_B	DDR_CH0_DQS0N_B
DDR_CH0_DQS1P_B	K1	DDR_CH0_DQS1P_B	DDR_CH0_DQS1P_B
DDR_CH0_DQS1N_B	K2	DDR_CH0_DQS1N_B	DDR_CH0_DQS1N_B
	C4	DDR_CH0_WCK0P_B	
	C3	DDR_CH0_WCK0N_B	
	E3	DDR_CH0_WCK1P_B	
	E4	DDR_CH0_WCK1N_B	
DDR_CH0_CK_B	V2	DDR_CH0_CK_B	DDR_CH0_CLKP_B
DDR_CH0_CKB_B	V1	DDR_CH0_CKB_B	DDR_CH0_CLKN_B
DDR_CH0_A0_B	U2	DDR_CH0_A0_B	DDR_CH0_A0_B
DDR_CH0_A1_B	R2	DDR_CH0_A1_B	DDR_CH0_A1_B
DDR_CH0_A2_B	R1	DDR_CH0_A2_B	DDR_CH0_A2_B
DDR_CH0_A3_B	D2	DDR_CH0_A3_B	DDR_CH0_A3_B
DDR_CH0_A4_B	E1	DDR_CH0_A4_B	DDR_CH0_A4_B
DDR_CH0_A5_B	L1	DDR_CH0_A5_B	DDR_CH0_A5_B
DDR_CH0_A6_B	H1		
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	H2	DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	DDR_CH0_LP4/4X_CKE0/LP5_CS0_B
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	F1	DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	DDR_CH0_LP4/4X_CKE1/LP5_CS1_B
DDR_CH0_LP4/4X_CS0_B	J1	DDR_CH0_LP4/4X_CS0_B	DDR_CH0_LP4/4X_CS0_B
DDR_CH0_LP4/4X_CS1_B	M1	DDR_CH0_LP4/4X_CS1_B	DDR_CH0_LP4/4X_CS1_B
DDR_CH0_RESET_B	P1		
DDR_CH0_ZQ_B	C1	1 240R R1201 R0201 1% 2	VDDQ_DDR_S0

DDR_PLL Power

DDR_CH0_PLL_DVDD	0.75-0.85V	
DDR_CH0_PLL_AVDD1V8	1.8V	
DDR_CH0_PLL_AVSS		
VDDA_DDR_PLL_S0	AB14	
AVDD1V8_DDR_PLL_S0	Y14	
	AA14	

LP4/4x CKE&LP5 CS Power&Reset

DDR_CH0_VDDQ_CKE_1	M6	VDDQ_DDR_CKE_S3
DDR_CH0_VDDQ_CKE_2	M7	

LPDDR4/4x =1.1V
LPDDR5 =1.05V

Memory Interface Power

DDR_CH0_VDD_MIF_1		
DDR_CH0_VDD_MIF_2	0.75-0.85V	
DDR_CH0_VDD_MIF_3		
VDD_DDR_S0	V12	
	V13	
	V14	

CK Power

DDR_CH0_VDDQ_CK_1	K9	VDDQ_DDR_CK_S0
DDR_CH0_VDDQ_CK_2	L9	

LPDDR4/4x =0.6V
LPDDR5 =0.5V

Digital Core Power

DDR_CH0_VDD_1		
DDR_CH0_VDD_2	0.75-0.85V	
DDR_CH0_VDD_3		
DDR_CH0_VDD_4		
	T12	
	T13	
	U12	
	U13	

DDR_IO Power (CKE and Reset)

DDR_CH0_VDDQ_1	P10	VDDQ_DDR_S0
DDR_CH0_VDDQ_2	R10	
DDR_CH0_VDDQ_3	T10	
DDR_CH0_VDDQ_4	V10	
DDR_CH0_VDDQ_5	W10	
DDR_CH0_VDDQ_6	Y10	

LPDDR4/4x =0.6V
LPDDR5 =0.5V

U1000-BRK3588S

DDR_CH1_DQ0_C	B20	DDR_CH1_DQ0_C	
DDR_CH1_DQ1_C	E20	DDR_CH1_DQ1_C	
DDR_CH1_DQ2_C	A20	DDR_CH1_DQ2_C	
DDR_CH1_DQ3_C	F20	DDR_CH1_DQ3_C	
DDR_CH1_DQ4_C	C17	DDR_CH1_DQ4_C	
DDR_CH1_DQ5_C	C16	DDR_CH1_DQ5_C	
DDR_CH1_DQ6_C	D17	DDR_CH1_DQ6_C	
DDR_CH1_DQ7_C	D16	DDR_CH1_DQ7_C	
DDR_CH1_DQ8_C	D10	DDR_CH1_DQ8_C	
DDR_CH1_DQ9_C	B12	DDR_CH1_DQ9_C	
DDR_CH1_DQ10_C	A12	DDR_CH1_DQ10_C	
DDR_CH1_DQ11_C	C10	DDR_CH1_DQ11_C	
DDR_CH1_DQ12_C	C13	DDR_CH1_DQ12_C	
DDR_CH1_DQ13_C	E13	DDR_CH1_DQ13_C	
DDR_CH1_DQ14_C	A16	DDR_CH1_DQ14_C	
DDR_CH1_DQ15_C	B16	DDR_CH1_DQ15_C	
DDR_CH1_DM0_C	E17	DDR_CH1_DM0_C	
DDR_CH1_DM1_C	D13	DDR_CH1_DM1_C	
DDR_CH1_DQS0P_C	A9	DDR_CH1_DQS0P_C	
DDR_CH1_DQS0N_C	B9	DDR_CH1_DQS0N_C	
DDR_CH1_DQS1P_C	A3	DDR_CH1_DQS1P_C	
DDR_CH1_DQS1N_C	A4	DDR_CH1_DQS1N_C	
	C8	DDR_CH1_WCK0P_C	
	D8	DDR_CH1_WCK0N_C	
	B6	DDR_CH1_WCK1P_C	
	A6	DDR_CH1_WCK1N_C	
DDR_CH1_CLKP_C	C21	DDR_CH1_CK_C	
DDR_CH1_CLKN_C	D21	DDR_CH1_CKB_C	
DDR_CH1_A0_C	B18	DDR_CH1_A0_C	
DDR_CH1_A1_C	A21	DDR_CH1_A1_C	
DDR_CH1_A2_C	B22	DDR_CH1_A2_C	
DDR_CH1_A3_C	A7	DDR_CH1_A3_C	
DDR_CH1_A4_C	A10	DDR_CH1_A4_C	
DDR_CH1_A5_C	A15	DDR_CH1_A5_C	
	B7	DDR_CH1_A6_C	
DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	A18	DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	
DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	A13	DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	
DDR_CH1_LP4/4X_CS0_C	B15	DDR_CH1_LP4/4X_CS0_C	
DDR_CH1_LP4/4X_CS1_C	A19	DDR_CH1_LP4/4X_CS1_C	
	B13	DDR_CH1_RESET_C	
VDDQ_DDR_S0 R1202 240R R0201 1%	A5	DDR_CH1_ZQ_C	

DDR_CH1_DQ0_D	A24	DDR_CH1_DQ0_D	DDR_CH1_DQ0_D
DDR_CH1_DQ1_D	C25	DDR_CH1_DQ1_D	DDR_CH1_DQ1_D
DDR_CH1_DQ2_D	B24	DDR_CH1_DQ2_D	DDR_CH1_DQ2_D
DDR_CH1_DQ3_D	A28	DDR_CH1_DQ3_D	DDR_CH1_DQ3_D
DDR_CH1_DQ4_D	D25	DDR_CH1_DQ4_D	DDR_CH1_DQ4_D
DDR_CH1_DQ5_D	B28	DDR_CH1_DQ5_D	DDR_CH1_DQ5_D
DDR_CH1_DQ6_D	C27	DDR_CH1_DQ6_D	DDR_CH1_DQ6_D
DDR_CH1_DQ7_D	C29	DDR_CH1_DQ7_D	DDR_CH1_DQ7_D
DDR_CH1_DQ8_D	D34	DDR_CH1_DQ8_D	DDR_CH1_DQ8_D
DDR_CH1_DQ9_D	D29	DDR_CH1_DQ9_D	DDR_CH1_DQ9_D
DDR_CH1_DQ10_D	F29	DDR_CH1_DQ10_D	DDR_CH1_DQ10_D
DDR_CH1_DQ11_D	E32	DDR_CH1_DQ11_D	DDR_CH1_DQ11_D
DDR_CH1_DQ12_D	B32	DDR_CH1_DQ12_D	DDR_CH1_DQ12_D
DDR_CH1_DQ13_D	C34	DDR_CH1_DQ13_D	DDR_CH1_DQ13_D
DDR_CH1_DQ14_D	C32	DDR_CH1_DQ14_D	DDR_CH1_DQ14_D
DDR_CH1_DQ15_D	A32	DDR_CH1_DQ15_D	DDR_CH1_DQ15_D
DDR_CH1_DM0_D	D27	DDR_CH1_DM0_D	DDR_CH1_DM0_D
DDR_CH1_DM1_D	C33	DDR_CH1_DM1_D	DDR_CH1_DM1_D
DDR_CH1_DQS0P_D	B41	DDR_CH1_DQS0P_D	DDR_CH1_DQS0P_D
DDR_CH1_DQS0N_D	A41	DDR_CH1_DQS0N_D	DDR_CH1_DQS0N_D
DDR_CH1_DQS1P_D	D36	DDR_CH1_DQS1P_D	DDR_CH1_DQS1P_D
DDR_CH1_DQS1N_D	C36	DDR_CH1_DQS1N_D	DDR_CH1_DQS1N_D
	B39	DDR_CH1_WCK0P_D	
	A39	DDR_CH1_WCK0N_D	
	A37	DDR_CH1_WCK1P_D	
	B37	DDR_CH1_WCK1N_D	
DDR_CH1_CLKP_D	C23	DDR_CH1_CK_D	DDR_CH1_CLKP_D
DDR_CH1_CLKN_D	D23	DDR_CH1_CKB_D	DDR_CH1_CLKN_D
DDR_CH1_A0_D	A26	DDR_CH1_A0_D	DDR_CH1_A0_D
DDR_CH1_A1_D	A27	DDR_CH1_A1_D	DDR_CH1_A1_D
DDR_CH1_A2_D	A30	DDR_CH1_A2_D	DDR_CH1_A2_D
DDR_CH1_A3_D	A36	DDR_CH1_A3_D	DDR_CH1_A3_D
DDR_CH1_A4_D	B33	DDR_CH1_A4_D	DDR_CH1_A4_D
DDR_CH1_A5_D	A38	DDR_CH1_A5_D	DDR_CH1_A5_D
	A33		
DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	A35	DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	DDR_CH1_LP4/4X_CKE0/LP5_CS0_D
DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	A31	DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	DDR_CH1_LP4/4X_CKE1/LP5_CS1_D
DDR_CH1_LP4/4X_CS0_D	B30	DDR_CH1_LP4/4X_CS0_D	DDR_CH1_LP4/4X_CS0_D
DDR_CH1_LP4/4X_CS1_D	A23	DDR_CH1_LP4/4X_CS1_D	DDR_CH1_LP4/4X_CS1_D
DDR_CH1_RESET_D	B25		
R1203 240R R0201 1%	A40		VDDQ_DDR_S0

DDR_PLL Power

DDR_CH1_PLL_DVDD	0.75-0.85V	
DDR_CH1_PLL_AVDD1V8	1.8V	
DDR_CH1_PLL_AVSS		
VDDA_DDR_PLL_S0	M16	
AVDD1V8_DDR_PLL_S0	L15	
	N15	

LP4/4x CKE&LP5 CS Power&Reset

DDR_CH1_VDDQ_CKE	G24	VDDQ_DDR_CKE_S3

LPDDR4/4x =1.1V
LPDDR5 =1.05V

Memory Interface Power

DDR_CH1_VDD_MIF_1		
DDR_CH1_VDD_MIF_2	0.75-0.85V	
DDR_CH1_VDD_MIF_3		
VDD_DDR_S0	J20	
	K20	
	L20	

CK Power

DDR_CH1_VDDQ_CK	H24	VDDQ_DDR_CK_S0

LPDDR4/4x =0.6V
LPDDR5 =0.5V

Digital Core Power

DDR_CH1_VDD_1		
DDR_CH1_VDD_2	0.75-0.85V	
DDR_CH1_VDD_3		
	J18	
	K18	
	L18	

DDR_IO Power (CKE and Reset)

DDR_CH1_VDDQ_1	H14	VDDQ_DDR_S0
DDR_CH1_VDDQ_2	H15	
DDR_CH1_VDDQ_3	H16	
DDR_CH1_VDDQ_4	H18	
DDR_CH1_VDDQ_5	H20	

LPDDR4/4x =0.6V
LPDDR5 =0.5V

DDR FILTER

VDDQ_DDR_S0: C1200 10uF C0402 X5R 4V; C1202 100nF X5R 10V C0201; C1203 100nF X5R 10V C0201; C1204 100nF X5R 10V C0201

VDD_DDR_S0: C1217 10uF C0402 X5R 4V; C1218 100nF X5R 10V C0201

VDD_DDR_S0: C1219 1uF C0201 X5R 4V; C1220 100nF X5R 10V C0201

AVDD1V8_DDR_PLL_S0: C1209 1uF C0201 X5R 4V

VDDA_DDR_PLL_S0: C1210 1uF C0201 X5R 4V

VDDQ_DDR_CK_S0: C1213 1uF C0201 X5R 4V

VDDQ_DDR_CKE_S3: C1212 1uF C0201 X5R 4V

VDDQ_DDR_S0: C1205 10uF C0402 X5R 4V; C1206 100nF X5R 10V C0201; C1207 100nF X5R 10V C0201; C1208 100nF X5R 10V C0201

VDD_DDR_S0: C1221 1uF C0201 X5R 4V; C1222 100nF X5R 10V C0201

VDD_DDR_S0: C1223 10uF C0402 X5R 4V; C1224 100nF X5R 10V C0201

VDDQ_DDR_S0: C1250 100nF X5R 10V C0201; C1251 100nF X5R 10V C0201; C1252 100nF X5R 10V C0201; C1253 100nF X5R 10V C0201

AVDD1V8_DDR_PLL_S0: C1214 1uF C0201 X5R 4V

VDDA_DDR_PLL_S0: C1215 1uF C0201 X5R 4V

VDDQ_DDR_CKE_S3: C1211 1uF C0201 X5R 4V

VDDQ_DDR_CK_S0: C1216 1uF C0201 X5R 4V

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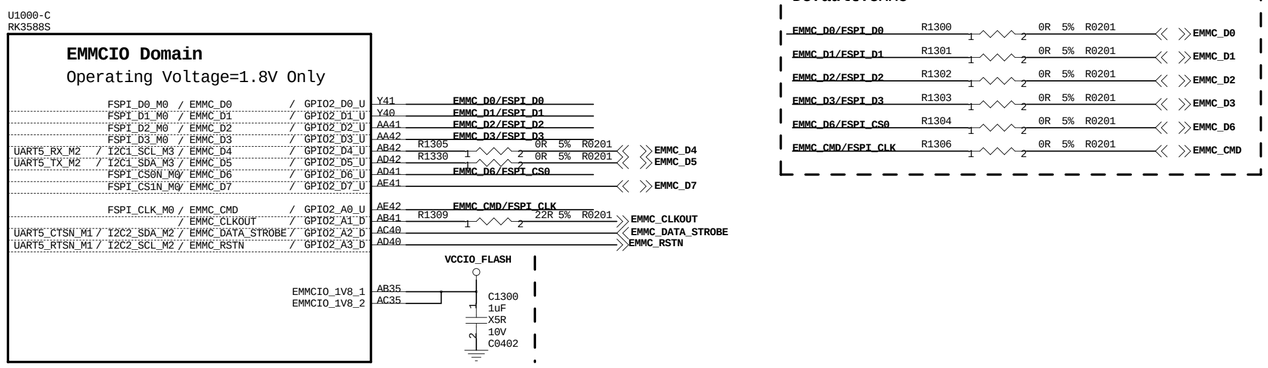
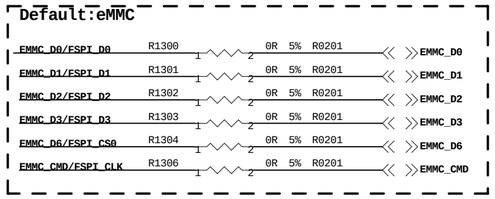
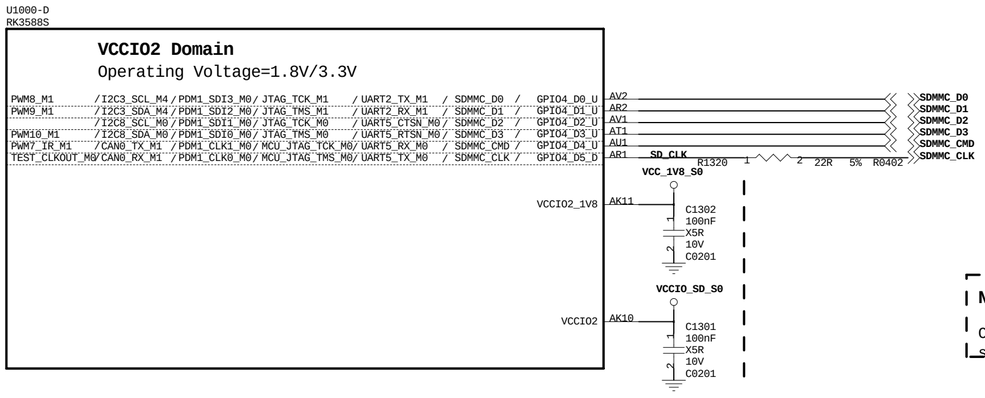
RK3588S(EMMCIO Domain)





RK3588S(VCCIO2 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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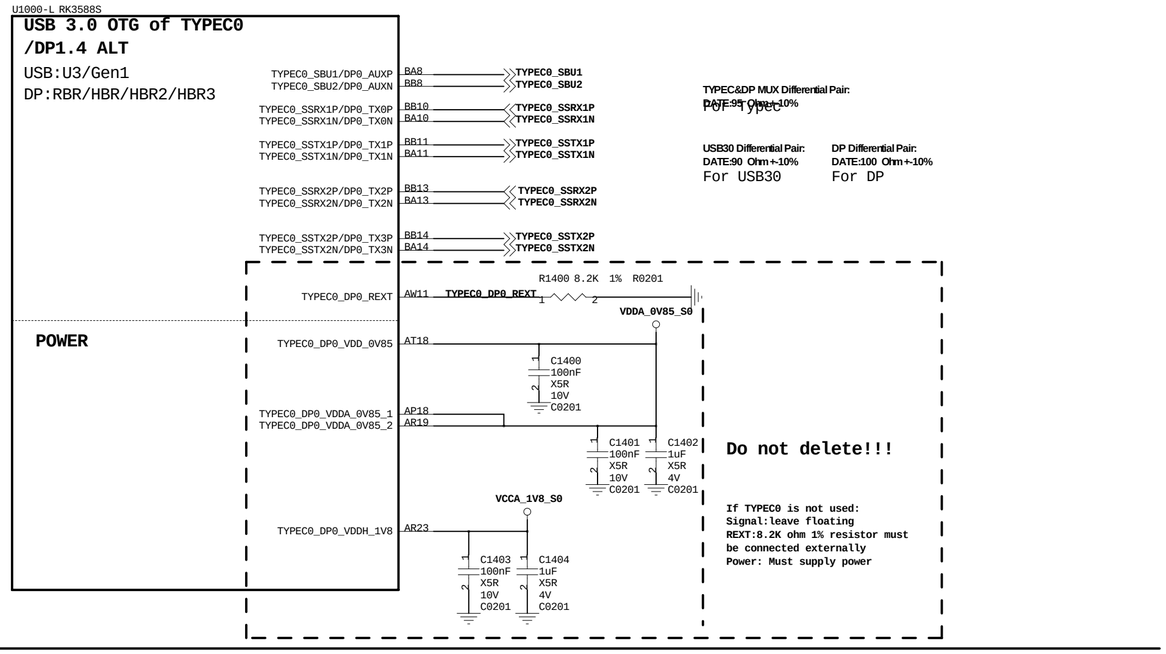
RK3588S(USB3.0/DP1.4)

ok

USB30/DP1.4 Alt Mode Configuration

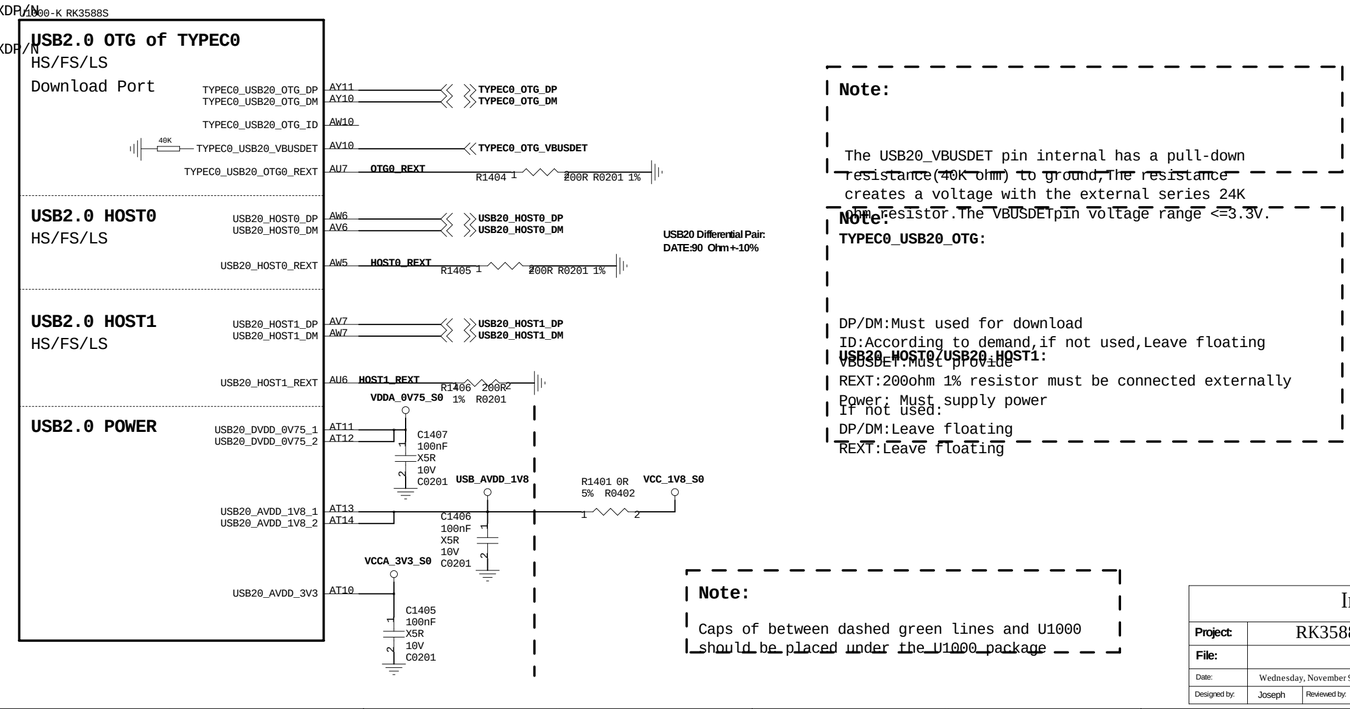
Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



RK3588S(USB2.0)

ok



Note:

The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,the resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power
If not used:
DP/DM:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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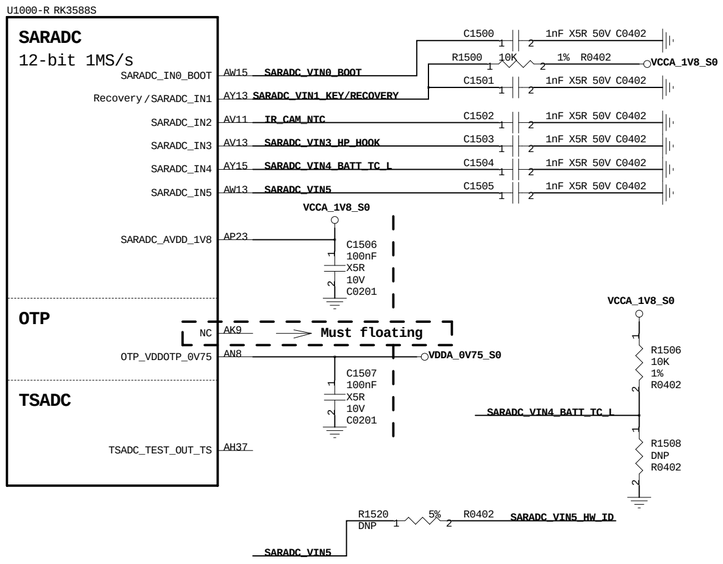
RK3588S(SARADC/OTP/TSADC)

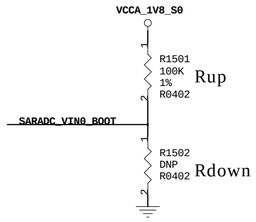
SARADC_VIN1_KEY/RECOVERY
IR_CAM_NTC

SARADC_VIN0_BOOT

IR_CAM_NTC

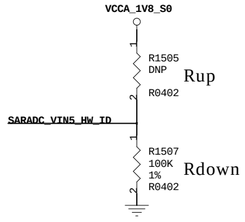


BOOT MODE CONFIG



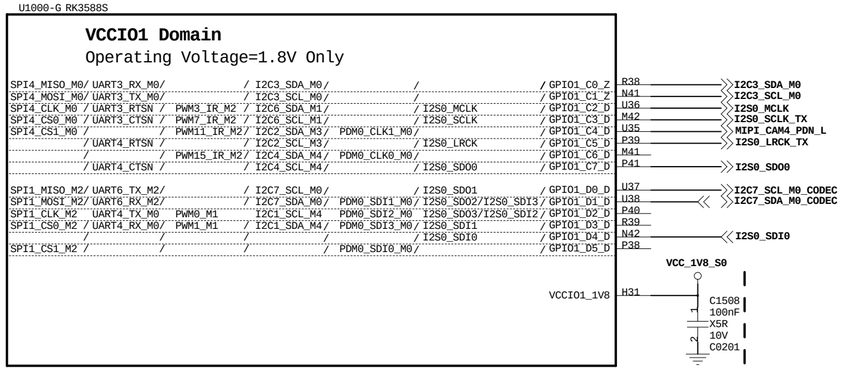
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB **(Maskrom mode)**
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

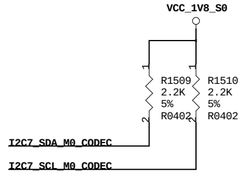
BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S(VCCIO1 Domain)





Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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RK3588S(MIPI_DPHY CSI0 RX)

U1000-N RK3588S

MIPI DPHY CSI_RX Port0

MIPI V1.2
2.5Gbps

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI0_CLK0P	AN42	MIPI_CSI0_RX_CLK0P
MIPI_CSI0_CLK0N	AN41	MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P	AL42	MIPI_CSI0_RX_D0P
MIPI_CSI0_D0N	AL41	MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P	AK41	MIPI_CSI0_RX_D1P
MIPI_CSI0_D1N	AK42	MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P	AU41	MIPI_CSI0_RX_CLK1P
MIPI_CSI0_CLK1N	AU42	MIPI_CSI0_RX_CLK1N
MIPI_CSI0_D2P	AT41	MIPI_CSI0_RX_D2P
MIPI_CSI0_D2N	AT42	MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P	AP42	MIPI_CSI0_RX_D3P
MIPI_CSI0_D3N	AP41	MIPI_CSI0_RX_D3N

VDDA_0V75_S0
MIPI_CSI0_AVCC0V75 AM37
C1602 100nF X5R 10V C0201
C1603 1uF X5R 4V C0201

VCCA_1V8_S0
MIPI_CSI0_AVCC1V8 AM35
C1600 1uF X5R 4V C0201
C1601 100nF X5R 10V C0201

Note:

If not used:
~~Signal:leave floating~~
Power: Floating

Option1	***Sensor1 x4Lane***	***MIPI_CSI_RX_D0-3*** ***MIPI_CSI_RX_CLK0***
Option2	***Sensor1 x2Lane*** ***+*** ***Sensor2 x2Lane***	***MIPI_CSI_RX_D0-1*** ***MIPI_CSI_RX_CLK0*** ***MIPI_CSI_RX_D2-3*** ***MIPI_CSI_RX_CLK1***

Note:

When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)

D-PHY:V2.0
4.5Gbps/Lane

MIPI D/C-PHY DSI_TX Port0

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	BB34	MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	BA34	MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	BB31	MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	BA31	MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	BA32	MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	BB32	MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	BA35	MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	BB35	MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE	BB37	MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	BA37	MIPI_DPHY0_TX_D3N

Default
MIPI_DPHY0_TX

MIPI_DPHY0_TX_CLKP		MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN		MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P		MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N		MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P		MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N		MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P		MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N		MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P		MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N		MIPI_DPHY0_TX_D3N

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	BB41
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	BA41
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	BA38
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	BB38
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	BA40
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AY40
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AY42
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	BA42
MIPI_DPHY0_RX_D3P/NO_USE	AW41
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AW42

Power

MIPI_D/C_PHY0_VREG AT33 MIPI_D/C_PHY0_VREG
C1604 1uF X5R 4V C0201

VDDA_0V75_S0
MIPI_D/C_PHY0_VDD AR33
C1605 1uF X5R 4V C0201
C1611 100nF X5R 10V C0201

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

VDDA_1V2_S0
MIPI_D/C_PHY_VDD_1V2_1 AR34
C1607 100nF X5R 10V C0201

VCCA_1V8_S0
MIPI_D/C_PHY_VDD_1V8_1 AR30
C1609 100nF X5R 10V C0201

Note:

If not used:
~~Signal:leave floating~~
Power: Floating

RK3588S(MIPI_D/C PHY1)

D-PHY:V2.0
4.5Gbps/Lane

MIPI D/C-PHY DSI_TX Port1

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	BB19
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	BA19
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	BB16
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	BA16
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	BA17
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	BB17
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	BA20
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	BB20
MIPI_DPHY1_TX_D3P/NO_USE	BB22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	BA22

Note:

The Port also support MIPI_CPHY1_TX,if need please Refer to the circuit of MIPI_CPHY0_TX

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	BA26
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	BB26
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	BA23
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	BB23
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	BB25
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	BA25
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	BB28
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	BA28
MIPI_DPHY1_RX_D3P/NO_USE	BA29
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	BB29

Power

MIPI_D/C_PHY1_VREG AT27 MIPI_D/C_PHY1_VREG
C1612 X5R 4V C0201

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

VDDA_0V75_S0
MIPI_D/C_PHY1_VDD AR27
R234
C1613 X5R 4V C0201

VDDA_1V2_S0
MIPI_D/C_PHY_VDD_1V2_2 AR35
R236
C1608 X5R 10V C0201

VCCA_1V8_S0
MIPI_D/C_PHY_VDD_1V8_2 AT30
R235
C1610 X5R 10V C0201

Note:

If not used:
~~Signal:leave floating~~
Power: Floating

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RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm¡ À10%

HDMI TX
100 Ohm¡ À10%

U1000-Q

HDMI TX/eDP1.3 MUX Port0
eDP£ºV1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P — BB4 HDMI0_TX0P
HDMI_TX0_D0N/EDP_TX0_D0N — BA4 HDMI0_TX0N
HDMI_TX0_D1P/EDP_TX0_D1P — BA5 HDMI0_TX1P
HDMI_TX0_D1N/EDP_TX0_D1N — BB5 HDMI0_TX1N
HDMI_TX0_D2P/EDP_TX0_D2P — BB7 HDMI0_TX2P
HDMI_TX0_D2N/EDP_TX0_D2N — BA7 HDMI0_TX2N
HDMI_TX0_D3P/EDP_TX0_D3P — BA2 HDMI0_TX3P
HDMI_TX0_D3N/EDP_TX0_D3N — BB2 HDMI0_TX3N
HDMI_TX0_SBDP/EDP_TX0_AUXP — BA1 HDMI0_TX_SBDP
HDMI_TX0_SBDN/EDP_TX0_AUXN — AY1 HDMI0_TX_SBDN
HDMI/EDP_TX0_REXT — AY3 HDMI/EDP_TX0_REXT — R1708 8.2K 1% R0201 — VDDA_0V75_S0

POWER

HDMI/EDP_TX0_VDD_0V75_1 — AM13
HDMI/EDP_TX0_VDD_0V75_2 — AN12
C1710 100nF X5R 10V C0201
C1711 4.7uF X5R 6.3V C0402
C1718 10uF X5R 6.3V C0603

HDMI/EDP_TX0_AVDD_0V75 — AN10
C1712 100nF X5R 10V C0201
C1725 1uF X5R 4V C0201

VCCA_1V8_S0

HDMI/EDP_TX0_VDD_IO_1V8 — AK12
HDMI/EDP_TX0_VDD_CMN_1V8 — AL14
C1713 100nF X5R 10V C0201
C1714 4.7uF X5R 6.3V C0402
C1716 4.7uF X5R 6.3V C0402

RK3588S

Option2:HDMI_TX0

HDMI0_TX0P ⟷ HDMI0_TX0P
HDMI0_TX0N ⟷ HDMI0_TX0N
HDMI0_TX1P ⟷ HDMI0_TX1P
HDMI0_TX1N ⟷ HDMI0_TX1N
HDMI0_TX2P ⟷ HDMI0_TX2P
HDMI0_TX2N ⟷ HDMI0_TX2N
HDMI0_TX3P ⟷ HDMI0_TX3P
HDMI0_TX3N ⟷ HDMI0_TX3N
HDMI0_TX_SBDP ⟷ HDMI0_TX_SBDP
HDMI0_TX_SBDN ⟷ HDMI0_TX_SBDN

Note:

If not used:
Signal: leave floating
Power: Floating or tie to VSS

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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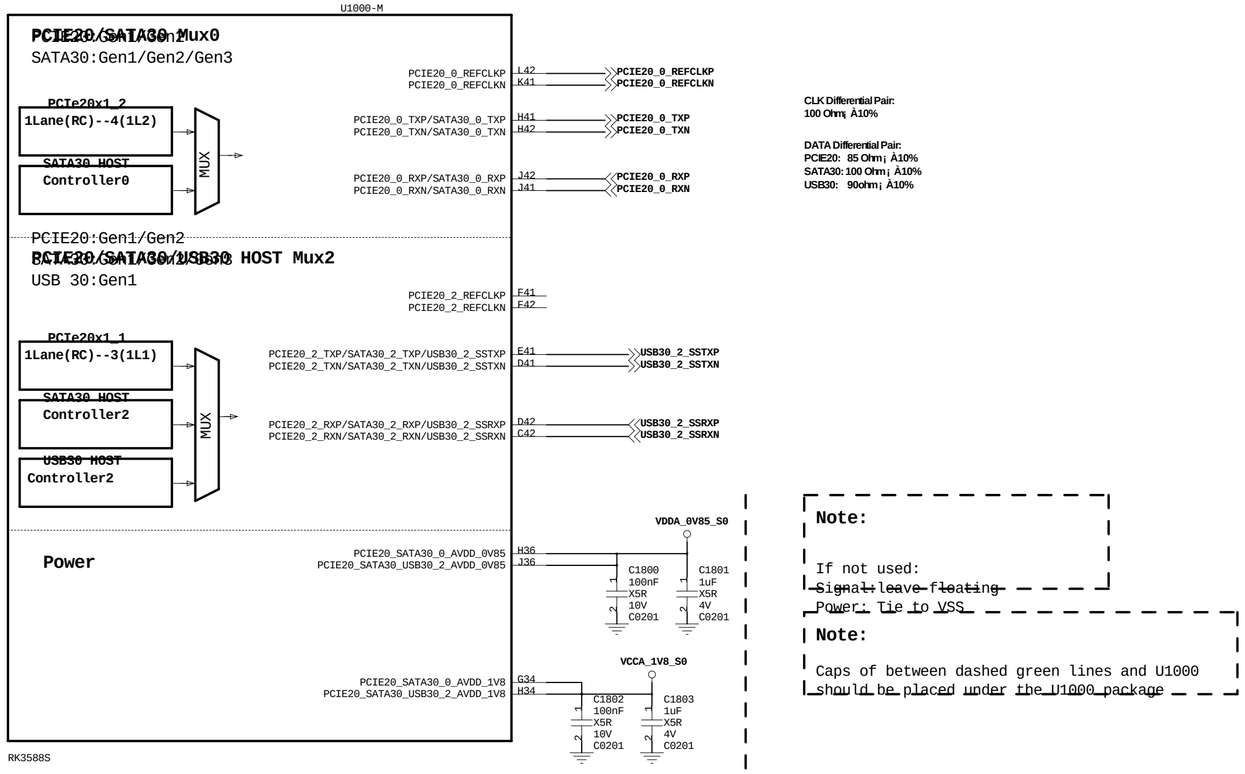
RK3588S(PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm¡ À10%

DATA Differential Pair:
PCIE20: 85 Ohm¡ À10%
SATA30: 100 Ohm¡ À10%
USB30: 90ohm¡ À10%

Note:

If not used:
~~Signal: leave floating~~
Power: Tie to VSS

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* ~~PCIE20X1_1_WAKEN_M*~~ PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

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RK3588S(VCCIO4 Domain)

U1000-H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	PCIE20X1_1_CLKREQN_M2	DP0_HPDIN_M2	UART6_RX_M1	SPI4_MISO_M2	I2C2_SDA_M4	GPIO1_A0_D	G40
	PCIE20X1_1_WAKEN_M2		UART6_TX_M1	SPI4_MOSI_M2	I2C2_SCL_M4	GPIO1_A1_D	L40
PWM0_M2		VOP_POST_EMPTY	UART6_RTSN_M1	SPI4_CLK_M2	I2C4_SDA_M3	GPIO1_A2_D	D38 — I2C4_SDA_M3_TP
PWM1_M2			UART6_CTSN_M1	SPI4_CS0_M2	I2C4_SCL_M3	GPIO1_A3_D	L39 — I2C4_SCL_M3_TP
				SPI2_MISO_M0		GPIO1_A4_D	G37 — GPIO1_A4_1_8V
		HDMI_TX0_HPD_M0		SPI2_MOSI_M0		GPIO1_A5_D	M40 — HDMI_TX0_HPD_M0
				SPI2_CLK_M0		GPIO1_A6_D	D39 — GPIO1_A6_CLK_1_8V
PWM3_IR_M3	PCIE20X1_1_PERSTN_M2			SPI2_CS0_M0	PDM1_SDI0_M1	GPIO1_A7_U	H38 — MIPI_CAM2_PDN_L
				SPI2_CS1_M0	PDM1_SDI1_M1	GPIO1_B0_U	H39 — LCD_RESET_L
				SPI0_MISO_M2	PDM1_SDI2_M1	GPIO1_B1_D	G39 — GPIO1_B1_1_8V
			UART4_RX_M2	SPI0_MOSI_M2	PDM1_SDI3_M1	GPIO1_B2_D	M38 — GPIO1_B2_1_8V
		SATA0_ACT_LED_M1	UART4_TX_M2	SPI0_CLK_M2	PDM1_CLK1_M1	GPIO1_B3_D	M37 — MIPI_CAM2_RST_L
			UART7_RX_M2	SPI0_CS0_M2	PDM1_CLK0_M1	GPIO1_B4_U	M39 — GPIO1_B4_1_8V
			UART7_TX_M2	SPI0_CS1_M2		GPIO1_B5_U	D40 — GPIO1_B5_1_8V
		MIPI_CAMERA1_CLK_M0	UART1_TX_M1	SPDIF0_TX_M0	I2C5_SCL_M3	GPIO1_B6_U	L38 — I2C5_SCL_M3_CAM
PWM13_M2	SATA2_ACT_LED_M1	MIPI_CAMERA2_CLK_M0	UART1_RX_M1	SPDIF1_TX_M0	I2C5_SDA_M3	GPIO1_B7_U	F37 — I2C5_SDA_M3_CAM
PWM14_M2		MIPI_CAMERA3_CLK_M0	UART1_RTSN_M1		I2C8_SCL_M2	GPIO1_D6_U	L37 — I2C8_SCL_M2_CAM_1_8V
PWM15_IR_M3		MIPI_CAMERA4_CLK_M0	UART1_CTSN_M1		I2C8_SDA_M2	GPIO1_D7_U	G38 — I2C8_SDA_M2_CAM_1_8V

VCCIO4_1V8_1 G27, VCCIO4_1V8_2 G28 — VCC_1V8_S0 — C1902 100nF X5R 10V C0201

VCCIO4 G31 — VCC_1V8_S0 — C1903 100nF X5R 10V C0201

VCC_1V8_S0 — R1916 2.2K 5% R0402 — I2C5_SCL_M3_CAM

VCC_1V8_S0 — R1917 2.2K 5% R0402 — I2C5_SDA_M3_CAM

RK3588S

RK3588S(VCCIO5 Domain)

U1000-I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	PWM10_M0	SPI4_MISO_M1/ I2C6_SDA_M4/	GMAC1_TXD2	I2S3_MCLK	FSPI_D0_M2	SDIO_D0_M1	GPIO3_A0_U — AR38 — SDIO_D0_M1_WIFI
AUDDSM_LN	PWM11_IR_M0	SPI4_MOSI_M1/ I2C6_SCL_M4/	GMAC1_TXD3	I2S3_SCLK	FSPI_D1_M2	SDIO_D1_M1	GPIO3_A1_U — AR37 — SDIO_D1_M1_WIFI
AUDDSM_LP	UART8_TX_M1	SPI4_CLK_M1 /	GMAC1_RXD2	I2S3_LRCK	FSPI_D2_M2	SDIO_D2_M1	GPIO3_A2_U — AT38 — SDIO_D2_M1_WIFI
AUDDSM_RN	UART8_RX_M1	SPI4_CS0_M1 /	GMAC1_RXD3	I2S3_SDO	FSPI_D3_M2	SDIO_D3_M1	GPIO3_A3_U — AT40 — SDIO_D3_M1_WIFI
AUDDSM_RP	UART8_RTSN_M1/	SPI4_CS1_M1 /	GMAC1_TXCLK	I2S3_SDI		SDIO_CMD_M1	GPIO3_A4_D — AT39 — SDIO_CMD_M1_WIFI
	UART8_CTSN_M1/	I2C4_SDA_M0/	GMAC1_RXCLK	FSPI_CLK_M2	MIPI_CAMERA0_CLK_M1	SDIO_CLK_M1	GPIO3_A5_D — AV38 SDIO_CLK_M1 — R1918 1 R0402 0R 5% — SDIO_CLK_M1_WIFI
		I2C4_SCL_M0/	ETH1_REFCLKO_25M		MIPI_CAMERA1_CLK_M1		GPIO3_A6_D — AV37 — MIPI_CAM1_CLKOUT
			GMAC1_RXD0		MIPI_CAMERA2_CLK_M1	PWM8_M0	GPIO3_A7_U — AT37 — MIPI_CAM2_CLKOUT
			GMAC1_RXD1		MIPI_CAMERA3_CLK_M1	PWM9_M0	GPIO3_B0_U — AR39 — GPIO3_B0_1_8V
	UART2_TX_M2		GMAC1_RXDV_CRS		MIPI_CAMERA4_CLK_M1	PWM2_M1	GPIO3_B1_D — AV39 — GPIO3_B1_1_8V
	UART2_RX_M2		GMAC1_TXER	I2S2_SDI_M1		PWM3_IR_M1	GPIO3_B2_D — AW34 — I2S2_SDI_M1_BT
	UART2_RTSN		GMAC1_TXD0	I2S2_SDO_M1			GPIO3_B3_U — AW35 — I2S2_SDO_M1_BT
	UART2_CTSN		GMAC1_TXD1	I2S2_MCLK_M1			GPIO3_B4_U — AV35 — MIPI_CAM4_RST_L
	UART3_TX_M1		CAN1_RX_M0 / GMAC1_TXEN	I2S2_SCLK_M1		PWM12_M0	GPIO3_B5_U — AY35 — I2S2_SCLK_M1_BT
	UART3_RX_M1		CAN1_TX_M0 / GMAC1_MCLKINOUT	I2S2_LRCK_M1		PWM13_M0	GPIO3_B6_D — AW37 — I2S2_LRCK_M1_BT
		SPI1_MOSI_M1/	I2C3_SCL_M1/ GMAC1_PTP_REF_CLK/				GPIO3_B7_D — AY34 — SPI1_MOSI_M1_1_8V
	UART7_TX_M1	SPI1_MISO_M1/	I2C3_SDA_M1/ GMAC1_PPSTRIG				GPIO3_C0_D — AR36 — SPI1_MISO_M1_1_8V
	UART7_RX_M1	SPI1_CLK_M1 /	GMAC1_PPSCLK				GPIO3_C1_D — AW38 — SPI1_CLK_M1_1_8V
	UART7_RTSN_M1/	SPI1_CS0_M1 /	I2C8_SCL_M4/ GMAC1_MDC		MIPI_TE0	PWM14_M0	GPIO3_C2_D — AV40 — TP_RST_L
	UART7_CTSN_M1/	SPI1_CS1_M1 /	I2C8_SDA_M4/ GMAC1_MDIO		MIPI_TE1	PWM15_IR_M0	GPIO3_C3_D — AW39 — SPI1_CS1_M1_1_8V
	UART5_TX_M1	SPI3_CS0_M3 /	CAN2_RX_M0 / CIF_D8		FSPI_CS0N_M2		GPIO3_C4_U — AU34 — GPIO3_C4_1_8V
	UART5_RX_M1	SPI3_CS1_M3 /	CAN2_TX_M0 / CIF_D9		FSPI_CS1N_M2		GPIO3_C5_U — AV34 — GPIO3_C5_1_8V
		SPI3_MISO_M3/	CIF_D10				GPIO3_C6_U — AV30 — LCD_PWREN_H
		SPI3_MOSI_M3/	I2C5_SCL_M0/ CIF_D11	PCIE20X1_2_CLKREQN_M0/	HDMI_TX0_SCL_M2		GPIO3_C7_U — AU30 — PCIE20X1_2_CLKREQN_M0
	UART4_RX_M1	SPI3_CLK_M3 /	I2C5_SDA_M0/ CIF_D12	PCIE20X1_2_WAKEN_M0	HDMI_TX0_SDA_M2	PWM8_M2	GPIO3_D0_U — AW31 — PCIE20X1_2_WAKEN_M0
	UART4_TX_M1	SPI0_MISO_M3/	CIF_D13	PCIE20X1_2_PERSTN_M0		PWM9_M2	GPIO3_D1_D — AY27 — PCIE20X1_2_PERSTN_M0
	UART9_RTSN_M2/	SPI0_MOSI_M3/	I2C7_SCL_M2/ CIF_D14				GPIO3_D2_D — AY30 — UART9_RTSN_M2_BT
	UART9_CTSN_M2/	SPI0_CLK_M3 /	I2C7_SDA_M2/ CIF_D15			PWM10_M2	GPIO3_D3_D — AY31 — UART9_CTSN_M2_BT
	UART9_RX_M2	SPI0_CS0_M3 /	MCU_JTAG_TCK_M1		HDMI_TX0_HPD_M1		GPIO3_D4_D — AV31 — UART9_RX_M2_BT
	UART9_TX_M2	SPI0_CS1_M3 /	MCU_JTAG_TMS_M1			PWM11_IR_M3	GPIO3_D5_D — AW30 — UART9_TX_M2_BT

RESERVED AF35

VCCIO5_1V8 AF36 — VCCIO5_1V8 — C1904 100nF X5R 10V C0201 — VCC_1V8_S0 — R1909 0R 5% R0402

VCCIO5_1 AC33, VCCIO5_2 AC34 — VCCIO5 — C1905 100nF X5R 10V C0201 — VCC_1V8_S0 — R1927 0R 5% R0402

RK3588S

RK3588S(VCCIO6 Domain)

U1000-J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

BT1120_D0	CIF_D0		I2S1_MCLK_M0	UART9_RTSN_M1	SPI0_MISO_M1 /		PCIE20X1_1_CLKREQN_M1/	GPIO4_A0_D — AV19 — TYPEC0_SBU1_DC
BT1120_D1	CIF_D1		I2S1_SCLK_M0	UART9_CTSN_M1	SPI0_MOSI_M1 /		PCIE20X1_1_WAKEN_M1	GPIO4_A1_D — AW18 — TYPEC0_SBU2_DC
BT1120_D2	CIF_D2		I2S1_LRCK_M0	/	SPI0_CLK_M1 /		PCIE20X1_1_PERSTN_M1	GPIO4_A2_D — AV26 — GPIO4_A2
BT1120_D3	CIF_D3		/	UART0_TX_M2	/	/	/	GPIO4_A3_D — AV19 — UART0_TX_M2
BT1120_D4	CIF_D4		/	UART0_RX_M2	SPI2_MISO_M1 /	I2C3_SCL_M2	/	GPIO4_A4_D — AW19 — UART0_RX_M2
BT1120_D5	CIF_D5		I2S1_SDI0_M0	UART3_TX_M2	SPI2_MOSI_M1 /	I2C3_SDA_M2	/	GPIO4_A5_D — AU15 — TYPEC5V_PWREN_H
BT1120_D6	CIF_D6		I2S1_SDI1_M0	UART3_RX_M2	SPI2_CLK_M1 /	I2C5_SCL_M2	/	GPIO4_A6_D — AV18 — GPIO4_A6
BT1120_D7	CIF_D7		I2S1_SDI2_M0	/	SPI2_CS0_M1 /	I2C5_SDA_M2	/	GPIO4_A7_D — AW26 — GPIO4_A7
BT1120_CLKOUT/	CIF_CLKIN		I2S1_SDI3_M0	UART8_TX_M0	SPI2_CS1_M1 /	I2C6_SDA_M3	/	GPIO4_B0_D — AW27 — I2C6_SDA_M3
SPDIF1_TX_M1	MIPI_CAMERA0_CLK_M0/	SATA2_ACT_LED_M0/	I2S1_SDO0_M0	UART8_RX_M0	SPI0_CS1_M1 /	I2C6_SCL_M3	/	GPIO4_B1_U — AU22 — I2C6_SCL_M3
CAN1_RX_M1 / BT1120_D8	CIF_HREF	PWM14_M1	I2S1_SDO1_M0	UART8_RTSN_M0	SPI0_CS0_M1 /	I2C7_SCL_M3	PCIE20X1_1_BUTTON_RSTN	GPIO4_B2_U — AT15 — LCD_BL_PWM14_M1
CAN1_TX_M1 / BT1120_D9	CIF_VSYNC	PWM15_IR_M1	I2S1_SDO2_M0	UART8_CTSN_M0	/	I2C7_SDA_M3	PCIE20X1_2_BUTTON_RSTN	GPIO4_B3_U — AV23 — GPIO4_B3
BT1120_D10	CIF_CLKOUT	PWM11_IR_M1	I2S1_SDO3_M0	UART9_TX_M1	/	DP0_HPDIN_M0 /	SPDIF0_TX_M1	GPIO4_B4_U — AV27 — GPIO4_B4
BT1120_D11	/	PWM12_M1	/	UART9_RX_M1	SPI3_MISO_M1 /		/	GPIO4_B5_D — AU23 — GPIO4_B5
BT1120_D12	/	PWM13_M1	/	/	SPI3_MOSI_M1 /	I2C5_SCL_M1 /	SATA0_ACT_LED_M0	GPIO4_B6_D — AW22 — HDMI0_TX_ON_H
BT1120_D13	/	/	HDMI_TX0_SCL_M0	/	SPI3_CLK_M1 /	I2C5_SDA_M1 /	PCIE20X1_2_CLKREQN_M1/	GPIO4_B7_U — AV22 — HDMI_TX0_SCL_M0
BT1120_D14	/	/	HDMI_TX0_SDA_M0	/	SPI3_CS0_M1 /	I2C8_SCL_M3	PCIE20X1_2_WAKEN_M1	GPIO4_C0_U — AW23 — HDMI_TX0_SDA_M0
BT1120_D15	SPDIF1_TX_M2	PWM6_M1	HDMI_TX0_CEC_M0	/	SPI3_CS1_M1 /	I2C8_SDA_M3 /	PCIE20X1_2_PERSTN_M1	GPIO4_C1_D — AY26 — HDMI_TX0_CEC_M0

Note:
BT1120 Only Support Output

RK3588S

VCCIO6_1V8 AJ34 — VCC_1V8_S0 — C1906 100nF X5R 10V C0201

VCCIO6_1 AL33, VCCIO6_2 AM33 — VCC_3V3_S0 — C1907 100nF X5R 10V C0201

VCC_3V3_S0 — R1914 2.2K 5% R0402 — I2C6_SCL_M3

VCC_3V3_S0 — R1915 2.2K 5% R0402 — I2C6_SDA_M3

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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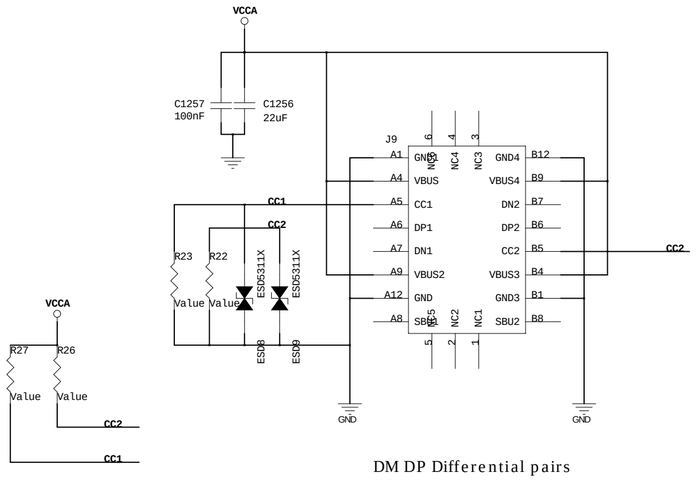
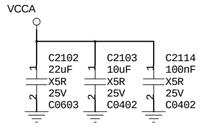
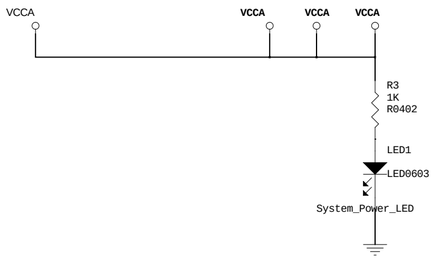
TPPE-C



DM DP Differential pairs
Z0= 90 ohm





LED0603
R0201

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PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1
VSEL4
VSEL5
PMIC_INT_L
PMIC_RESET_L
PWRON_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI

VCC_SYSIN
ED2200 AZ5825-01F ESD0402

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!

DO NOT DELETE IT!

Device Working Maximum Supply Voltage ≤5.5V
Recommended Supply Voltage 3.3V
Clamping Voltage@1A (8/20uS) ≤6.5V
Surge Current@(8/20uS) ≥1A
Reverse Stand-off Voltage ≥3.3V
Reverse Leakage Current@3.3V ≤1uA
Operating Temperature -55℃ ~ +125℃
Package DFN1006-2L
Equivalent to ESD0402 in same specifications

VSEL5 — R2242 0R — PMIC_PWR_CTRL2
VSEL4 — R2290 0R — PMIC_PWR_CTRL3

PMIC RK806-1 BUCK

U2200-A

BUCK5 2.5A	VCC5 44	SW5 45	VOUT5 46
BUCK1 6.5A	VCC1_1 52, VCC1_2 53	SW1_1 50, SW1_2 51	VOUT1 49
BUCK6 2.5A	VCC6 28	SW6 29	VOUT6 30
BUCK2 5A	VCC2_1 33, VCC2_2 34	SW2_1 35, SW2_2 36	VOUT2 37
BUCK9 2.5A	VCC9 1	SW9 68	VOUT9 67
BUCK3 5A	VCC3 54	SW3 55	VOUT3 56
BUCK8 2.5A	VCC8 7	SW8 6	VOUT8 5
BUCK4 5A	VCC4 22	SW4 23	VOUT4 24
BUCK10 2.5A	VCC10 27	SW10 26	VOUT10 25
BUCK7 2.5A	VCC7 43	SW7 42	VOUT7 41

FB5 (FB=0.5V) — FB1 (FB=0.5V) — FB6 (FB=0.5V) — FB2 (FB=0.5V) — FB9 (FB=0.5V)

RK806-1

VDD_DDR_S0 — Default:0.85V; Low frequency: 0.85V-->0.75V — Feedback from RK3588S
L2200 0.47uH IND_201610 — R2200 100R 5% R0402 — C9922 1uF X5R 10V C0402
C2202 22uF, C2203 22uF X5R 10V C0603, C0603

VDDQ_DDR_S0 — Default:0.6V — Feedback from RK3588S
L2204 0.47uH IND_201610 — R2236 20K 1% R0402 — C2229 100pF C0G 50V C0402 — R2241 100K 1% R0402
C2228 22uF, C2227 22uF X5R 10V C0603, C0603

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VDD2_DDR_S3 — Default:1.2V — Feedback from RK3588S
L2202 0.47uH IND_201610 — R2218 120K 1% R0402 — C2216 100pF C0G 50V C0402 — R2227 100K 1% R0402

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

VDD_GPU_S0 — Default:0.75V — Feedback from RK3588S
L2201 0.24uH IND_404020
C2209 1uF X5R 10V C0402, R2208 100R 5% R0402, C2210 47uF X5R 6.3V C0805, C2205 47uF X5R 6.3V C0805, C2280 22uF X5R 10V C0603

VDD_CPU_LIT_S0 — Default:0.75V — Feedback from RK3588S
L2203 0.24uH IND_252012
C2221 1uF X5R 10V C0402, R2219 100R 5% R0402, C2217 22uF X5R 10V C0603, C2218 22uF X5R 10V C0603, C2281 22uF X5R 10V C0603

VDD_LOGIC_S0 — Default:0.75V — Feedback from RK3588S
L2205 0.24uH IND_252012
C2230 1uF X5R 10V C0402, R2238 100R 5% R0402, C2231 22uF X5R 10V C0603, C2232 22uF X5R 10V C0603, C2282 22uF X5R 10V C0603

VDD_VDENC_S0 — Default:0.85V — Feedback from RK3588
L2207 0.24uH IND_252012
C2291 1uF X5R 10V C0402, R2209 100R 5% R0402, C2240 22uF X5R 10V C0603, C2237 22uF X5R 10V C0603, C2283 22uF X5R 10V C0603

VCC_2V0_PLDO_S3 — Default:2.0V — Feedback from RK3588
L2209 0.47uH IND_201610
C2244 22uF X5R 10V C0603, C2245 22uF X5R 10V C0603

VCC_1V8_S3 — Default:1.8V
L2208 0.47uH IND_201610
C2242 22uF, C2243 22uF X5R 10V C0603, C0603

VCC1V8_PMU_DDR_S3 — R2210 0R 5% DNP — R2211 0R 5%

VCC_SYSIN: C2200 22uF X5R 10V C0603; C2201 22uF 10V X5R C0805; C2213 22uF 10V X5R C0805; C2226 22uF 10V X5R C0603; C2236 22uF 10V X5R C0603; C2241 22uF X5R 10V C0603

PMIC RK806-1 Managerment

U2200-C

VCC_1V8_S3_PLDO6: C2248 1uF 10V X5R C0402

VCCIO
- (IIC/SPI)CS — PMIC_SPI_CS
- (SDA)MOSI — PMIC_SPI_MOSI
- (SCL)CLK — PMIC_SPI_CLK
- (PWRCTRL3)SO — PMIC_PWR_CTRL3
- PWRCTRL2 — PMIC_PWR_CTRL2
- PWRCTRL1 — SLEEP1_RESET1_DEVOFF1_VSEL1
- (M/S)EXT_EN — PMIC_EXT_EN_OUT
- INT — PMIC_INT_L
- RESETB — PMIC_RESET_L
- EPAD 69

PLDO6 200mA

VCCA: C2254 1uF X5R 10V C0402
- SYNC_CLK 3
- SYNC 2
- VDC 32
- PWRON 4

VBUS_TYPEC — R2264 39K 5% R0402; R2265 10K 5% R0402
PMIC_VDC — C2260 1nF C0G 25V C0402
PWRON_L — C2261 100nF X5R 16V C0402

VCC_1V8_S3: R2261 10K 5% R0402; R2263 10K 5% R0402
R2258 100K 5% R0402
C2262 100nF X5R 16V C0402

RK806-1

RK3588S: nPOR, TSADC_SHUT
RK806-1: RESETB
Reset Key

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200-B

VCC_2V0_PLDO_S3 — C2247 1uF X5R 10V C0402
VCC_SYSIN — C2252 1uF X5R 10V C0402
VCC_1V1_NLDO_S3 — C2257 1uF X5R 10V C0402
VCC_1V1_NLDO_S3 — C2264 1uF X5R 10V C0402

VCC11 59	0.5A	PLDO1	60	VCC_1V8_S0	Default:1.8V
	0.3A	PLDO2	58	VCCA_1V8_S0	Default:1.8V
	0.3A	PLDO3	57	VDDA_1V2_S0	Default:1.2V
VCC12 64	0.5A	PLDO4	63	VCCA_3V3_S0	Default:3.3V
	0.3A	PLDO5	65	VCCIO_SD_S0	Default:3.3V
PLDO					
VCC13 13	0.3A	NLDO1	14	VDD_0V75_S3	Default:0.75V
	0.3A	NLDO2	12	VDDA_DDR_PLL_S0	Default:0.85V; Low frequency:0.85V-->0.75V
	0.5A	NLDO3	11	VDDA_0V75_S0	Default:0.75V
VCC14 9	0.5A	NLDO4	10	VDDA_0V85_S0	Default:0.85V
	0.3A	NLDO5	8	C2265 2.2uF	Default:0.75V Reserved
NLDO					

C2246 1uF, C2249 1uF, C2250 1uF, C2251 1uF, C2253 1uF, C2255 2.2uF, C2258 2.2uF, C2259 2.2uF, C2263 2.2uF, C2265 2.2uF — 10V C0402 X5R

VCCA_1V8_S0 — R2274 0R 5% R0402 — AVDD1V8_DDR_PLL_S0 — C2290 1uF X5R 10V C0402

RK806-1

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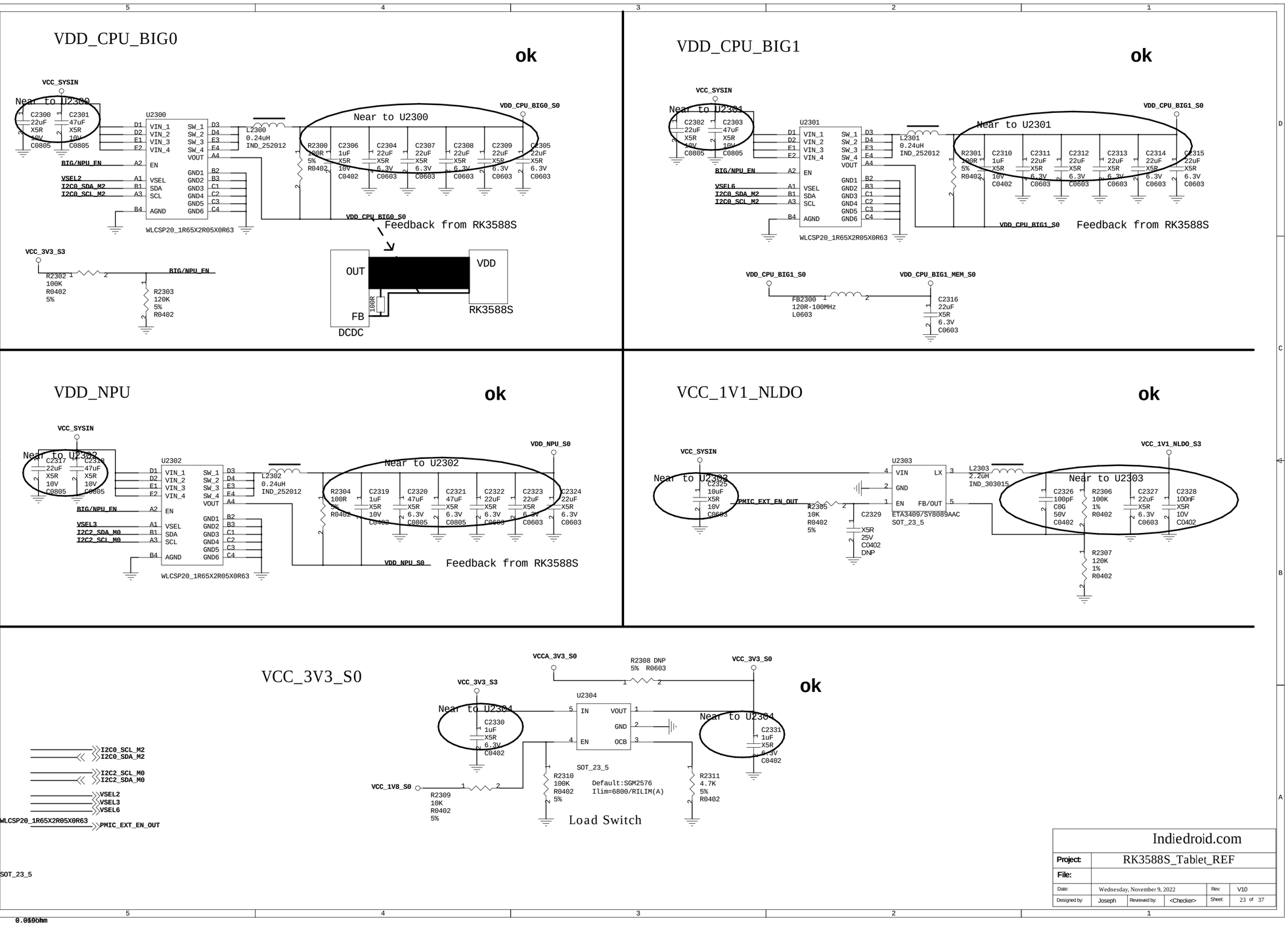
ESD0402



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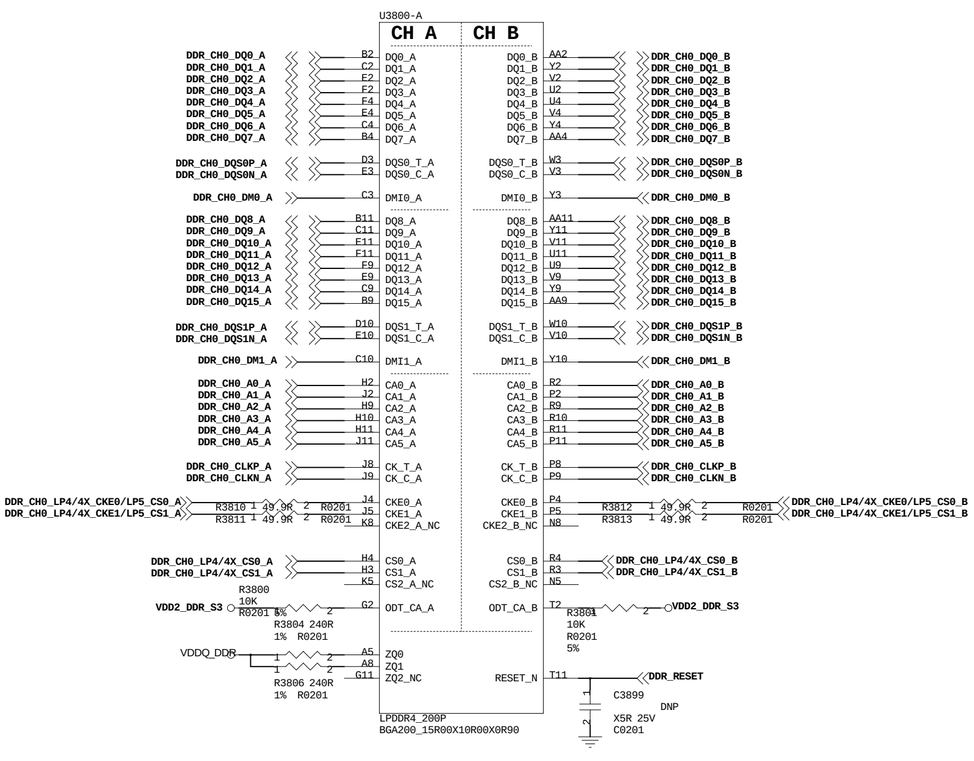
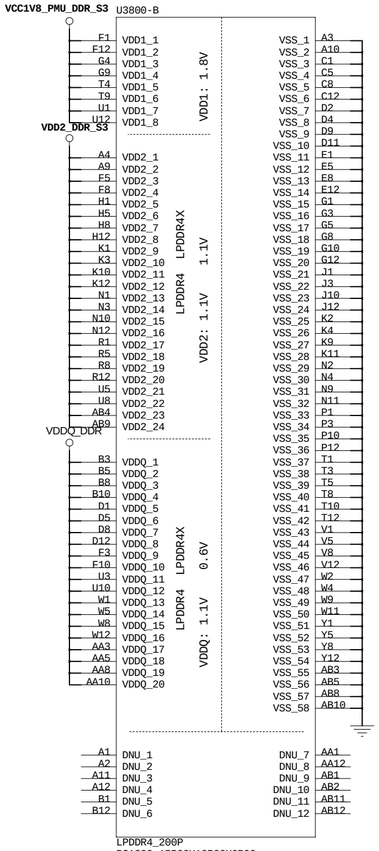
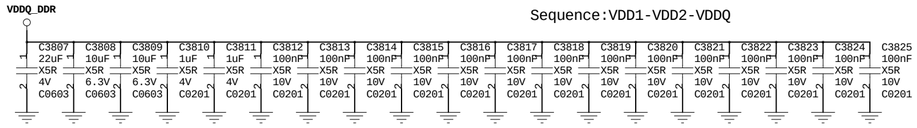
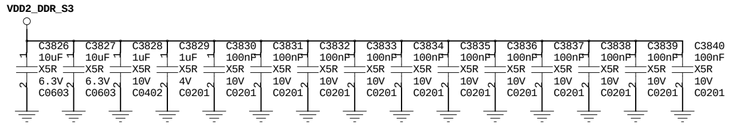
DRAM-LPDDR4/4x_2X32bit



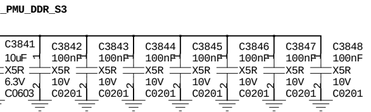


Sequence:VDD1-VDD2-VDDQ



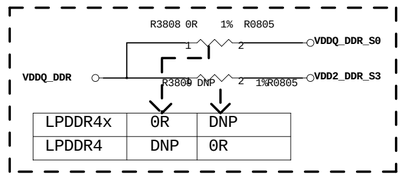


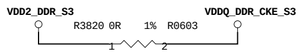
For U3800

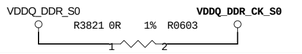


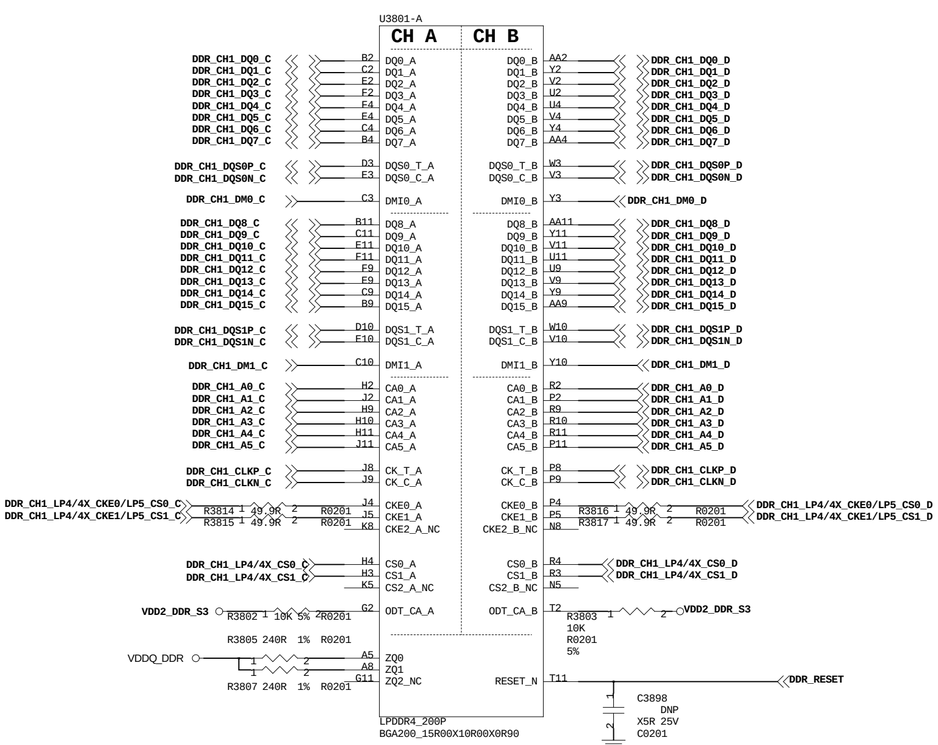
Sequence:VDD1-VDD2-VDDQ

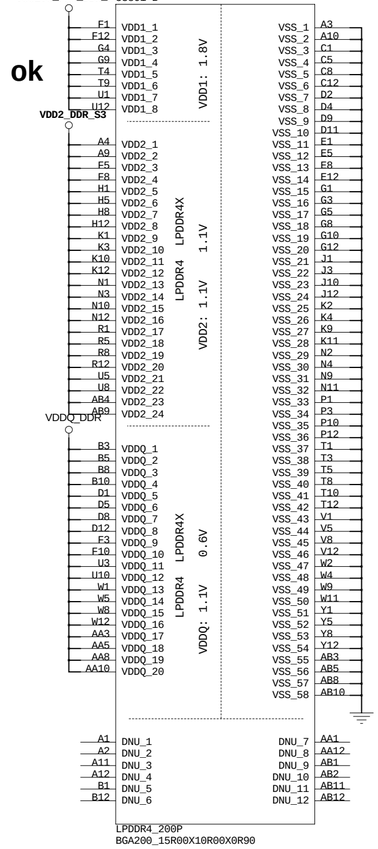
LPDDR4 LPDDR4X
VDD1: 1.70-1.95 1.70-1.95
VDD2: 1.06-1.17 1.06-1.17
VDDQ: 1.06-1.17 0.57-0.65











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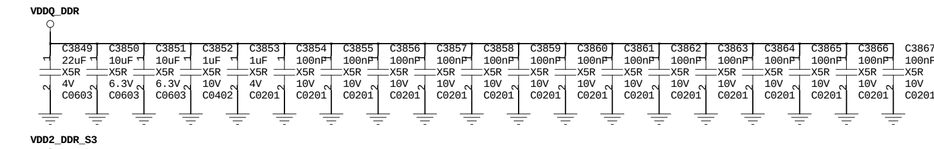
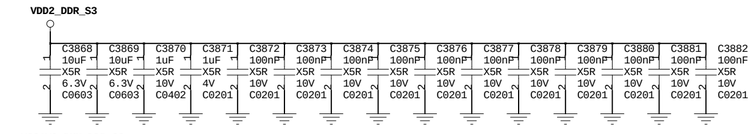
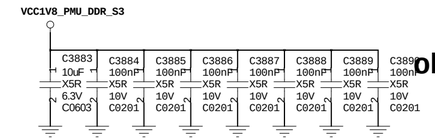




For U3801



ok

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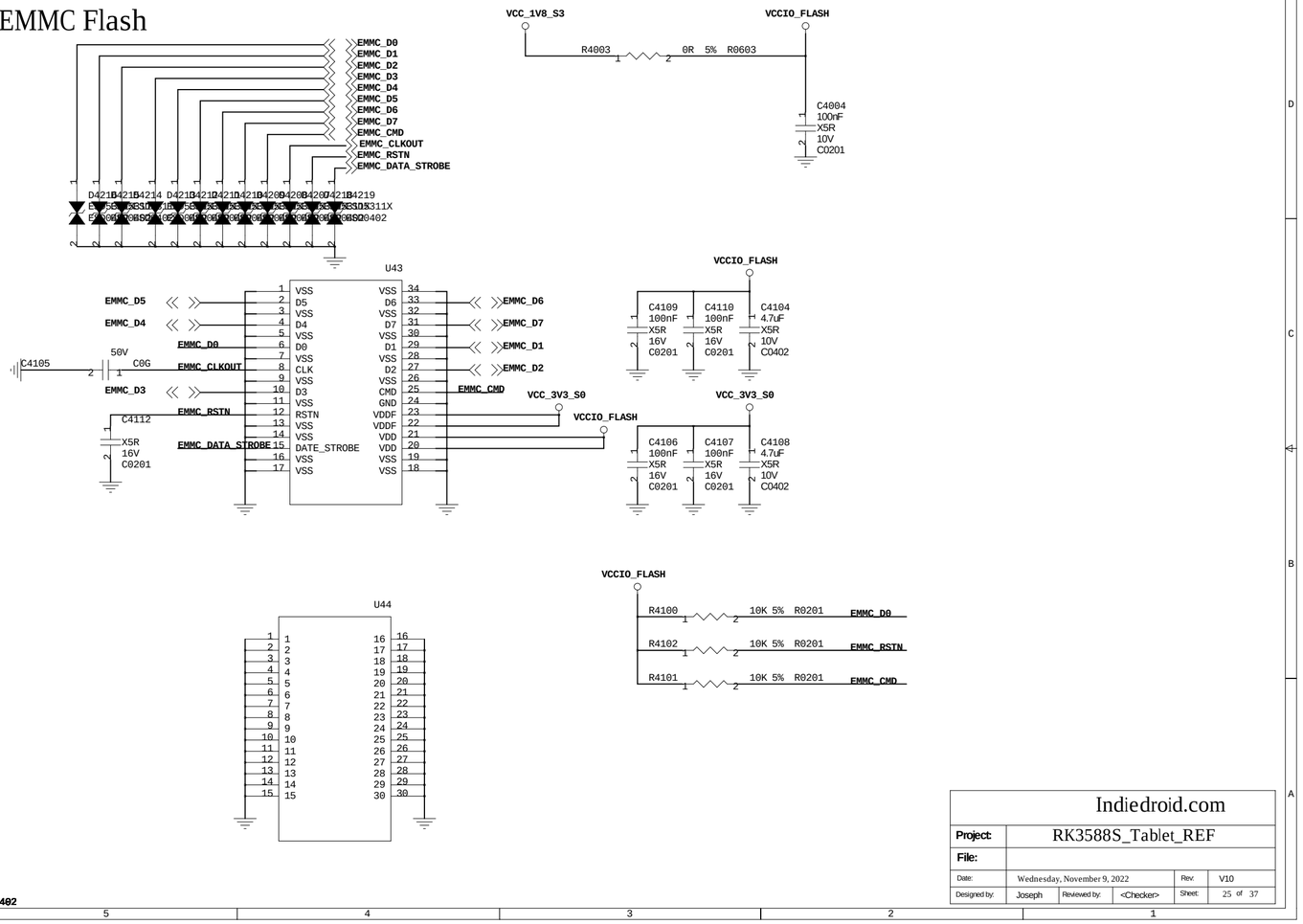
EMMC Flash



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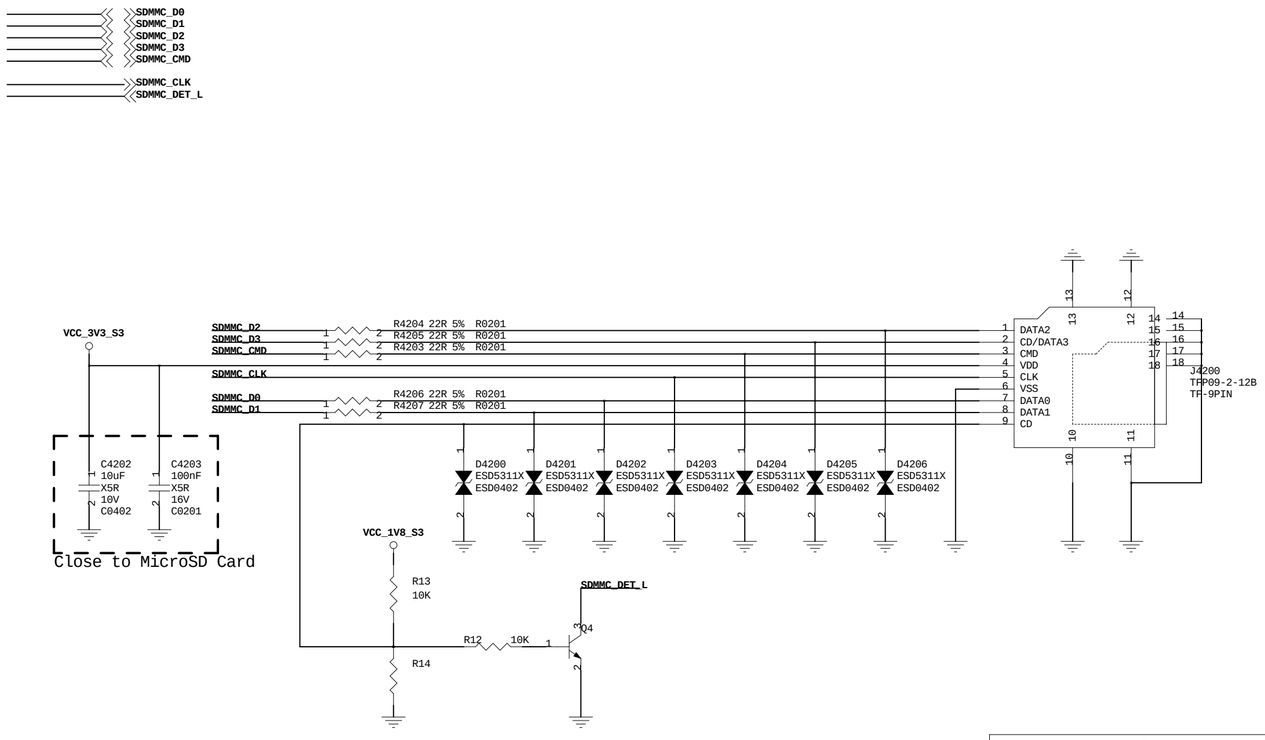
MicroSD Card



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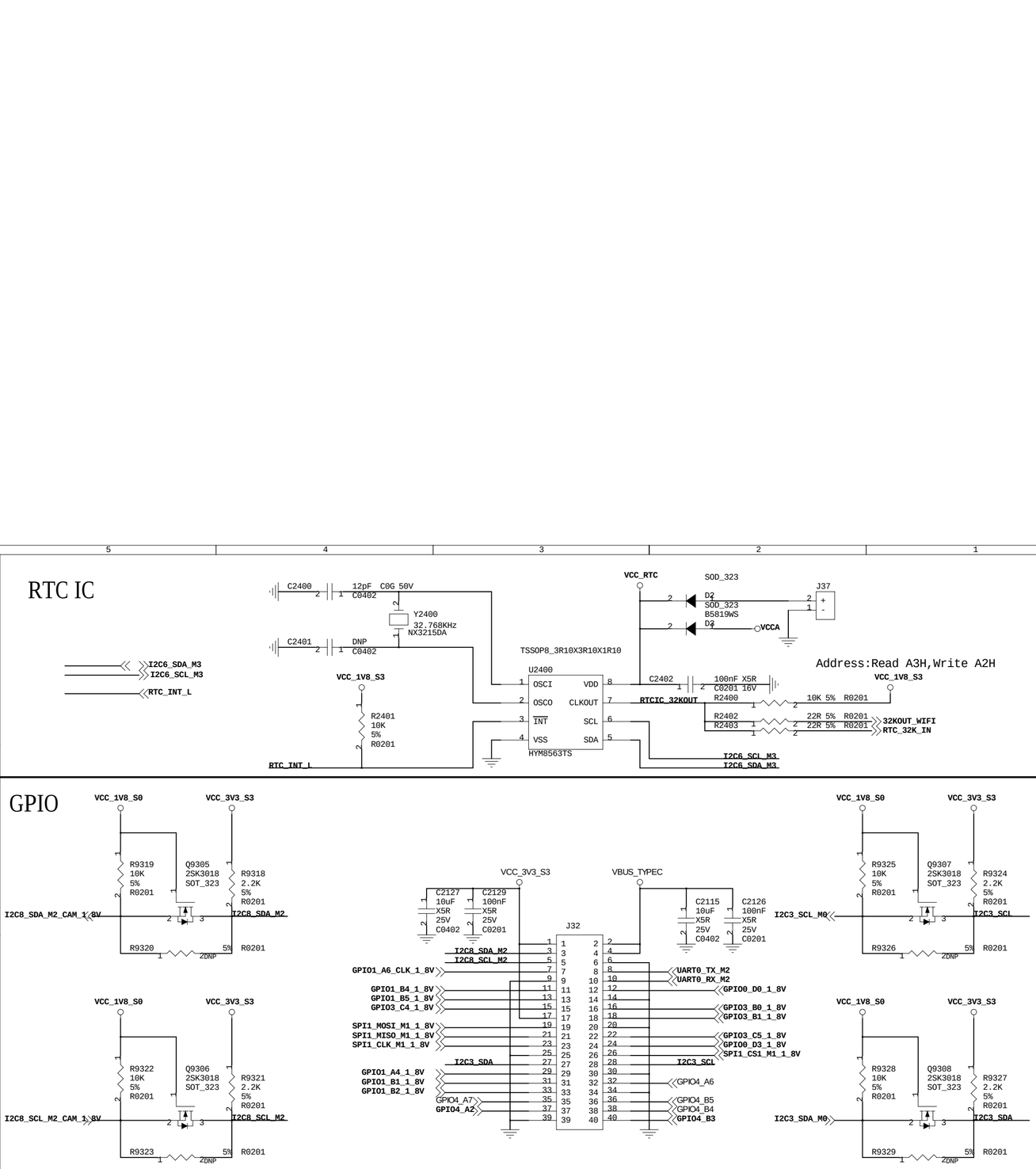
ESD0402

RTC IC

GPIO



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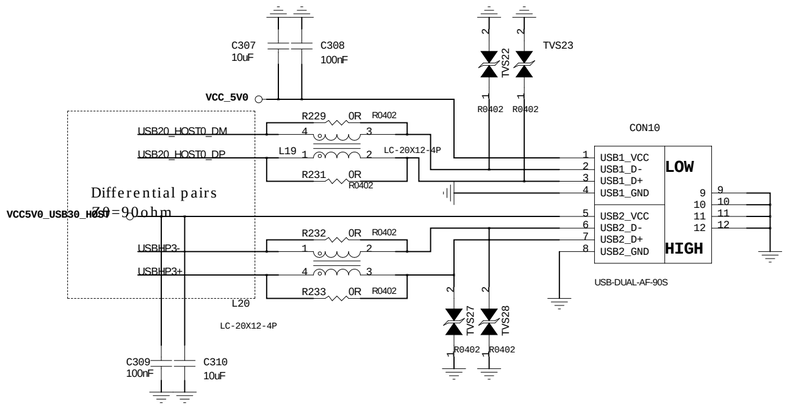
SOD_323

SOT_323

USB2.0 HOST

USB20_HOST0_DP
USB20_HOST0_DM

USBHP3+
USBHP3-



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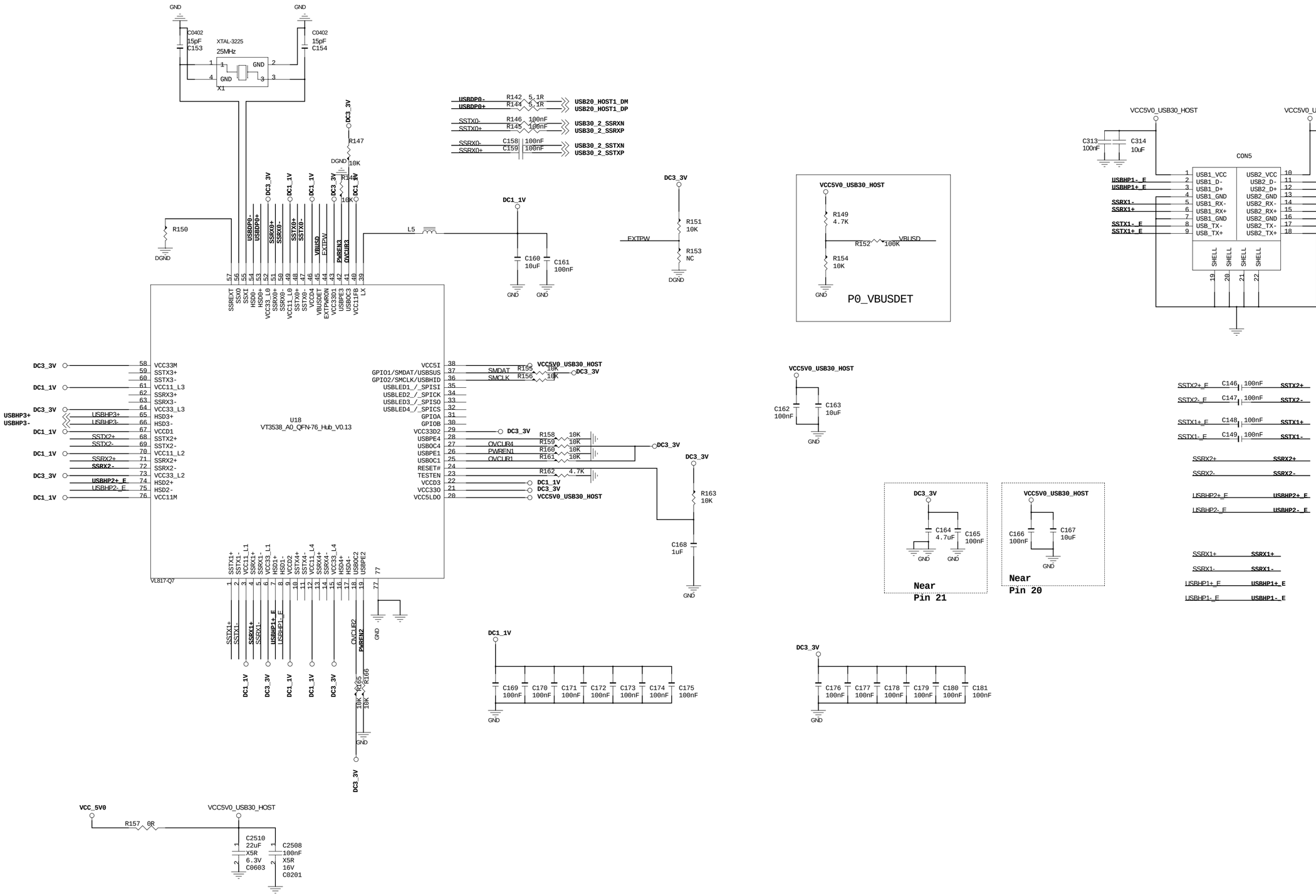
USB3.0 HOST



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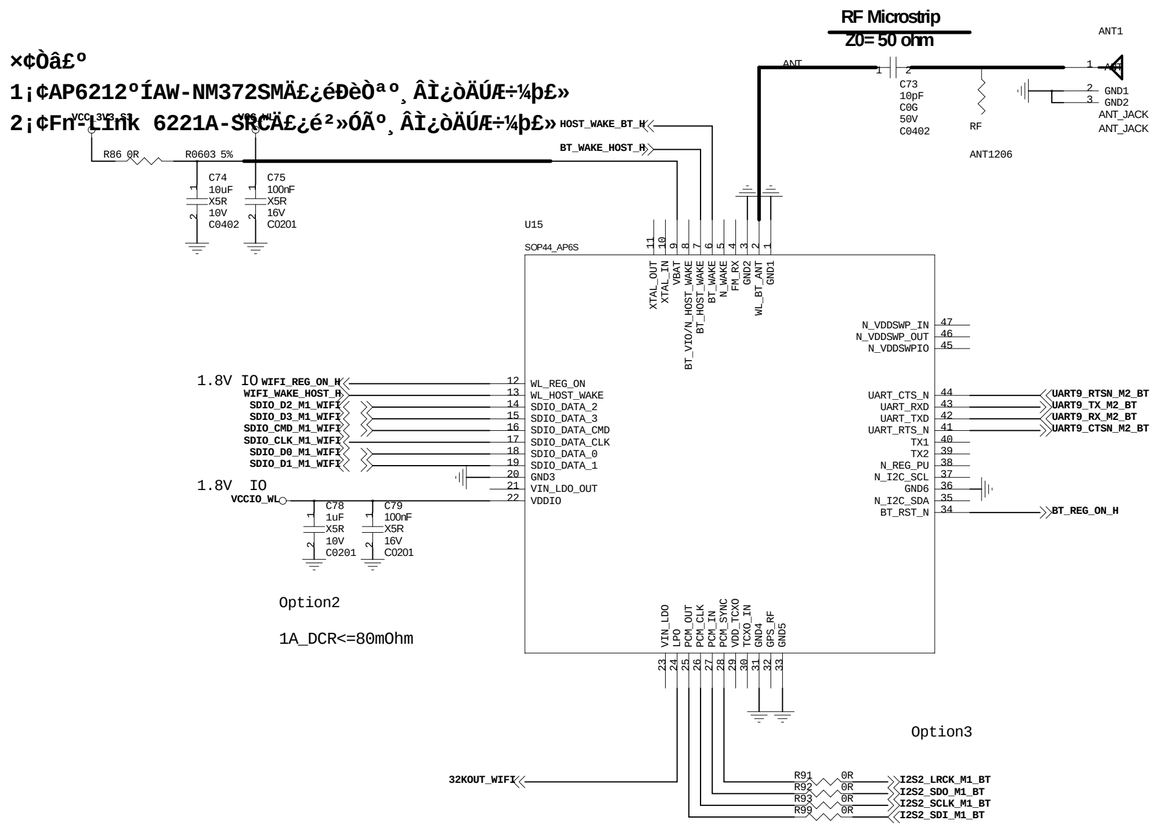
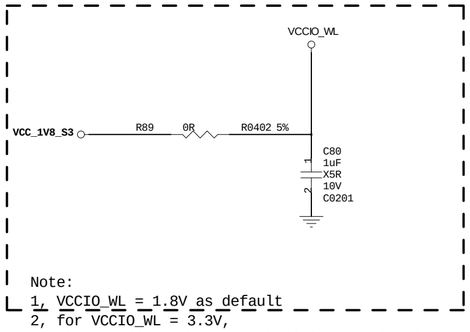
SDIO WIFI/BT Module-1T1R





Note:
1, VCCIO_WL = 1.8V as default
2, for VCCIO_WL = 3.3V,
please adjust the control IOs' power level

Note:
Yes: ~~option circuit be mounted~~

No: option circuit not be mounted OPTION	WIFI a	WIFI b/g/n	WIFI ac	WIFI 5GHz	BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0	No
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No@SDIO3.0 No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0	No
RTL8189ETV	No	Yes	No	No	No	Module	1.8-3.3V	No	No	No@SDIO3.0 No	No
Module F89FTSM12-W3 RTL8723DS	No	Yes	No	No	4.2	Integrated Module	1.62-3.6V	No	No	No	Yes
Module 6223A-SRD RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Integrated Module Integrated	1.7-3.45V	No	No	No	No

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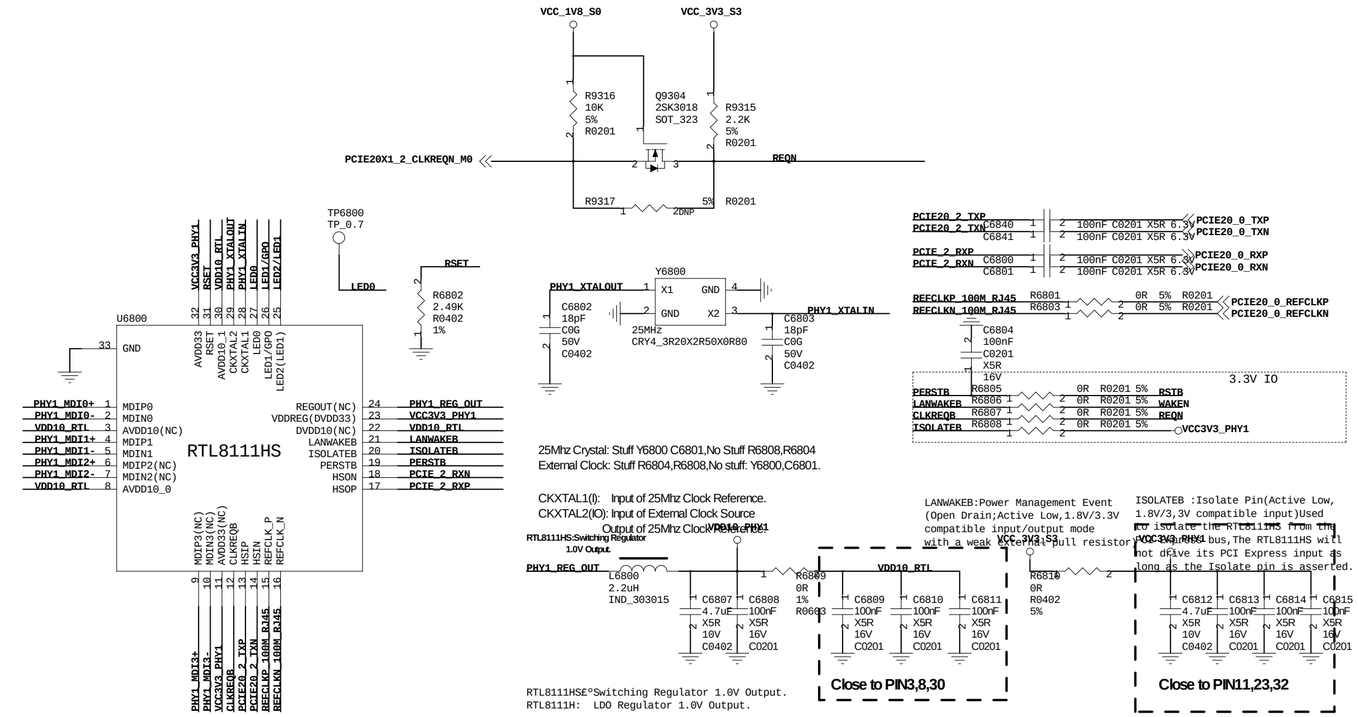
PCIE TO RJ45



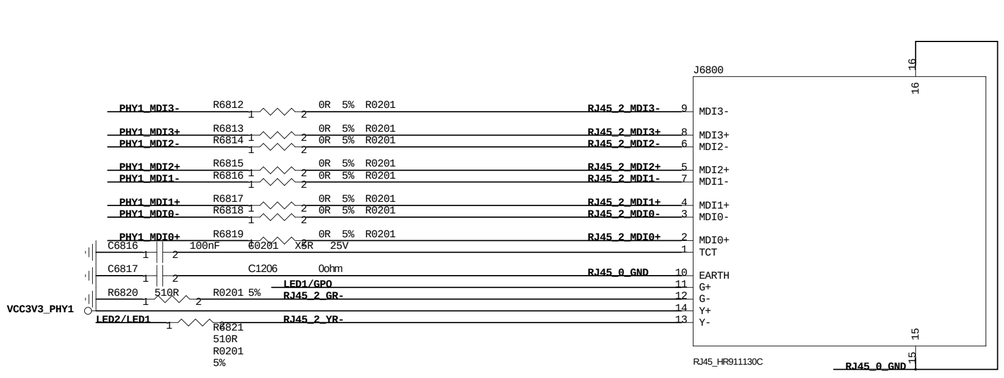
25Mhz Crystal: Stuff Y6800 C6801,No Stuff R6808,R6804
External Clock: Stuff R6804,R6808,No stuff: Y6800,C6801.

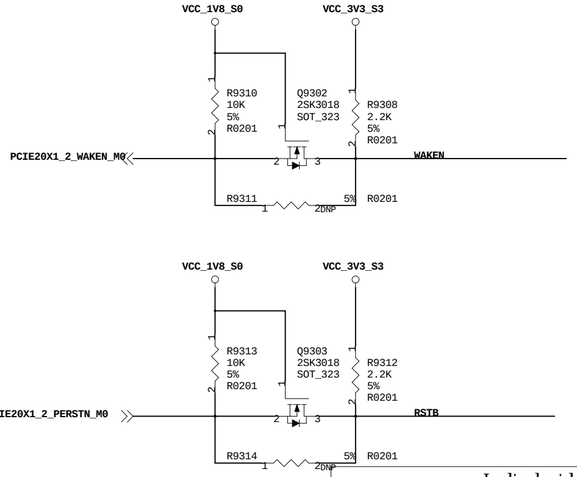
CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference

LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor on VCC3V3_PHY1 bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus.

RTL8111HS:Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.





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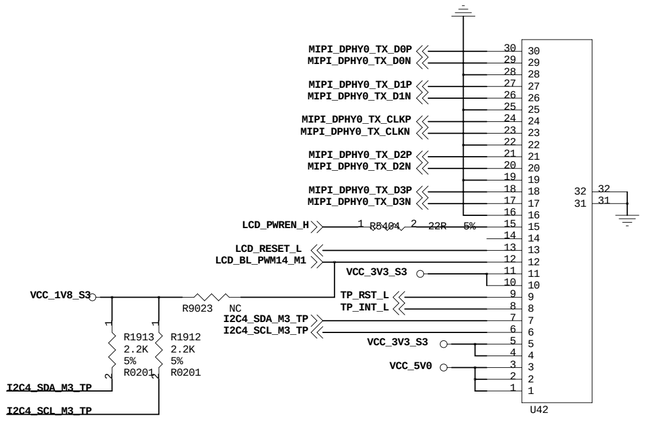
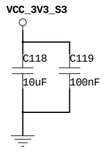
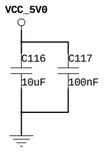
CRY4_3R20X2R50X0R80

0.80.0.23

Single-MIPI LCM(MIPI DPHY0 TX)







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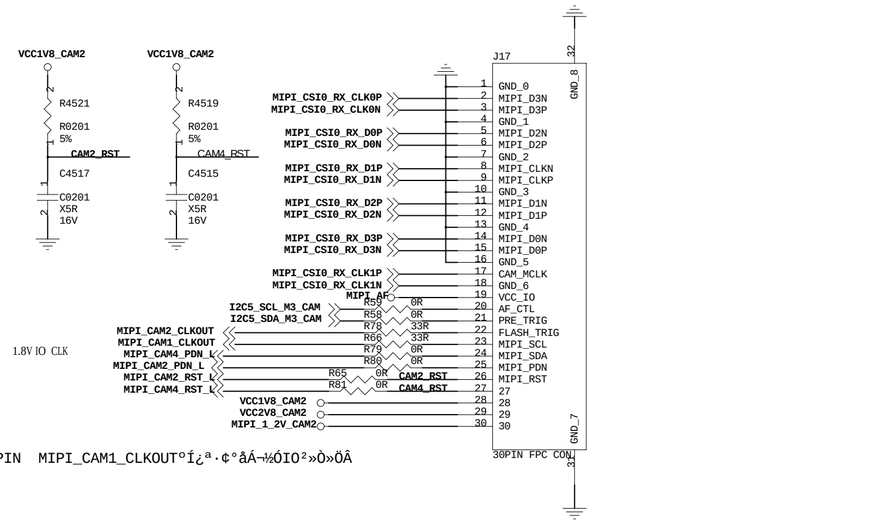
MIPI-DPHY0_RX

Rear Camera



1.8V IO CLK

23PIN MIPI_CAM1_CLKOUT°Í¿ª·¢°åÁ¬½ÓIO²»Ò»ÖÂ

Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

Note:

According to camera model,
DCDC power supply is
recommended
if the DVDD current
Below 100mA

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HDMI2.1 TX0

HDMI0_TX0P
HDMI0_TX0N
HDMI0_TX1P
HDMI0_TX1N
HDMI0_TX2P
HDMI0_TX2N
HDMI0_TX3P
HDMI0_TX3N

HDMI0_TX_SBDP
HDMI0_TX_SBDN

HDMI_TX0_SCL_M0
HDMI_TX0_SDA_M0
HDMI_TX0_CEC_M0
HDMI_TX0_HPD_M0

HDMI0_TX_ON_H

U5000 ESD73034D
SON10_2R50X1R00X0R50

Cj<=0.2pF

HDMI0_TX2P	C5000	220nF X5R 10V C0201	HDMI0_TX2P_PORT	IO1 / NC_10	HDMI0_TX2P_PORT
HDMI0_TX2N	C5001	220nF X5R 10V C0201	HDMI0_TX2N_PORT	IO2 / NC_9	HDMI0_TX2N_PORT
HDMI0_TX1P	C5002	220nF X5R 10V C0201	HDMI0_TX1P_PORT	GND / GND	HDMI0_TX1P_PORT
HDMI0_TX1N	C5003	220nF X5R 10V C0201	HDMI0_TX1N_PORT	IO3 / NC_7	HDMI0_TX1N_PORT
HDMI0_TX0P	C5004	220nF X5R 10V C0201	HDMI0_TX0P_PORT	IO4 / NC_6	HDMI0_TX0P_PORT
HDMI0_TX0N	C5005	220nF X5R 10V C0201	HDMI0_TX0N_PORT		HDMI0_TX0N_PORT
HDMI0_TX3P	C5006	220nF X5R 10V C0201	HDMI0_TX3P_PORT		HDMI0_TX3P_PORT
HDMI0_TX3N	C5007	220nF X5R 10V C0201	HDMI0_TX3N_PORT		HDMI0_TX3N_PORT

U5001 ESD73034D
SON10_2R50X1R00X0R50

HDMI0_TX_CEC_PORT
HDMI0_TX_SCL_PORT
HDMI0_TX_SDA_PORT

HDMI0_SBDP
HDMI0_SBDN

VCC5V_HDMI_TX0

ED5005 ESD5311X ESD0402
ED5000 ESD5311X ESD0402
ED5001 ESD5311X ESD0402
ED5002 ESD5311X ESD0402
ED5003 ESD5311X ESD0402

C5008 1uF X5R 10V C0201

1	HPD				
2	UTILITY				
3	D2P				
4	D2_GND				
5	D2N				
6	D1P				
7	D1_GND				
8	D1N				
9	D0P				
10	D0_GND				
11	D0N				
12	CLKP				
13	CLK_GND				
14	CLKN				
15	CEC				
16	DDC/CEC_GND				
17	SCL				
18	SDA				
19	5V_POWER				
20		G1			
21		G2			
22		G3			
23		G4			

J5000
MICROHDMI-2

Note:

This reference circuit use TYPE C by default
If the project needs TYPE A, you must replace the library with TYPE A.

HDMI TX DDC

VCC_5V0
VCC_3V3_S0

D5001 B5819WS SOD_323

R5000 10K 5% R0402
Q5000 2SK3018 SOT_323
R5001 1.8K 5% R0402

HDMI_TX0_SCL_M0 — HDMI0_TX_SCL_PORT

R5002 10K 5% R0402
R5003 1K 5% R0402
C5011 100pF C0G 50V C0402
Q5001 2SK3018 SOT_323
R5012 1.8K 5% R0402

HDMI_TX0_SDA_M0 — HDMI0_TX_SDA_PORT

HDMI TX CEC

VCC_3V3_S0 VCC_5V0

R5017 27K 5% R0402
Q5008 2SK3018 SOT_323

HDMI_TX0_CEC_M0 — HDMI0_TX_CEC_PORT

VCC_5V0 — D5000 B5819W SOD_123 — VCC5V_HDMI_TX0

HDMI0_TX0P_PORT
HDMI0_TX0N_PORT
HDMI0_TX1P_PORT
HDMI0_TX1N_PORT
HDMI0_TX2P_PORT
HDMI0_TX2N_PORT
HDMI0_TX3P_PORT
HDMI0_TX3N_PORT

R5004 R5005 R5006 R5007 R5008 R5009 R5010 R5011
1% R0201

Q5002 WNM6002-3/TR SOT_323
Q5003 WNM6002-3/TR SOT_323
Q5004 WNM6002-3/TR SOT_323
Q5005 WNM6002-3/TR SOT_323

HDMI0_TX_ON_H

Rds=1.7ohm/2.6V
Coss=7.33pf

Note:

The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

HDMI0_TX_SBDP — C5009 1uF X5R 10V C0402 — HDMI0_SBDP
HDMI0_TX_SBDN — C5010 1uF X5R 10V C0402 — HDMI0_SBDN

VCC_1V8_S0

R5013 47K R0402 5%
R5014 47K R0402 5%

HDMI_TX0_HPD_M0

Q5006 2SK3018 SOT_323
Q5007 2SK3018 SOT_323

2.4-5.3V

R5015 1.2K R0402 5%
R5016 47K R0402 5%

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Reviewed by:	<Checker>
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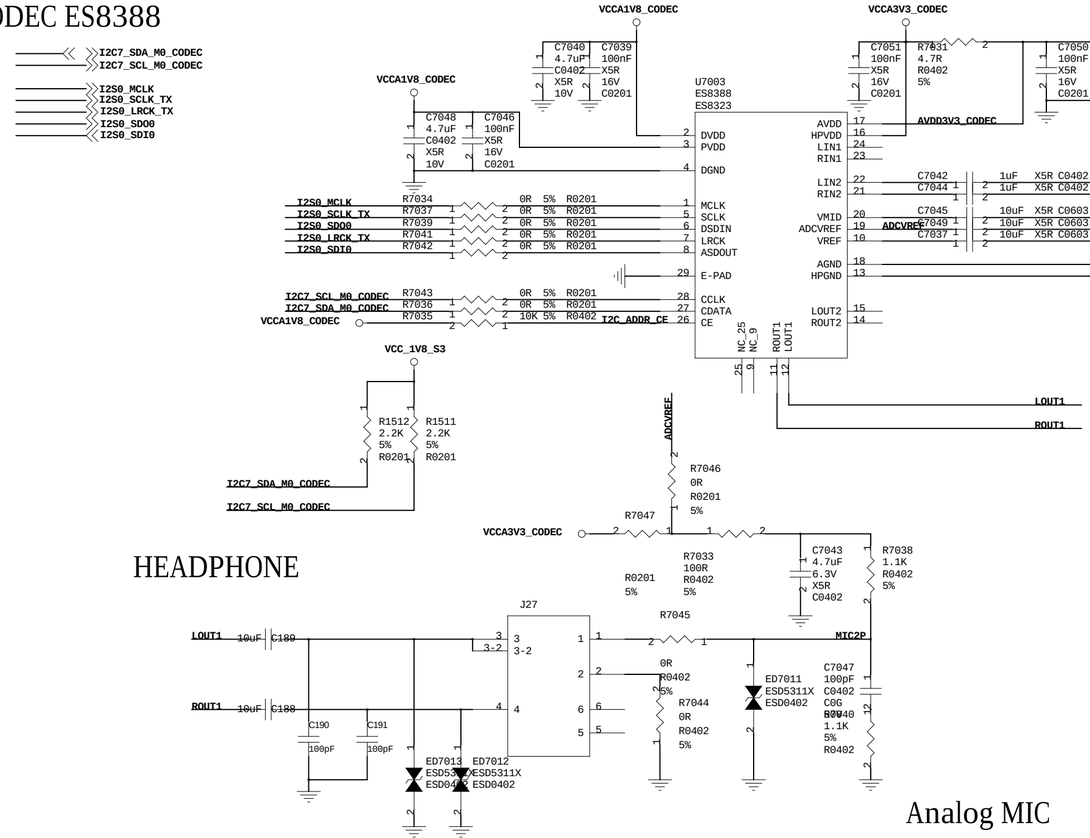
ESD0402
SOD_323
SOT_323

CODEC ES8388



ES8323

ESD0402

Indiedroid.com					
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UART Debug

UART2_RX_M0 — UART2_RX_M0

UART2_TX_M0 — UART2_TX_M0

J5 1

J6 1

J3 1

J4 1

KEY

PWRON_L — SW5 — ED9201 ESD5311X — ESD0402

RESET_L — SW6 — ED9204 ESD5311X — ESD0402

SARADC_VIN0_BOOT — SW7 — ED9205 ESD5311X — ESD0402

SARADC_VIN1_KEY/RECOVERY — R176 10K — VCC_1V8_S3; R177 100R SW1; D28 ESD5311X

Note:

If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

VCC_3V3_S3

UART2_RX_M0 — R9300 100R 5% R0201

UART2_TX_M0 — R9301 100R 5% R0201

J11

D9300 ESD5311X ESD0402

D9301 ESD5311X ESD0402

ESD0402

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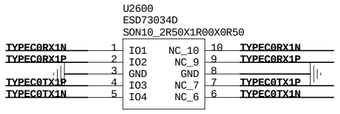
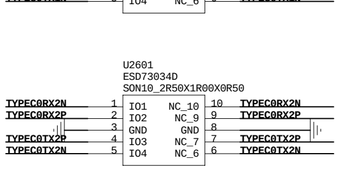
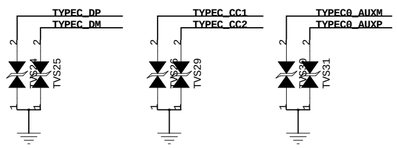
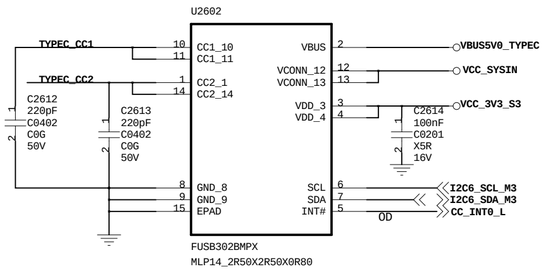
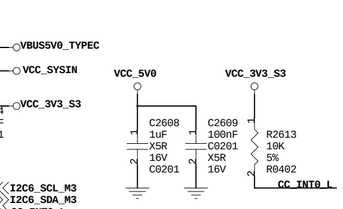
Type-C PORT

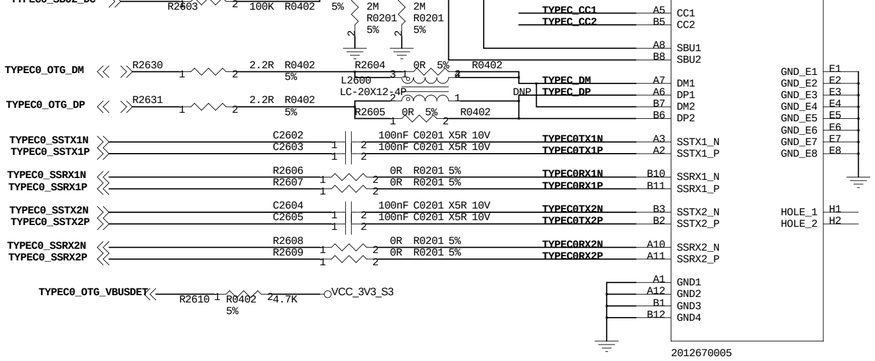


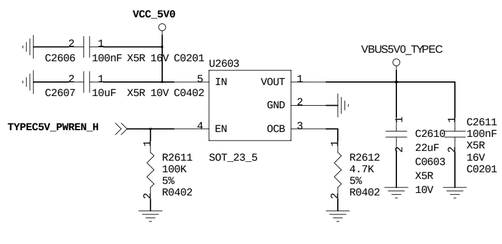












TYPEC3.1_GD-TC-002-03

MLP14_2R50X2R50X0R80

SOT_23_5

LC-20X12-4P

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