5. Compilation (Incomplete)

Makefiles

Makefiles consist of a sequence of rules specifying the target, i.e. the file to be constructed, the dependencies, and the recipe, i.e. the list of commands required to create the target. The recipe is executed if either the target doesn't exist ot one or more of the dependencies are newer than the target.

```
target: dependency_1 dependeny_2...
        recipe
```

The command `make` is used to run the Makefile. If no command line arguments are passed, only the first rule will be evaluated. However, if a command line argument is passed, then it will evaluate the rule for that target. If the rule contains dependencies and the dependencies are also targets in the Makefile, then those rules will be evaluated first.

Makefiles also support name wildcards and variables.

More information can be found here