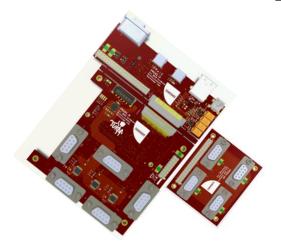
Sundance Multiprocessor Technology Limited PCIe/104 OneBank ARM+FPGA+FMC Carrier

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VITA57.1 FMC[™]-LPC I/O Module w. ADCs/DACs + USB3.0 ports



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0.3	Applied changes	19/03/2018	PM
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1 Introduction

This document describes the hardware features and some operational details of the FM191-RUA1 I/O Module. The FM191-RUA1 has a VITA57.1 FMC-LPC connector and follow the electronics specification and recommendation of the standard but is **NOT** form-factor compatible and will **NOT** fit all FMC carriers. Two versions are available. The FM191-R main features are a daughter card which provides 5V-TTL-compatible Analogue and Digital GPIOs that are suitable for robotics, motors and sensor application. The FM191-U is an expansion board which can be added to the FM191-R for delivering 4-port USB3.0 (2x USB type C, 1x IP67 USB Type C and 1x USB Type A) connectivity and more I/O pins on a 40-way header that follows Raspberry-PI pin-out. The additional board FM191-A1 provides easy connections to interface the 40 pin GPIO header.

The FM191-RUA1 is 100% compatible with the EMC²-xxxx PCIe/104 OneBank board that has different FPGAs SoM (System-on-Modules) from Xilinx or Microsemi. FM191-RUA1 does not have any PC/104 compatible bus interfaces, like PCIe or PCI. The FM191-RUA1 can safely be used with ANY carrier board that has a FMC connector, either directly onto the connector or via Samtec SeaRay cable, as long as it supports 1.8V Standards. No power is derived from the carrier and power has to be connected to the FM191-RUA1 with a suitable power-cable (supplied)

1.1 Main Features

1.1.1 Hardware

The FM191-R board is designed to fan out the FMC-LPC connector parallel I/Os and high-speed SerDes to five DB9 connectors and one SEIC connector.

The FM191-R was specially designed for the Sundance EMC² and other FPGA systems that have available a VITA57.1 FMC-LPC interface, for robotic/mobile applications.

The FM191-R provides connectivity to a wide range of 5V TTL sensors/actuators which are exposed to vibrations accessible via 5x DB9 connectors.

The FM191-U provides 4x USB3.0 ports(2x USB type C, 1x IP67 USB Type C and 1x USB Type A) for interfacing with high-speed sensors (e.g. depth sensors) or external storage (HDD/SSD) devices and provides 28 digital I/Os accessible via one 40-pin General Propose Input Output (GPIOs) connector.

The FM191-A1 fans-out the digital 40-pin GPIO I/Os from the FM191-U to 4x DB9 connectors.

1.1.2 Common Features

The common features of the FM191-RUA1 are:

- FMC LPC connector with I/O and single high-speed serial.
- Single +5 and +3.3V (external ATX connector) for powering external sensors via the DB9 connectors.
- 100-way SEIC peripheral interface connector.
- 15x single-ended digital I/Os 5V TTL are accessible via 3x DB9 (P3-P5).
- 12x analogue Inputs 5V TTL, with a resolution of 24-bits@2kSPS via 2x DB9 (P1-P2).
- 8x analogue Outputs 5V TTL, with a resolution of 12-bits via 2x DB9 (P2 and P5).

- 4x USB3.0 connections (2x USB type C, 1x IP67 USB Type C and 1x USB Type A) and 28x single-ended digital I/Os 5V TTL 40-pin GPIO connectors available via the expansion FM191-U board.
- 28x single-ended digital I/Os 5V TTL accessible 4x DB9 (P6-P9) via the expansion board FM191-A1
- 4x DB9 connectors (P6-P9) to interface the 40 pin GPIO header via the expansion FM191-A1 board.

1.2 Notes

Several part numbers are described in the text, as Hyperlinks. These are possible part numbers, and alternative devices may be designed in at a later date. Hyperlinks will provide access to external sites for more details.

2 Related Documents

2.1 Referenced Documents

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Abbreviations / Definitions

ADC Analog to Digital Converter

DAC Digital to Analogue Converter

EEPROM Also called E²PROM (or just E²). Electrically erasable and programmable ROM.

FPGA Field Programmable Gate Array.

GPIO General Purpose Input Output.

I²C Inter-integrated Circuit. A two wire low speed serial interface.

SEIC Sundance External Interface Connector.

SPI Serial Peripheral Interface

3.2 Definitions

4 Functional Description

4.1 Block Diagram

The FM191-RUA1 system is composed of 3 boards, namely, the FM191-R, FM191-U and FM191-A1. Figure 1 shows a representation of the FM191-RUA1 board.

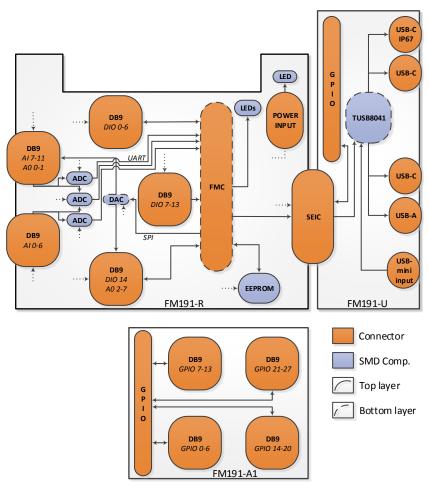


Figure 1: FM191-RUA1 block diagram

4.2 Module Description

The main connectors of the FM191-R (Figure 1) are the 5x DB9 connectors (P1-P5). DB9 connectors were chosen because of their reliability, low-price and mechanic locking which is desirable in applications exposed to high level of vibrations.

Supplied by external 5V, the DIOs are shifted down to 1.8V before the FMC interface.

Similarly, both ADC outputs to the FMC and DAC inputs from the FMC are under 1.8V, shifted from 5V (ADC) and to 5V (DAC). These 5V are independent from both converters and managed from two regulators which take external 12V.

The FMC connector not only interacts with the DB9s providing I/Os flexibility, but also supplying to the SEIC connector FMC-JTAG, FMC-I2C and some differential pairs. These features are not connected in FM191-U, but are present for other possible expansions in the future. Also, the pinout of the SEIC connector is compatible with the expansion board of EMC2-DP, which means that any I2C device in it could be used (HDMI). Equally, FM191-U can be used with EMC2-DP, having UART available at the GPIO header.

Apart from those signals, USB3.0 and GPIO are interconnected from the FMC.

The FM191-U is plugged via the SEIC connector and provides 4x USB3.0 ports - type C. Please note that this expansion board is **NOT COMPATIBLE** with the USB3.1. A 40-pin GPIO (compatible with the Raspberry PI V3) is also available and can be used to provide connectivity to a wide range of R-PI/Arduino shields. The 40-pin and DB9

connectors can provides up to 5V@2A (protected by an independent fuse) powered by the FM191-R.

The user may opt to use EMC2-DPV2 with FM191-U. **WARNING**: Please contact Sundance before attempting to connect the FM191-U to the EMC2-DPV2.

Users must be aware of the following when connecting the FM191-R to the EMC2-DPV2:

- The GPIO signals are 1.8V TTL, and therefore, injecting 5V TTL to any digital I/O would damage the FPGA module on the EMC2-DPV2;
- The USB3 chip is powered using 5V, which is not provided by the EMC2-DPV2 to the FM191-U.

These 2 issues can be solved using the jumpers J9 (1.8V) and J8 (5V) are available at FM191-U. **NOTE**: that 5V must be externally supplied via J8 or the USB3.0 will not work.

The FM191-A1 fans-out the 28x digital I/Os available on the FM191-U to 4x DB9 (P6-P9). This board was designed for providing an high flexibility to users and therefore the FM191-A1 can be connected to the FM191-U using any of the connection types shown in Figure 2 to Figure 5:



Figure 2: Standard flat 40-pin IDE PATA cable



Figure 3: Round 40-pin IDE PATA cable

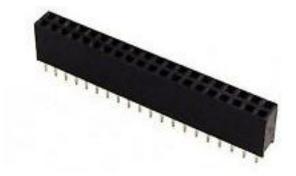


Figure 4: Stacked up by replacing 40-pin male by a female connector



Figure 5: Stacked up by soldering the FM191-A1 to FM191-U using long 40-pin male connector.

Please contact Sundance to select the best stack up configuration for the target application.

4.3 Interface Description

4.3.1 Mechanical Interface

4.3.1.1 External Power Supply connector

The FM191-R is powered directly from an external power source via J1 connector (ERNI 254831).

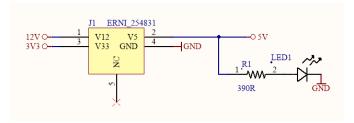


Figure 6: Schematics of the power connector.

4.3.1.2 SEIC Connector

The FM191-U is plugged to the FM191-R via the SEIC connector. One Samtec's <u>LSHM-150-01-L-DH-A-S-TR</u> is used in the FM191-R and one <u>LSHM-150-01-L-RH-A-S-TR</u> is used in the FM191-U. All the remaining pins in the FMC are routed to the SEIC connector, increasing the flexibility and enabling the possibility of creating future SEIC boards. Figure 7 shows the pin-map of the SEIC connectors for both boards.

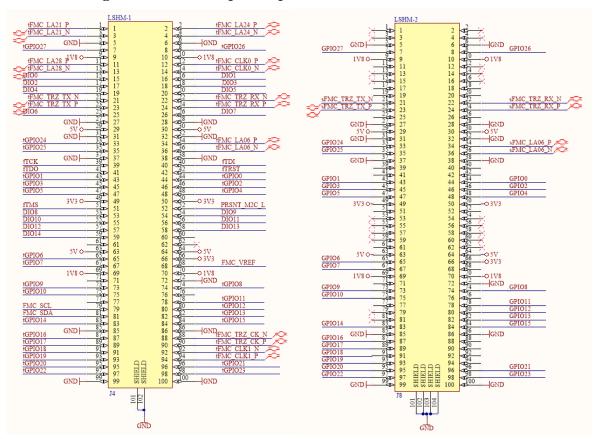


Figure 7: SEIC pin map in the FM191-R (left) and FM191-U (right)

4.3.1.3 USB connectors

4.3.2 Electrical Interface

4.3.2.1 Local and external Power Supplies

One MAX8556 DC-DC step-down converter (FM191-R) is used to create the local voltage of 1.8V@4A and one LM3674 to create the local voltage of 1.1V@0.6A.

The FM191-R must be powered (5V@14A and 3.3V@5A) by an external power source unit (e.g the <u>DCX6.360</u>) supply via the J1 5-pin power connector. External sensors and actuators can be powered via the DB9 (5V@2A per connector) and 40-pin (2-pins at 5V@2A and 2-pins 3.3V@2A) connectors.

ADCs and DAC are supplied with independent 5V each, from linear regulators (<u>LP4951C</u>) supplied with 12V input.

4.3.2.2 Level shifters

Seven TI <u>TXS0108E</u> are used for converting from 1.8V TTL single-ended I/Os to 5V. All the level shifters on the FM191-R.

4.3.2.3 I2C EEPROM

A 512x8bits ST M24C04-F EEPROM is available for storage small amounts of data which can programmed via the I²C bus (Figure 8). This device can be used to store operating parameters separate from the configuration Flash (e.g. Serial Number).

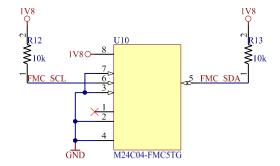


Figure 8: Schematics of the M24C04 EEPROM.

4.3.2.4 LEDs

LED 1 for sensing power from the ATX and 4 user LEDS (LED2-5) which can be freely configured by the user (Figure 9).

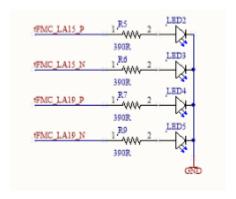


Figure 9: User LEDs

4.3.2.5 4-Port USB 3.0

One TI <u>TUSB8041</u> 4-port USB3.0 is used to provide 4x USB3.0 ports on the FM191-RU. The 4-ports can be accessed via the USB type C connectors. Please note that the FM191-RU is **NOT COMPATIBLE** with the USB3.1.

The TUSB8041 is physical wired to the Programmable Logic (PL) side via the signals tFMC_TRZ_RX_P, tFMC_TRZ_RX_N, tFMC_TRZ_TX_P and tFMC_TRZ_TX_N (see Table 2 for further details).

4.3.3 VITA57.1 FMC-LPC I/O Module

The LPC (low-pin count) variant provides 34 differential I/O or 68x single-ended I/Os and 2 clocks as differential pairs. I²C and JTAG signals are also present. Background information here. A pin-out is provided at the end of this document and the signal names is shown in Figure 10.

Further details about the FMC-LPC module can be found in the following link http://en.wikipedia.org/wiki/FPGA_Mezzanine_Card.

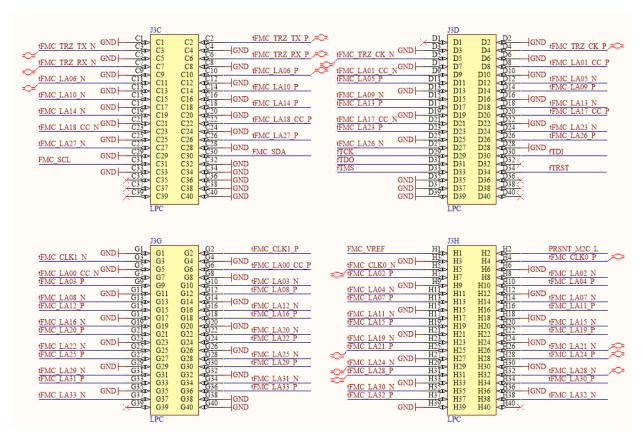


Figure 10: FMC-LPC pinout

4.3.4 ADC

Three TI <u>ADS122U04</u> 24bit, 4-channel, 2kSPS with UART interface are used for providing the 12x Analogue inputs 5V TTL. The ADCs channels are accessible via the P1 and P2 DB9 connectors. Analogue channels 0 to 6 (AO0-AO6) are accessible via P1 and AO7-AO11 via P2 connectors. Each ADC IC is programmed via a dedicated UART ports (UART1 to UART3).

Each DB9 (pin 1) supplies up to 5v@2A and it is protected with a fuse. Figure 11, Figure 12 and Figure 13 show the schematics of the signals of the level shifters, connectors and ADC ICs.

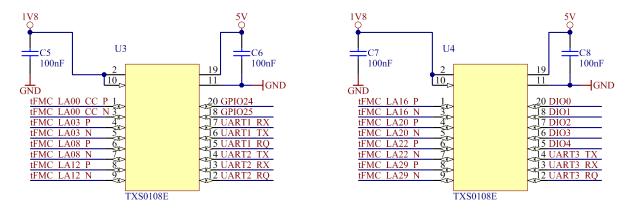


Figure 11: Schematics of the level shifters and pin-map of the UART ports.

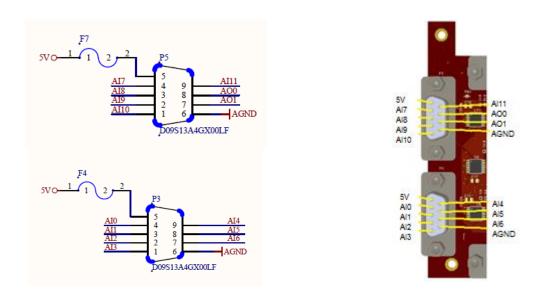


Figure 12: Schematics of P3 and P5 DB9 connectors (AIs)

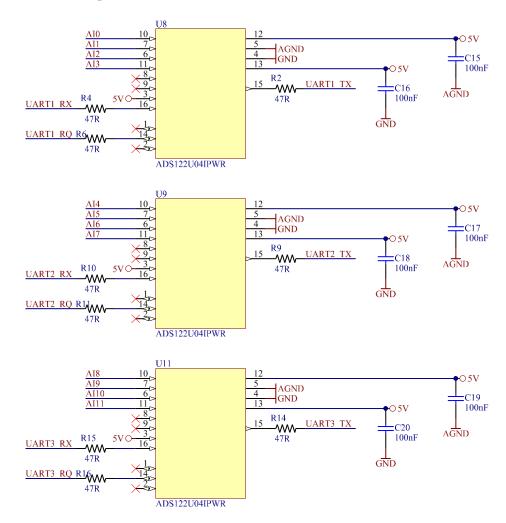


Figure 13: Schematics of the Analogue channels

4.3.5 DAC

One TI <u>DAC60508Z</u> 12bit, 8-channel with SPI interface is used for providing the 8x Analogue Outputs 5V TTL. The DACs channels are accessible via the P2 and P5 DB9 connectors. Analogue channels 0 to 1 (AO0-AO1) are accessible via P2 and AO2-A7 via P5 connectors. The DAC is programmed via a dedicated SPI ports.

Each DB9 (pin 1) supplies up to 5v@2A and it is protected with a fuse. Figure 14, Figure 15, Figure 16 show the schematics of the signals of the level shifters, connectors and DAC IC.

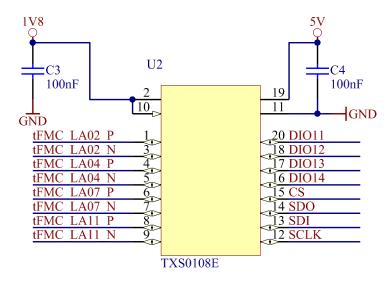


Figure 14: Schematics of the level shifters and pin-map of the SPI signals (CS, SDO, SDI, SDO).

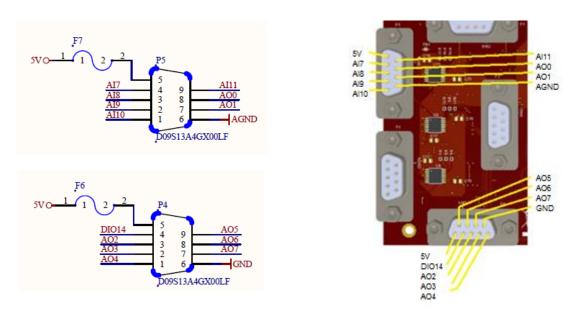


Figure 15: Schematics of P5 and P4 DB9 connectors (AOs)

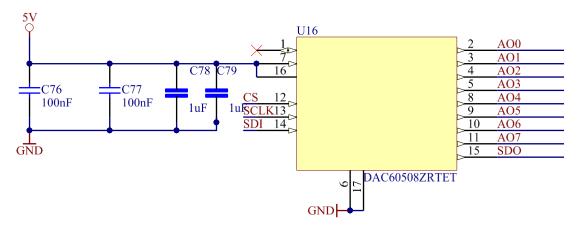
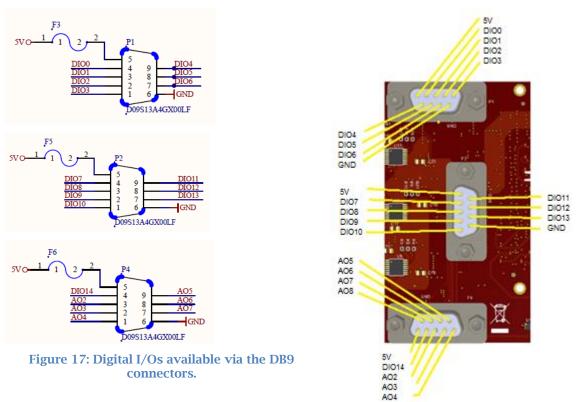


Figure 16: Schematics of the DAC

4.3.6 Single ended I/Os

15x digital I/Os (DIOs) 5V TTL are accessible via the P3, P4 and P5 DB9 connectors. P3 provides access to D0-D6, P4 to D7 – D13 and P4 to D14. Each DB9 (pin 1) supplies up to 5V@2A (per pin) and it is protected with a fuse.

28x general propose I/Os (GPIO0-GPIO27) 5V TTL are accessible via the 40-pin GPIOs. 5V@2A (per pin) can be driven from Pins 1 and 3 and 3V3@2A (the absolute maximum for both pins is 3A) from pins 2 and 4 and the pins are protected by fuses (Figure 17, Figure 18, Figure 19, Figure 20, Figure 21 and Figure 22).



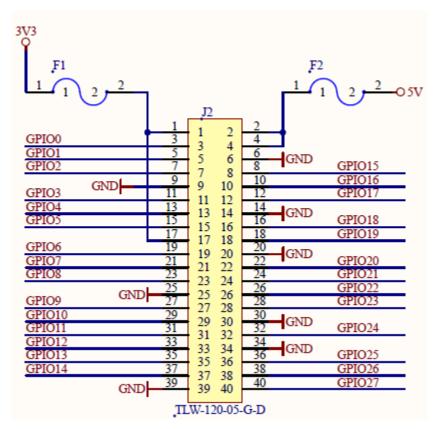


Figure 18: Schematics of the 40-pin GPIO at the FM191-U

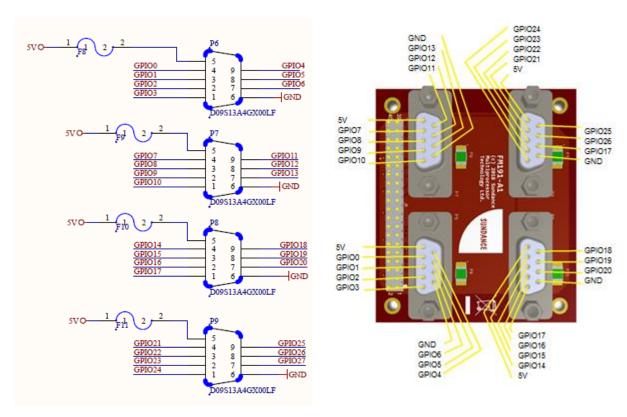


Figure 19: 40-pin GPIO connector schematics, and DB9s at FM191-A1

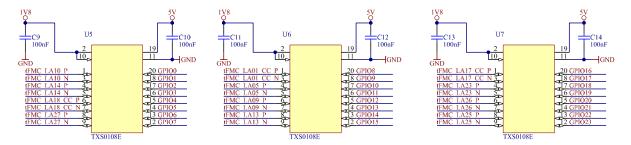


Figure 20: Level shifters and digital signals mapping (1/3)

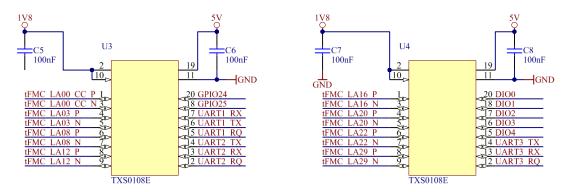


Figure 21: Level shifters and digital signals mapping (2/3)

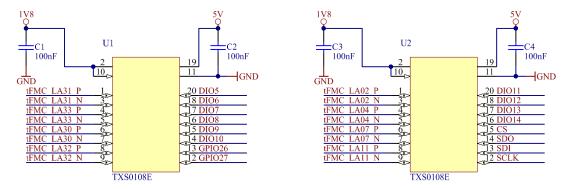


Figure 22: Level shifters digital signals mapping (3/3)

Board parts

Figure 23 shows the top view of the FM191-RU:

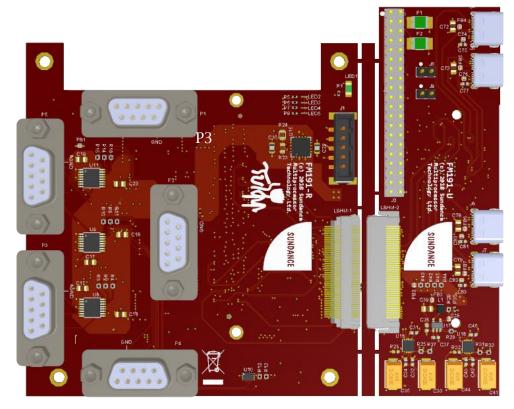


Figure 23: FM191-RU Top view

Figure 24 shows the bottom view of the FM191-RU:

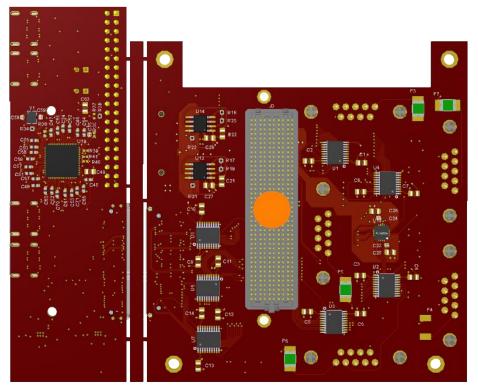


Figure 24 Bottom View of FM191-RU

Figure 25 shows the top/bottom view of the FM191-A1:

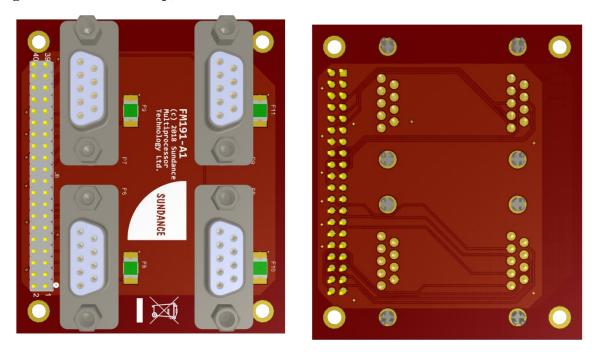


Figure 25 Top/Bottom View of FM191-A1

Table 1 lists all the connectors available on the FM191-RUA1 system.

Table 1: Connectors list

Connector reference	Description
P 1:9	DB9 connectors (top layer)
FMC-LPC	FMC – LPC connector (bottom layer)
USB-c 0:3	USB type c connectors (top layer)
GPIO	40-pin GPIO connector
ERNI	Power connector (PN: ERNI 254831)
LSHM-RA	100x pin's Samtec's LSHM right angle connector
LSHM-RRA	100x pin's Samtec's LSHM reverse right angle connector

5 Physical Properties

FM191-R Dimension	90mm	96mm
FM191 -U Dimension	33mm	106mm

Weight	
--------	--

Voltage	Power (estimate)

RH	10-80%
Temperature range	-10 to +50°C

MTBF	> 50,000 hours
------	----------------

6 EMC2-DP-V2 FMC Pin-Out

Table 2: EMC2-DP V2 - FM191-RUA1 pin map

EMC2-DP V2		IDV	TATA	TN f	TE0	TE0715-30		TE0715-30 TE0820		E0820	FM191- RUA1
SIGNAL	JBX	JBX PIN	JMX PIN	JM X	FPGA PIN	SIGN AL	FPG A PIN	SIGNAL	SIGNAL		
FMC_SCL/FMC1A-C30	JB1	32	31	JM1	W12	B13_L3_P	F5	B66_L6_N	FMC_SCL		
FMC_SDA/FMC1A-C31	ЈВ1	34	33	JM1	W13	B13_L3_N	G5	B66_L6_P	FMC_SDA		
tFMC_LA12_P/FMC1C-G15	ЈВ1	36	35	JM1	U11	B13_L5_P	C8	B66_L22_P	UART2_RX		
tFMC_LA12_N/FMC1C-G16	JB1	38	37	JM1	U12	B13_L5_N	В8	B66_L22_N	UART2_RQ		
tFMC_LA03_P/FMC1C-G9	JB1	46	45	JM1	R17	B13_L19_P	В6	B66_L20_N	UART1_RX		
tFMC_LA03_N/FMC1C-G10	ЈВ1	48	47	JM1	T17	B13_L19_N	C6	B66_L20_P	UART1_TX		
tFMC_LA04_P/FMC1D-H10	ЈВ1	50	49	JM1	V13	B13_L1_P	B1	B66_L7_N	DIO13		
tFMC_LA04_N/FMC1D-H11	JB1	52	51	JM1	V14	B13_L1_N	C1	B66_L7_P	DIO14		
tFMC_LA08_P/FMC1C-G12	JB1	56	55	JM1	AB13	B13_L9_P	D1	B66_L2_N	UART1_RQ		
tFMC_LA08_N/FMC1C-G13	JB1	58	57	JM1	AB14	B13_L9_N	E1	B66_L2_P	UART2_TX		
tFMC_CLK0_P/FMC1D-H4	JB1	60	59	JM1	Y15	B13_L12_N	D5	B66_L14_N	N/A		
tFMC_CLK0_N/FMC1D-H5	JB1	62	61	JM1	Y14	B13_L12_P	E5	B66_L14_P	N/A		
tFMC_LA01_P/FMC1B-D8	ЈВ1	66	65	JM1	AA15	B13_L11_N	C4	B66_L11_N	GPIO8		
tFMC_LA01_N/FMC1B-D9	JB1	68	67	JM1	AA14	B13_L11_P	D4	B66_L11_P	GPIO9		
tFMC_LA13_P/FMC1B-D17	JB1	70	69	JM1	AB16	B13_L17_P	G1	B66_L1_P	GPIO14		
tFMC_LA13_N/FMC1B-D18	JB1	72	71	JM1	AB17	B13_L17_N	F1	B66_L1_N	GPIO15		
tFMC_LA00_P/FMC1C-G6	ЈВ1	76	75	JM1	Y19	B13_L13_N	C2	B66_L12_N	GPIO24		
tFMC_LA00_N/FMC1C-G7	JB1	78	77	JM1	Y18	B13_L13_P	С3	B66_L12_P	GPIO25		
tFMC_LA02_P/FMC1D-H7	JB1	35	36	JM1	U13	B13_L6_P	E9	B66_L18_P	DIO11		
tFMC_LA02_N/FMC1D-H8	JB1	37	38	JM1	U14	B13_L6_N	D9	B66_L18_N	DIO12		
tFMC_LA11_P/FMC1D-H16	JB1	39	40	JM1	V11	B13_L4_P	G8	B66_L16_P	SDI		
tFMC_LA11_N/FMC1D-H17	JB1	41	42	JM1	W11	B13_L4_N	F7	B66_L16_N	SCLK		
tFMC_LA06_P/FMC1A-C10	JB1	45	46	JM1	AA11	B13_L7_P	E8	B66_L17_N	-		
tFMC_LA06_N/FMC1A-C11	ЈВ1	47	48	JM1	AB11	B13_L7_N	F8	B66_L17_P	-		
tFMC_LA05_P/FMC1B-D11	ЈВ1	49	50	JM1	AA12	B13_L8_P	G6	B66_L15_P	GPIO10		
tFMC_LA05_N/FMC1B-D12	ЈВ1	51	52	JM1	AB12	B13_L8_N	F6	B66_L15_N	GPIO11		
tFMC_LA07_P/FMC1D-H13	ЈВ1	55	56	JM1	Y12	B13_L10_P	F2	B66_L3_P	CS		
tFMC_LA07_N/FMC1D-H14	ЈВ1	57	58	JM1	Y13	B13_L10_N	E2	B66_L3_N	SDO		
tFMC_LA10_P/FMC1A-C14	JB1	59	60	JM1	V16	B13_L23_P	E4	B66_L5_P	GPIO0		
tFMC_LA10_N/FMC1A-C15	JB1	61	62	JM1	W16	B13_L23_N	E3	B66_L5_N	GPIO1		
tFMC_CLK1_P/FMC1C-G2	 ЈВ1	65	66	JM1	AA17	B13_L14_N	D6	B66_L13_N	N/A		
tFMC_CLK1_N/FMC1C-G3	 ЈВ1	67	68	JM1	AA16	B13_L14_P	D7	B66_L13_P	N/A		
tFMC_LA14_P/FMC1A-C18	ЈВ1	69	70	JM1	Y17	B13_L24_N	C9	B66_L24_P	GPIO2		
tFMC_LA14_N/FMC1A-C19	ЈВ1	71	72	JM1	W17	B13_L24_P	В9	B66_L24_N	GPIO3		
tFMC_LA15_P/FMC1D-H19	ЈВ1	75	76	JM1	AA19	B13_L18_P	A8	B66_L23_N	LED2		
tFMC_LA15_N/FMC1D-H20	ЈВ1	77	78	JM1	AA20	B13_L18_N	A9	B66_L23_P	LED3		
tFMC_LA09_P/FMC1B-D14	JB2	42	41	JM2	E3	B35_L21_N	AB3	B64_L15_N	GPIO12		
tFMC_LA09_N/FMC1B-D15	JB2	44	43	JM2	E4	B35_L21_P	AB4	B64_L15_P	GPIO13		
tFMC_LA20_N/FMC1C-G22	JB2	46	45	JM2	B6	B35_L8_N	AB4	B64_L17_P	DIO3		
tFMC_LA20_P/FMC1C-G22	JB2	48	47	JM2	В7	B35_L8_N B35_L8_P	AC2	B64_L17_P	DIO2		

BINCLAM PURCHACAZZ BIZ 34 33 DRZ CS BIS LILLY ACA BIS LILLY GORD	AFMC I A 10 P /PMC1 A COO	mo	ED		DAG.	GC.	DOE III D	4.04	DC4 114 D	CDIO 4
### OMICLARS_PYMICHEDS ### OF BE	tFMC_LA18_P/FMC1A-C22	JB2	52	51	JM2	C6	B35_L11_P	AC4	B64_L14_P	GPIO4
INICLASSASPICIOSIZE										
IFINC LAIS NYMCIE G19										
IPINC_LAIG_PYPINCIACIS										
### ### ### ### ### ### ### ### ### ##										
PRICLAZZ, N/SMCIACZZ										
THINCLAZ4_PYPINCID-IZES JB2 S2 S1 JM2 E5 B35_L5_N AG4 B6_L119_P N/A THINCLAZ4_PYPINCID-IZES JB2 S4 S3 JM2 F5 B35_L5_P AH4 B6_L119_N N/A THINCLAZ8_PYPINCID-IZES JB2 S8 S7 JM2 G6 B35_L6_N AG3 B6_L120_P N/A THINCLAZ8_PYPINCID-IZES JB2 S8 S7 JM2 G6 B35_L6_P AH5 B6_L120_N N/A THINCLAJ3_PYPINCID-IZES JB2 S8 S7 JM2 G6 B35_L6_P AH5 B6_L120_N N/A THINCLAJ3_PYPINCID-IZES JB2 S9 JM2 J6 B35_L14_P AE5 B6_L12_P THINCLA19_PYPINCID-IZES JB2 S1 S2 JM2 D3 B3_L14_P AE5 B6_L112_P THINCLA19_PYPINCID-IZES JB2 S3 S4 JM2 C3 B35_L14_P AE5 B6_L112_P THINCLA17_PYPINCID-IZES JB2 S3 S4 JM2 C4 B35_L14_N AF5 B6_L112_N THINCLA17_PYPINCID-IZES JB2 S7 S8 JM2 C4 B35_L14_N AF5 B6_L112_N THINCLA17_PYPINCID-IZES JB2 S3 S4 JM2 C4 B35_L14_N AF5 B6_L113_N GFF017 GFF016 JB2 G7 S8 JM2 F1 B35_L3_N AG0 B6_L7_P D604 THINCLA12_PYPINCID-IZES JB2 S3 S4 JM2 F2 B35_L3_N AG0 B6_L7_P D604 THINCLA12_PYPINCID-IZES JB2 S5 S6 JM2 D6 B35_L2_N AF8 B6_L18_N N/A THINCLA23_PYPINCID-IZES JB2 S5 S6 JM2 D6 B35_L2_N AF8 B6_L18_N N/A GFF017 JM2_L32_PYPINCID-IZES JB2 T3 T4 JM2 D2 B35_L17_N AH7 B6_L19_N GFF019 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D2 B35_L17_N AH7 B6_L19_N GFF019 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D2 B35_L17_N AH7 B6_L19_N GFF019 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D2 B35_L19_N AB7 B6_L14_N GFF022 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D2 B35_L19_N AB7 B6_L14_N GFF022 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D2 B35_L19_N AB7 B6_L14_N GFF025 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 D3 B35_L19_N AB7 B6_L14_N GFF026 THINCLA23_PYPINCID-IZES JB2 T7 T8 JM2 GFF B35_L19_N AB7 B6_L14_N GF										
##MCLA24_N/MCID420 ##R2 84 83 M2 F5 R53_L5_P ##R4 B64_L10_N N/A ##R4_LA28_N/MCID421 ##R2 148_N/MCID422 ##R2 88 87 M2 F6 R53_L6_N ##R4_LA28_N/MCID422 ##R2 90 80 M2 H6 R53_L0_P ##R4_LA28_N/MCID422 ##R2 51 52 M2 D3 R53_L14_P ##R4_LA28_N/MCID422 ##R2 51 55 56 M2 D3 R53_L14_P ##R4_LA28_N/MCID422 ##R2 55 55 56 M2 D5 R53_L14_N ##R4_LA28_N/MCID422 ##R2 57 58 M2 C4 R53_L12_N ##R4_LA28_N/MCIC624 ##R2 61 62 M2 F1 855_L12_N ##R4_LA28_N/MCIC625 ##R2 63 64 M2 F1 855_L12_N ##R4_LA28_N/MCIC625 ##R2 63 66 M2 F2 R53_L32_P ##R4_LA28_N/MCIC625 ##R2 65 66 M2 F2 R53_L32_P ##R4_LA28_N/MCID426 ##R4_LA28_N/MCIC625 ##R2 65 66 M2 F2 R53_L32_P ##R4_LA28_N/MCIC625 ##R2 67 68 M2 D5 R53_L12_N ##R5_LA28_N/MCIC626 ##R4_LA28_N/MCIC626 ##R4_LA28_N/MCIC627 ##R4_LA28_N/MCIC627 ##R4_LA28_N/MCIC628 ##R4_LA28_N/MCIC628 ##R4_LA28_N/MCIC628 ##R4_LA28_N/MCIC638 ##R4_LA38_N/MCIC638 ##R4_LA38_N/MCIC638 ##R4_LA38_N/MCIC638 ##R4_LA38_N/MCIC636 ##R4_LA38_N/MCIC636 ##R4_LA38_N/MCIC637 ##R4_LA										
### BEST 16.N AG3 B64_LEQ.P N/A ### DESCRIPTION OF THE CLASS_NIPMCID HSS BS BS BS BS BS BS BS					_					
### ### ### ### ### ### ### ### ### ##							B35_L5_P			
HINCLASZ_N/INICIDHS8	tFMC_LA28_P/FMC1D-H31	JB2	86	85	JM2	F6	B35_L6_N	AG3	B64_L20_P	N/A
IFINC_LAID_P/FINCID-ID22 JR2 51 52 JM2 D3 R35_L14_P AES R64_L12_P IED4 IFINC_LAID_N/FINCID-ID23 JR2 53 54 JM2 C3 R35_L14_N AFS R64_L12_N IED5 IFINC_LAIZ_P/FINCID-ID20 JR2 55 56 JM2 D5 R35_L12_P AD3 R64_L13_P GPIO16 IFINC_LAIZ_P/FINCID-ID21 JR2 57 58 JM2 C4 R35_L12_N AD4 R64_L13_N GPIO17 IFINC_LAIZ_P/FINCID-ID23 JR2 61 62 JM2 F1 R35_L22_N AG9 R64_L7_P D104 IFINC_LAIZ_P/FINCID-ID25 JR2 63 64 JM2 F2 R35_L23_P AH9 R64_L13_P D104 IFINC_LAIZ_P/FINCID-ID25 JR2 65 66 JM2 D6 R35_L2_P AF8 R64_L8_P N/A IFINC_LAIZ_P/FINCID-ID25 JR2 67 68 JM2 D7 R35_L2_P AG8 R64_L8_P N/A IFINC_LAIZ_P/FINCID-ID23 JR2 77 77 JM2 E2 R35_L12_P AH8 R64_L9_P GPIO18 IFINC_LAIZ_P/FINCID-ID23 JR2 77 77 JM2 E2 R35_L12_P AH8 R64_L9_P GPIO19 IFINC_LAIZ_P/FINCID-ID23 JR2 77 78 JM2 D2 R35_L12_N AH7 R64_L9_P GPIO23 IFINC_LAIZ_P/FINCID-ID24 JR2 77 78 JM2 G1 R35_L12_N AH7 R64_L9_P GPIO23 IFINC_LAIZ_P/FINCID-G31 JR2 R3 R4 JM2 AF R35_L9_P AC7 R64_L5_P UARTI_RX IFINC_LAIZ_P/FINCID-G31 JR2 R3 R4 JM2 A7 R35_L9_P AC7 R64_L5_N UARTI_RX IFINC_LAIS_P/FINCID-G34 JR2 R7 R8 JM2 A7 R35_L9_P AC7 R64_L5_N DIO5 IFINC_LAIS_P/FINCID-G34 JR2 R7 R8 JM2 A7 R35_L9_P AC7 R64_L5_N DIO5 IFINC_LAIS_P/FINCID-G34 JR2 87 R8 JM2 A7 R35_L10_P AC7 R64_L5_N DIO5 IFINC_LAIS_P/FINCID-G34 JR2 87 R8 JM2 A7 R35_L10_P AC7 R64_L5_N DIO5 IFINC_LAIS_P/FINCID-G36 JR2 97 98 JM2 A4 R35_L10_N AF1 R64_L24_P DIO5 IFINC_LAIS_P/FINCID-G36 JR2 97 98 JM2 A7 R35_L0_P AH1 R64_L24_P DIO5 IFINC_LAIS_P/FINCID-G36 JR2 97 98 JM2 A7 R35_L0_P AH1 R64_L24_P DIO5 IFINC_LAIS_P/FINCID-G36 JR2 97 98 JM2 A7 R35_L0_P AH1 R64_L24_N DIO6 IFINC_LAIS_P	tFMC_LA28_N/FMC1D-H32	JB2	88	87	JM2	G6	B35_L6_P	АНЗ	B64_L20_N	N/A
FINCLIA19.N/PMCID-H23 JIE 53 54 JM2 C3 B35_L14_N AF5 B64_L12_N LED5 FINCLIA17_N/PMCIB-D20 JIE 55 56 JM2 D5 B35_L12_P AD5 B64_L13_P GPI016 FIMC_LA17_N/PMCIB-D21 JB2 57 58 JM2 C4 B35_L12_N AD4 B64_L13_N GPI017 FIMC_LA22_P/PMCIC-G24 JB2 61 62 JM2 F1 B35_L23_N AG9 B64_L7_P DIO4 FIMC_LA22_N/PMCIC-G25 JB2 63 64 JM2 F2 B35_L12_N AF8 B64_L7_N UART3_TX FIMC_LA21_N/PMCID-H25 JJE 65 66 JM2 D6 B35_L2_N AF8 B64_L8_P N/A FIMC_LA21_N/PMCID-H26 JJE 67 68 JM2 D7 B35_L2_P AG8 B64_L8_N N/A FIMC_LA23_N/PMCIB-D23 JJE 71 72 JM2 E2 B35_L17_P AH8 B64_L9_P GPI018 FIMC_LA23_N/PMCIB-D24 JJE 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GPI019 FIMC_LA25_N/PMCIC-G27 JJE 75 76 JM2 H1 B35_L24_P AE7 B64_L4_P GPI022 FIMC_LA25_N/PMCIC-G28 JJE 77 78 JM2 G1 B35_L14_N AD7 B64_L4_P GPI023 FIMC_LA29_N/PMCIC-G30 JJE 81 82 JM2 A6 B35_L12_N AB7 B64_L5_D UART3_RX FIMC_LA29_N/PMCIC-G31 JJE 83 84 JM2 A7 B35_L2_P AC7 B64_L5_N UART3_RX FIMC_LA29_N/PMCIC-G31 JJE 83 84 JM2 A7 B35_L2_D AC7 B64_L5_N UART3_RX FIMC_LA29_N/PMCIC-G31 JJE 85 86 JM2 G2 B35_L12_N AB6 B64_L5_D DI05 FIMC_LA31_N/PMCIC-G34 JJE 87 88 JM2 G3 B35_L12_D AC6 B64_L5_D DI05 FIMC_LA31_N/PMCIC-G36 JJE 97 98 JM2 A4 B35_L10_N AFI B64_L2_D DI05 FIMC_LA32_N/PMCID-H35 JJE 97 98 JM2 G4 B35_L20_D AH1 B64_L23_N DI06 FIMC_LA32_N/PMCID-H37 JJE 99 100 JM2 H5 B35_L20_D AH1 B64_L23_N DI06 FIMC_LA32_N/PMCID-H37 JJE 99 100 JM2 H5 B35_L20_D AH1 B64_L24_N DI010 FIMC_LA32_N/PMCID-H37 JJE 99 100 JM2 H5 B35_L20_D AH1 B64_L24_N DI010 FIMC_LA32_N/PMCID-H37 JJE 99 100 JM2 H5 B35_L20_D AH1 B64_L23_N DI06 FIMC_LA32_N/PMCID-H37 JJE 99 100 JM2 H5	tFMC_LA32_N/FMC1D-H38	JB2	90	89	JM2	Н6	B35_L0	AD6	B64_T0	GPIO27
FENC_LAI7_P/FENCIB-D20 JB2 55 56 JM2 D5 B35_L12_P AD5 B64_L13_P GPI016 FENC_LAI7_N/FENCIB-D21 JB2 57 58 JM2 C4 B35_L12_N AD4 B64_L13_N GPI017 FENC_LAIZ_P/FENCIC-G24 JB2 61 62 JM2 F1 B35_L23_N AG6 B64_L17_P DI04 FENC_LAIZ_P/FENCIC-G25 JB2 63 64 JM2 F2 B35_L23_P AH9 B64_L17_N UART3_TX FENC_LAIZ_P/FENCID-H25 JB2 65 66 JM2 D6 B35_L2_N AF8 B64_L8_P N/A FENC_LAIZ_P/FENCID-H25 JB2 67 68 JM2 D7 B35_L2_P AG8 B64_L8_N N/A FENC_LAIZ_P/FENCID-H26 JB2 67 68 JM2 D7 B35_L12_P AG8 B64_L8_N N/A FENC_LAIZ_P/FENCID-H26 JB2 71 72 JM2 E2 B35_L17_P AH8 B64_L9_P GPI018 FENC_LAIZ_P/FENCID-H27 JB2 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GPI019 FENC_LAIZ_P/FENCID-G27 JB2 75 76 JM2 H1 B35_L24_P AE7 B64_L4_N GPI023 FENC_LAIZ_P/FENCID-G28 JB2 77 78 JM2 G1 B35_L9_N AD7 B64_L4_P GPI023 FENC_LAIZ_P/FENCID-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX FENC_LAIZ_P/FENCID-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX FENC_LAIZ_P/FENCID-G31 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_N DI05 FENC_LAIZ_P/FENCID-G31 JB2 87 88 JM2 G3 B35_L12_P AC6 B64_L6_N DI05 FENC_LAIZ_P/FENCID-G36 JB2 97 98 JM2 A3 B35_L10_P AG1 B64_L2_N DI06 FENC_LAIZ_P/FENCID-G37 JB2 97 98 JM2 A3 B35_L10_P AG1 B64_L2_N DI06 FENC_LAIZ_P/FENCID-G37 JB2 97 98 JM2 A6 B35_L12_D AH1 B64_L12_N DI06 FENC_LAIZ_P/FENCID-G37 JB2 97 98 JM2 A6 B35_L12_D AH1 B64_L12_N DI06 FENC_LAIZ_P/FENCID-G36 JB2 97 98 JM2 A6 B35_L12_D AH1 B64_L12_N DI06 FENC_LAIZ_P/FENCID-G37 JB2 97 98 JM2 A6 B35_L12_D AH1 B64_L12_N DI06 FENC_LAIZ_P/FENCID-G36 JB2 97 98 JM2 A6 B35_L12_D AH1 B64_L12_N DI06 FENC_LAIZ_P/FENCID-G37 JB2 97 98	tFMC_LA19_P/FMC1D-H22	JB2	51	52	JM2	D3	B35_L14_P	AE5	B64_L12_P	LED4
FINCLIAIZ.N/FINCID-D21 JB2 57 58 JM2 C4 B35.L12.N AD4 B64.L13.N GFI017 FINCLIAIZ.P/FINCICG24 JB2 61 62 JM2 F1 B35.L23.N AG9 B64.L7.P DIO4 FINCLIAIZ.P/FINCICG25 JB2 63 64 JM2 F2 B35.L23.P AH9 B64.L7.N UART3.TX FINCLIAIZ.P/FINCID-HI25 JB2 65 66 JM2 D6 B35.L2.N AF8 B64.L8.P N/A FINCLIAIZ.P/FINCID-HI26 JB2 67 68 JM2 D7 B35.L2.P AG8 B64.L8.P N/A FINCLIAIZ.P/FINCID-HI26 JB2 77 77 JM2 E2 B35.L17.P AH8 B64.L9.P GFI018 FINCLIAIZ.P/FINCIB-D23 JB2 77 74 JM2 D2 B35.L17.N AH7 B64.L9.N GFI019 FINCLIAIZ.P/FINCIC-G27 JB2 75 76 JM2 H1 B35.L24.P AE7 B64.L4.N GFI022 FINCLIAIZ.P/FINCIC-G28 JB2 77 78 JM2 G1 B35.L12.N AB7 B64.L4.P GFI023 FINCLIAIZ.P/FINCIC-G30 JB2 81 82 JM2 A6 B35.L9.N AB7 B64.L5.P UART3.RX FINCLIAIZ.P/FINCIC-G31 JB2 83 84 JM2 A7 B35.L9.P AC7 B64.L5.N UART3.RQ FINCLIAIZ.P/FINCIC-G34 JB2 87 88 JM2 G3 B35.L12.P AC6 B64.L6.N DIO6 FINCLIAIZ.N/FINCIC-G34 JB2 87 88 JM2 G3 B35.L12.P AC6 B64.L6.N DIO6 FINCLIAIZ.N/FINCIC-G36 JB2 93 94 JM2 A5 B35.L10.N AF1 B64.L24.P DIO9 FINCLIAIZ.N/FINCIC-G37 JB2 93 94 JM2 A5 B35.L10.P AG1 B64.L24.N DIO10 FINCLIAIZ.N/FINCIC-G37 JB2 97 98 JM2 G4 B35.L25 AH6 B64.T1 GFI026 FINCLIAIZ.N/FINCIC-G37 JB2 97 98 JM2 G4 B35.L25 AH6 B64.T1 GFI026 FINCLIAIZ.N/FINCIC-G37 JB2 97 98 JM2 G4 B35.L25 AH6 B64.T1 GFI026 FINCLIAIZ.N/FINCIC-G37 JB3 26 25 JM3 W2 MGT.TX3.N E25 B505.TX0.D UXR.STRM.LIP FINCLIAIZ.N/FINCIC-G46 JB3 27 28 JM3 W6 MGT.RX3.N F27 B505.RX0.D UXR.STRM.LIP FINCLIAIZ.N/FINCIC-G46 JB3 27 28 JM3 W6 MGT.RX3.N F27 B505.RX0.D UXR.STRM.LIP FINCLIAIZ.N/FINCIC-G6 JB3 27 28 JM3 W6 MGT.RX3.D F28 B505.RX0.D UXR.STRM.LIP	tFMC_LA19_N/FMC1D-H23	JB2	53	54	JM2	С3	B35_L14_N	AF5	B64_L12_N	LED5
FENC_LA22_P/FENCICG24 Biz 61 62 JM2 FI B35_L23_N AG9 B64_L7_P DIO4 FENC_LA22_P/FENCICG25 Biz 63 64 JM2 F2 B35_L23_P AH9 B64_L7_N UART3_TX FENC_LA21_P/FENCICH25 JB2 65 66 JM2 D6 B35_L2_N AF8 B64_L8_P N/A FENC_LA21_P/FENCICH25 JB2 67 68 JM2 D7 B35_L2_P AG8 B64_L8_N N/A FENC_LA23_P/FENCICH26 JB2 71 72 JM2 E2 B35_L17_P AH8 B64_L9_P GFIO18 FENC_LA23_N/FENCICH23 JB2 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GFIO19 FENC_LA23_N/FENCICG27 JB2 75 76 JM2 H1 B35_L24_P AE7 B64_L4_N GFIO22 FENC_LA25_N/FENCICG27 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GFIO23 FENC_LA25_N/FENCICG30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX FENC_LA25_N/FENCICG31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX FENC_LA25_N/FENCICG31 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_P DIO5 FENC_LA31_N/FENCICG34 JB2 87 88 JM2 G3 B35_L22_P AC6 B64_L6_N DIO6 FENC_LA31_N/FENCICG34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_P DIO9 FENC_LA31_N/FENCICG36 JB2 95 96 JM2 A5 B35_L10_N AF1 B64_L24_N DIO10 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 A5 B35_L10_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB2 97 98 JM2 G4 B35_L20_N AH1 B64_L23_N DIO8 FENC_LA32_N/FENCICG37 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B305_TX0_N USE_SSTM_UP FENC_TRZ_TX_N/FENCICG5 JB3 27 28 JM3 W6 M	tFMC_LA17_P/FMC1B-D20	JB2	55	56	JM2	D5	B35_L12_P	AD5	B64_L13_P	GPIO16
FENC_LA22_N/FENCICG25 JB2 63 64 JM2 F2 B35_L23_P AHD B64_L7_N UART3_TX	tFMC_LA17_N/FMC1B-D21	JB2	57	58	JM2	C4	B35_L12_N	AD4	B64_L13_N	GPIO17
IFMC_LA21_P/FMCIDH25	tFMC_LA22_P/FMC1C-G24	JB2	61	62	JM2	F1	B35_L23_N	AG9	B64_L7_P	DIO4
IEMC_LA21_N/FMCID-H26 JB2 67 68 JM2 D7 B35_L2_P AG8 B64_L8_N N/A IFMC_LA23_P/FMCIB-D23 JB2 71 72 JM2 E2 B35_L17_P AH8 B64_L9_P GPI018 IFMC_LA23_P/FMCID-D24 JB2 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GPI019 IFMC_LA25_P/FMCID-G27 JB2 75 76 JM2 H1 B35_L24_P AE7 B64_L4_P GPI022 IFMC_LA25_P/FMCID-G28 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GPI023 IFMC_LA29_P/FMCID-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX IFMC_LA31_P/FMCIC-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX IFMC_LA31_P/FMCIC-G33 JB2 87 88 JM2 G2 B35_L22_N AB6 B64_L6_P DI05	tFMC_LA22_N/FMC1C-G25	JB2	63	64	JM2	F2	B35_L23_P	AH9	B64_L7_N	UART3_TX
IFMC_LA23_P/FMCIB-D23 JB2 71 72 JM2 E2 B35_L17_P AH8 B64_L9_P GPI018 IFMC_LA23_N/FMCIB-D24 JB2 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GPI019 IFMC_LA25_P/FMCIC-G27 JB2 75 76 JM2 H1 B35_L24_P AE7 B64_L4_N GPI029 IFMC_LA25_P/FMCIC-G28 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GPI023 IFMC_LA29_P/FMCIC-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_N UART3_RX IFMC_LA31_P/FMCIC-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX IFMC_LA31_N/FMCIC-G33 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_P DI05 IFMC_LA31_N/FMCIC-G34 JB2 87 88 JM2 G3 B35_L12_N AC6 B64_L6_N DI	tFMC_LA21_P/FMC1D-H25	JB2	65	66	JM2	D6	B35_L2_N	AF8	B64_L8_P	N/A
IFMC_LA23_N/FMCIB-D24 JB2 73 74 JM2 D2 B35_L17_N AH7 B64_L9_N GPI019 IFMC_LA23_N/FMCIB-D24 JB2 75 76 JM2 H1 B35_L124_P AE7 B64_L4_N GPI022 IFMC_LA25_N/FMCIG-G28 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GPI023 IFMC_LA29_N/FMCIG-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX IFMC_LA31_N/FMCIG-G31 JB2 83 84 JM2 A7 B35_L9_N AB6 B64_L5_N UART3_RX IFMC_LA31_N/FMCIG-G33 JB2 85 86 JM2 G2 B35_L12_N AB6 B64_L6_P DI05 IFMC_LA31_N/FMCIG-G34 JB2 87 88 JM2 G3 B35_L10_N AF1 B64_L6_N DI06 IFMC_LA32_N/FMCIG-G36 JB2 93 94 JM2 A5 B35_L10_N AH2 B64_L24_N DI	tFMC_LA21_N/FMC1D-H26	ЈВ2	67	68	JM2	D7	B35_L2_P	AG8	B64_L8_N	N/A
tFMC_LA25_P/FMC1C-G27 JB2 75 76 JM2 H1 B35_L24_P AE7 B64_L4_N GPI022 tFMC_LA25_P/FMC1C-G28 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GPI023 tFMC_LA29_P/FMC1C-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX tFMC_LA31_P/FMC1C-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX tFMC_LA31_P/FMC1C-G33 JB2 85 86 JM2 G2 B35_L12_N AB6 B64_L6_P DI05 tFMC_LA31_P/FMC1C-G34 JB2 87 88 JM2 G3 B35_L12_N AG6 B64_L6_N DI06 tFMC_LA30_P/FMC1D-H34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_N DI010 tFMC_LA33_P/FMC1D-H35 JB2 93 94 JM2 A5 B35_L10_N AH2 B64_L24_N DI0	tFMC_LA23_P/FMC1B-D23	ЈВ2	71	72	JM2	E2	B35_L17_P	AH8	B64_L9_P	GPIO18
IFMC_LA25_N/FMCIC-G28 JB2 77 78 JM2 G1 B35_L24_N AD7 B64_L4_P GPIO23 IFMC_LA29_N/FMCIC-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX IFMC_LA31_N/FMCIC-G31 JB2 83 84 JM2 A7 B35_L9_N AC7 B64_L5_N UART3_RX IFMC_LA31_N/FMCIC-G33 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_N DIO5 IFMC_LA31_N/FMCIC-G34 JB2 87 88 JM2 G3 B35_L22_N AC6 B64_L6_N DIO6 IFMC_LA31_N/FMCID-H34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_N DIO9 IFMC_LA33_N/FMCID-H35 JB2 93 94 JM2 A5 B35_L20_N AH2 B64_L23_N DIO7 IFMC_LA33_N/FMCIC-G36 JB2 95 96 JM2 F4 B35_L20_N AH1 B64_L23_N DIO7<	tFMC_LA23_N/FMC1B-D24	ЈВ2	73	74	JM2	D2	B35_L17_N	AH7	B64_L9_N	GPIO19
tFMC_LA29_P/FMC1C-G30 JB2 81 82 JM2 A6 B35_L9_N AB7 B64_L5_P UART3_RX tFMC_LA29_N/FMC1C-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RX tFMC_LA31_P/FMC1C-G33 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_P DIO5 tFMC_LA31_N/FMC1C-G34 JB2 87 88 JM2 G3 B35_L12_P AC6 B64_L6_N DIO6 tFMC_LA30_P/FMC1D-H34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_P DIO9 tFMC_LA30_N/FMC1D-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DIO10 tFMC_LA33_P/FMC1C-G36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_N DIO7 tFMC_LA32_P/FMC1D-H37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8<	tFMC_LA25_P/FMC1C-G27	ЈВ2	75	76	JM2	H1	B35_L24_P	AE7	B64_L4_N	GPIO22
tfmc_La29_N/FMC1C-G31 JB2 83 84 JM2 A7 B35_L9_P AC7 B64_L5_N UART3_RQ tfmc_La31_P/FMC1C-G33 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_P DIO5 tfmC_La31_N/FMC1C-G34 JB2 87 88 JM2 G3 B35_L12_P AC6 B64_L6_N DIO6 tfmC_LA30_P/FMC1D-H34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_P DIO9 tfmC_LA30_N/FMC1D-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DIO10 tfmC_LA33_N/FMC1C-G36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_N DIO7 tfmC_LA33_N/FMC1C-G37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8 tfmC_LA32_P/FMC1D-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_L11 GPIO26 <td>tFMC_LA25_N/FMC1C-G28</td> <td>ЈВ2</td> <td>77</td> <td>78</td> <td>JM2</td> <td>G1</td> <td>B35_L24_N</td> <td>AD7</td> <td>B64_L4_P</td> <td>GPIO23</td>	tFMC_LA25_N/FMC1C-G28	ЈВ2	77	78	JM2	G1	B35_L24_N	AD7	B64_L4_P	GPIO23
tfmc_La31_P/fmc1c-G33 JB2 85 86 JM2 G2 B35_L22_N AB6 B64_L6_P DIO5 tfmc_La31_N/fmc1c-G34 JB2 87 88 JM2 G3 B35_L22_P AC6 B64_L6_N DIO6 tfmc_La30_P/fmc1D-H34 JB2 91 92 JM2 A4 B35_L10_N AF1 B64_L24_P DIO9 tfmc_La30_N/fmc1D-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DIO10 tfmc_La33_N/fmc1C-G36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_P DIO7 tfmc_La32_P/fmc1C-G37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8 tfmc_La32_P/fmc1D-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_T1 GPIO26 tfmC_TRZ_TX_N/fmc1A-C3 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B505_TX0_N USB_SSTXM	tFMC_LA29_P/FMC1C-G30	ЈВ2	81	82	JM2	A6	B35_L9_N	AB7	B64_L5_P	UART3_RX
tFMC_LA31_N/FMC1C-G34 JB2 87 88 JM2 G3 B35_L22_P AC6 B64_L6_N DIO6 tFMC_LA30_P/FMC1D-H34 JB2 91 92 JM2 A4 B35_L10_N AFI B64_L24_P DIO9 tFMC_LA30_N/FMC1D-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DIO10 tFMC_LA33_P/FMC1C-G36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_P DIO7 tFMC_LA33_N/FMC1C-G37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8 tFMC_LA32_P/FMC1D-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_T1 GPIO26 tFMC_TRZ_TX_N/FMC1A-C3 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B505_TX0_P USB_SSTXP_UP tFMC_TRZ_TX_N/FMC1A-C2 JB3 25 26 JM3 Y6 MGT_RX3_N F27 B505_RX0_N <t< td=""><td>tFMC_LA29_N/FMC1C-G31</td><td>ЈВ2</td><td>83</td><td>84</td><td>JM2</td><td>A7</td><td>B35_L9_P</td><td>AC7</td><td>B64_L5_N</td><td>UART3_RQ</td></t<>	tFMC_LA29_N/FMC1C-G31	ЈВ2	83	84	JM2	A7	B35_L9_P	AC7	B64_L5_N	UART3_RQ
tFMC_LA30_P/FMC1D-H34 JB2 91 92 JM2 A4 B35_L10_N AFI B64_L24_P DIO9 tFMC_LA30_N/FMC1D-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DIO10 tFMC_LA33_P/FMC1C-G36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_P DIO7 tFMC_LA33_N/FMC1C-G37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8 tFMC_LA32_P/FMC1D-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_LT3_N DIO8 tFMC_TRZ_TX_N/FMC1A-C3 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B505_TX0_P USB_SSTXM_UP tFMC_TRZ_RX_N/FMC1A-C2 JB3 28 27 JM3 Y2 MGT_RX3_N F27 B505_RX0_P USB_SSRXM_UP tFMC_TRZ_RX_P/FMC1A-C6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N <td>tFMC_LA31_P/FMC1C-G33</td> <td>ЈВ2</td> <td>85</td> <td>86</td> <td>JM2</td> <td>G2</td> <td>B35_L22_N</td> <td>AB6</td> <td>B64_L6_P</td> <td>DIO5</td>	tFMC_LA31_P/FMC1C-G33	ЈВ2	85	86	JM2	G2	B35_L22_N	AB6	B64_L6_P	DIO5
tfmc_La30_n/fmc1d-H35 JB2 93 94 JM2 A5 B35_L10_P AG1 B64_L24_N DI010 tfmc_La33_n/fmc1c-G36 JB2 95 96 JM2 F4 B35_L20_n AH2 B64_L23_n DI07 tfmc_La33_n/fmc1c-G37 JB2 97 98 JM2 G4 B35_L20_n AH1 B64_L23_n DI08 tfmc_La32_n/fmc1d-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_L123_n DI08 tfmc_trz_tx_n/fmc1a-c3 JB3 26 25 JM3 Y2 MGT_tx3_n E25 B505_tx0_p USB_SSTXM_UP tfmc_trz_tx_n/fmc1a-c2 JB3 28 27 JM3 W2 MGT_tx3_n E26 B505_tx0_n USB_SSRXM_UP tfmc_trz_rx_n/fmc1a-c6 JB3 27 28 JM3 W6 MGT_rx3_p F28 B505_rx0_n USB_SSRXP_UP tfmc_trz_ck_p/fmc1a-c6 JB3 31 32 JM3 W6 MGT_rx3_p F28 B50	tFMC_LA31_N/FMC1C-G34	JB2	87	88	JM2	G3	B35_L22_P	AC6	B64_L6_N	DIO6
tfmc_la33_p/fmc1c-g36 JB2 95 96 JM2 F4 B35_L20_N AH2 B64_L23_P Dio7 tfmc_la33_n/fmc1c-g37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N Dio8 tfmc_la32_p/fmc1d-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_L23_N Dio8 tfmc_trz_tx_n/fmc1a-c3 JB3 26 25 JM3 Y2 MGT_tx3_N E25 B505_tx0_P USB_SSTXM_UP tfmc_trz_tx_p/fmc1a-c2 JB3 28 27 JM3 Y2 MGT_tx3_N F26 B505_tx0_N USB_SSTXM_UP tfmc_trz_rx_n/fmc1a-c7 JB3 25 26 JM3 Y6 MGT_rx3_N F27 B505_rx0_P USB_SSRXM_UP tfmc_trz_rx_p/fmc1a-c6 JB3 27 28 JM3 W6 MGT_rx3_P F28 B505_rx0_N USB_SSRXP_UP tfmc_trz_ck_p/fmc1b-d4 JB3 31 32 JM3 CLKIN2_P CLKIN2_P CLKIN_P <td>tFMC_LA30_P/FMC1D-H34</td> <td>JB2</td> <td>91</td> <td>92</td> <td>JM2</td> <td>A4</td> <td>B35_L10_N</td> <td>AF1</td> <td>B64_L24_P</td> <td>DIO9</td>	tFMC_LA30_P/FMC1D-H34	JB2	91	92	JM2	A4	B35_L10_N	AF1	B64_L24_P	DIO9
tFMC_LA33_N/FMC1C-G37 JB2 97 98 JM2 G4 B35_L20_P AH1 B64_L23_N DIO8 tFMC_LA32_P/FMC1D-H37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_T1 GPIO26 tFMC_TRZ_TX_N/FMC1A-C3 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B505_TX0_P USB_SSTXM_UP tFMC_TRZ_TX_P/FMC1A-C2 JB3 28 27 JM3 W2 MGT_TX3_P E26 B505_TX0_N USB_SSTXP_UP tFMC_TRZ_RX_N/FMC1A-C7 JB3 25 26 JM3 Y6 MGT_RX3_N F27 B505_RX0_P USB_SSRXM_UP tFMC_TRZ_RX_P/FMC1A-C6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N USB_SSRXP_UP tFMC_TRZ_CK_P/FMC1B-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_LA30_N/FMC1D-H35	JB2	93	94	JM2	A5	B35_L10_P	AG1	B64_L24_N	DIO10
tfmc_la32_p/fmc1d-h37 JB2 99 100 JM2 H5 B35_L25 AH6 B64_T1 GPI026 tfmc_trz_tx_n/fmc1a-c3 JB3 26 25 JM3 Y2 MGT_tx3_n E25 B505_tx0_p USB_SSTXM_UP tfmc_trz_tx_p/fmc1a-c2 JB3 28 27 JM3 W2 MGT_tx3_p E26 B505_tx0_n USB_SSTXP_UP tfmc_trz_rx_n/fmc1a-c7 JB3 25 26 JM3 Y6 MGT_rx3_n F27 B505_rx0_p USB_SSRXM_UP tfmc_trz_rx_n/fmc1a-c6 JB3 27 28 JM3 W6 MGT_rx3_p F28 B505_rx0_n USB_SSRXP_UP tfmc_trz_ck_p/fmc1a-c6 JB3 31 32 JM3 CLKIN2_p CLKIN2_p N/A	tFMC_LA33_P/FMC1C-G36	ЈВ2	95	96	JM2	F4	B35_L20_N	AH2	B64_L23_P	DIO7
tfmC_Trz_Tx_n/fmc1a-c3 JB3 26 25 JM3 Y2 MGT_TX3_N E25 B505_TX0_P USB_SSTXM_UP tfmC_Trz_Tx_P/fmC1a-c2 JB3 28 27 JM3 W2 MGT_TX3_P E26 B505_TX0_N USB_SSTXP_UP tfmC_Trz_rx_N/fmC1a-c7 JB3 25 26 JM3 Y6 MGT_RX3_N F27 B505_RX0_P USB_SSRXM_UP tfmC_Trz_rx_r/fmC1a-c6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N USB_SSRXP_UP tfmC_Trz_ck_P/fmC1b-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_LA33_N/FMC1C-G37	ЈВ2	97	98	JM2	G4	B35_L20_P	AH1	B64_L23_N	DIO8
tFMC_TRZ_TX_P/FMC1A-C2 JB3 28 27 JM3 W2 MGT_TX3_P E26 B505_TX0_N USB_SSTXP_UP tFMC_TRZ_RX_N/FMC1A-C7 JB3 25 26 JM3 Y6 MGT_RX3_N F27 B505_RX0_P USB_SSRXM_UP tFMC_TRZ_RX_P/FMC1A-C6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N USB_SSRXP_UP tFMC_TRZ_CK_P/FMC1B-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_LA32_P/FMC1D-H37	JB2	99	100	JM2	Н5	B35_L25	АН6	B64_T1	GPIO26
tFMC_TRZ_RX_N/FMC1A-C7 JB3 25 26 JM3 Y6 MGT_RX3_N F27 B505_RX0_P USB_SSRXM_UP tFMC_TRZ_RX_P/FMC1A-C6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N USB_SSRXP_UP tFMC_TRZ_CK_P/FMC1B-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_TRZ_TX_N/FMC1A-C3	ЈВ3	26	25	JM3	Y2	MGT_TX3_N	E25	B505_TX0_P	USB_SSTXM_UP
tFMC_TRZ_RX_P/FMC1A-C6 JB3 27 28 JM3 W6 MGT_RX3_P F28 B505_RX0_N USB_SSRXP_UP tFMC_TRZ_CK_P/FMC1B-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_TRZ_TX_P/FMC1A-C2	ЈВ3	28	27	JM3	W2	MGT_TX3_P	E26	B505_TX0_N	USB_SSTXP_UP
tFMC_TRZ_CK_P/FMC1B-D4 JB3 31 32 JM3 CLKIN2_P CLKIN_P N/A	tFMC_TRZ_RX_N/FMC1A-C7	ЈВ3	25	26	JM3	Y6	MGT_RX3_N	F27	B505_RX0_P	USB_SSRXM_UP
	tFMC_TRZ_RX_P/FMC1A-C6	ЈВ3	27	28	JM3	W6	MGT_RX3_P	F28	B505_RX0_N	USB_SSRXP_UP
tFMC_TRZ_CK_N/FMC1B-D5 JB3 33 34 JM3 CLKIN2_N CLKIN_N N/A	tFMC_TRZ_CK_P/FMC1B-D4	JB3	31	32	JM3		CLKIN2_P		CLKIN_P	N/A
	tFMC_TRZ_CK_N/FMC1B-D5	ЈВ3	33	34	JM3		CLKIN2_N		CLKIN_N	N/A

7 Design Release & Quality

The full schematic will be available Sundance as will the FPGA reference designs to interface the FM191 to a EMC²-Z7030 Zynq Module and a software package that will allow control of EMC² + FM191 from any Ethernet port. The framework will be http://www.ros.org/ compatible.

All components on FM191-RUA1 are extended temperature range, suitable for industrial applications in terms of temperature, but does not comply to any IP rating for moisture.

Verification, Review & Validation Procedures to be carried out in accordance with the <u>Sundance Quality Procedures</u> (ISO9001-2015).

8 Safety

This module presents no hazard to the user when in normal use.

9 EMC

The FM191-RUA1 system is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate enclosure.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

10 Ordering Information

Order number:

FM191-R	ADC Input, DAC Output and Digital I/O
FM191-RU	As above, but added SEIC with I/O + USB3.0
FM191-RUA1	As above, but added the GPIO extension board

oi928-Z7030-R	$EMC^2-Z7030 + FM191-R$
oi928-Z7030-RU	EMC ² -Z7030 + FM191-RU
oi928-Z7030-RUA1	EMC ² -Z7030 + FM191-RUA1