ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION –

Lesson-12: ARM

The ARM architecture processors popular in Mobile phone systems

ARM Features

- ARM has 32-bit architecture but supports 16 bit or 8 bit data types also.
- ARM is programmable as little endian or big endian data alignment in memory.
- ARM provides the advantage of using a CISC in terms of functionality, along with the advantage of an RISC in terms of faster program implementation as well as reduced code lengths.

ARM7, ARM9 and ARM 11 microprocessors

- ARM processor has an RISC core for processing
- Combination of RISC and CISC features—ARM supports to a complex addressing modes based instruction set

In-built compilation unit

- Compiles the CISC instructions into RISC formats, which are then implemented by the RISC core of the processor.
- Internally the implementation for many instructions is like in an RISC (without the micro-programmed unit)

Jazelle technology

- Faster Java codes execution

ARM Thumb 16-bit instructions

- Thumb Set designed for 16-bit word lengths and instructions, which internally executes by same 32-bit core.
- Instruction fetch of 2 bytes in Thumb mode in place of 4 bytes in ARM mode.
- Data alignment at steps of 2 bytes in Thumb mode in place of 4 bytes in ARM mode Memory savings of up to 35%, over the equivalent 32-bit code, while retaining all the benefits of a 32-bit system (such as access to a full 32-bit address space).
- Enables 32-bit performance at the 8/16-bit system cost in terms of memory needs.

Thumb and 32-bit ARM modes

- Switch from one mode to another
- No overheads (in terms of time and memory) in moving between Thumb and the normal ARM state of the codes. Two states are compatible on a normal basis.
- Gives code designer complete control over performance and code-size optimisation

ARM7 versions

- ARM7TDMI® (Integer Core)
- ARM7TDMI-S™, (Synthesisable version of ARM7TDMI)
- ARM7EJ-S™ (Synthesisable core with DSP and Jazelle technology)
- ARM720T™ (cached processor macrocell , 8K Cached Core with Memory Management Unit (MMU) supporting operating systems1 including Windows CE, Palm OS, Symbian OS and Linux)
- 130 MIPS using Dhrystone 2.1 benchmark in typical 0.13µm process

ARM9 versions

- ARM920T (Dual 16k caches with MMU support multiple OSs.
- ARM922T (Dual 8k caches for applications support multiple OSs1.
- ARM940T™ (Dual 4k caches for embedded control applications running a RTOS)
- 32-bit RISC processor core Super scaling 5-stage integer pipeline. 8-entry write buffers to avoid blocking the processor on external memory *writes*
- Achieves 1.1 MIPS/MHz, 300 MIPS (Dhrystone 2.1) in a typical 0.13µm process

ARM11 versions

- Families with ARMv6 instruction set architecture that includes the Thumb® extensions for code density, Jazelle™ technology for Java™ acceleration, ARM DSP extensions, and SIMD media processing extensions. MMU) supporting operating systems1 and palm OS
- 32-bit RISC processor core with 8-stage integer pipeline, static and dynamic branch prediction, and separate load-store and arithmetic pipelines to maximize instruction throughput
- Targets a performance range of Dhrystone MIPS 400 to 1200

Memory Architecture

- ARM7 has Princeton memory architecture.
- ARM9 processor has Harvard architecture

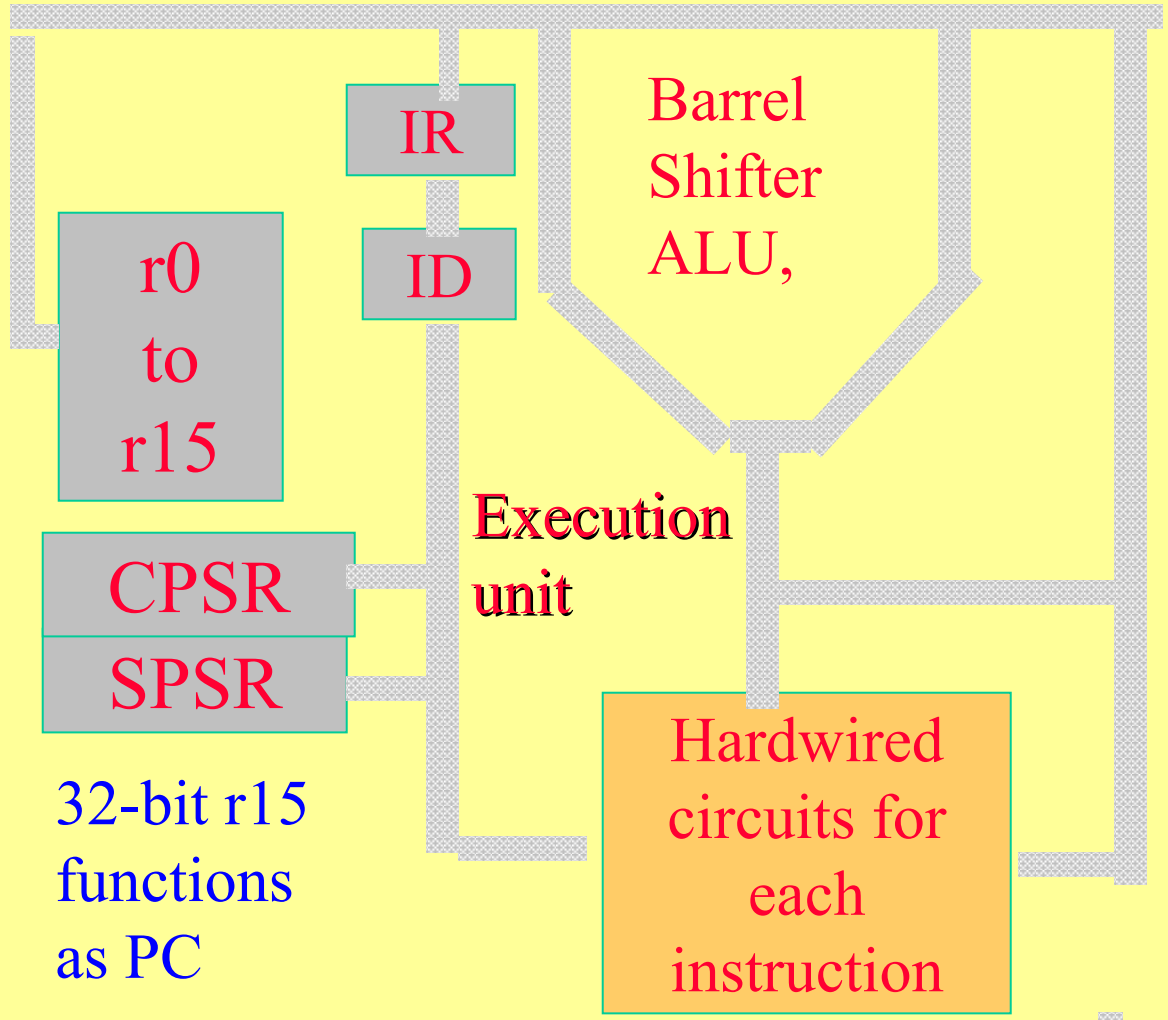
Faster implementation and Reduced code lengths

- Due to the instant availability of the register word to the execution-unit.
- Reduced code lengths— Most instructions use registers as operands.
- Few bits in the instruction specify a register as operand. 8, 16 or 32 bits specify a memory address as operand and the displacement bits in the instruction.

ARM registers

- R0 to R15.
- R15 also function as program counter.
- R14 function as link register.
- R13 may be used as stack pointer
- CPSR (current program status register)
- SPSR (saved program status register).

ARM Architecture



ARM Codes

- ARM Codes─ Forward compatible with higher versions.
- ARM7 codes ─ Forward compatible with ARM9, ARM9E and ARM10 processors as well as Intel XScale micro-architecture.
- ARM9E and ARM 10 families use a Vector Floating Point (VFP) ARM coprocessor, which adds full floating point operands.
- VFP also provides fast development in SoC design when using tools like MatLab®.
- Applications are in image processing (scaling), 2D and 3D transformations, font generation and digital filters.

ARM Intelligent Energy Manager (IEM) technology

- Advanced algorithms to optimally balance processor workload and energy consumption.
- Maximizes system responsiveness.
- IEM works with the operating system and mobile OS.
- Application running on a mobile phone dynamically adjusts the required CPU performance level.

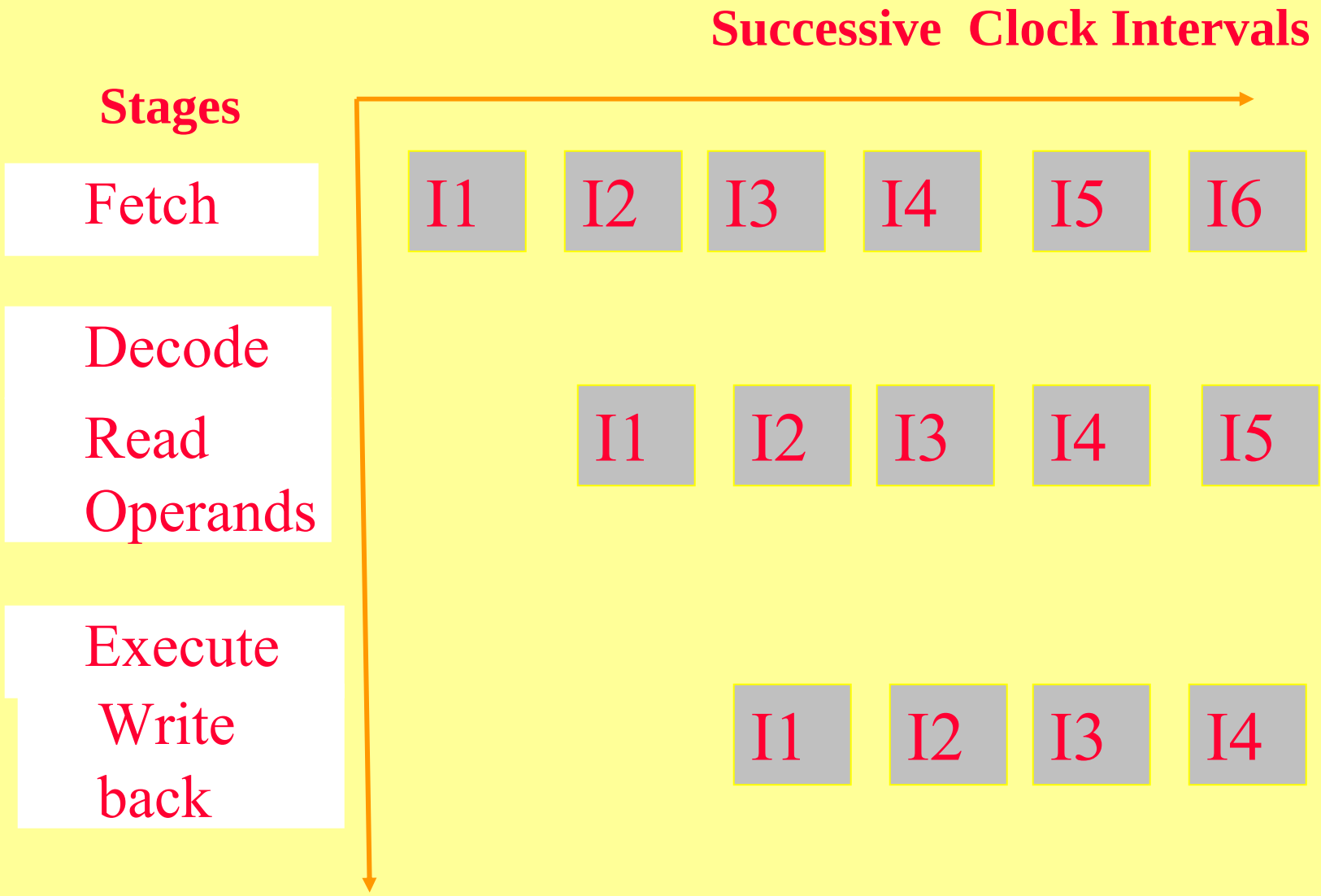
ARM processors AHB (AMBA Advanced High Performance Bus) interface

- AMBA an established open source specification for on-chip interconnects.
- AMBA serves as a framework for SoC designs and development of the IP library.
- AHB support in all new ARM cores.

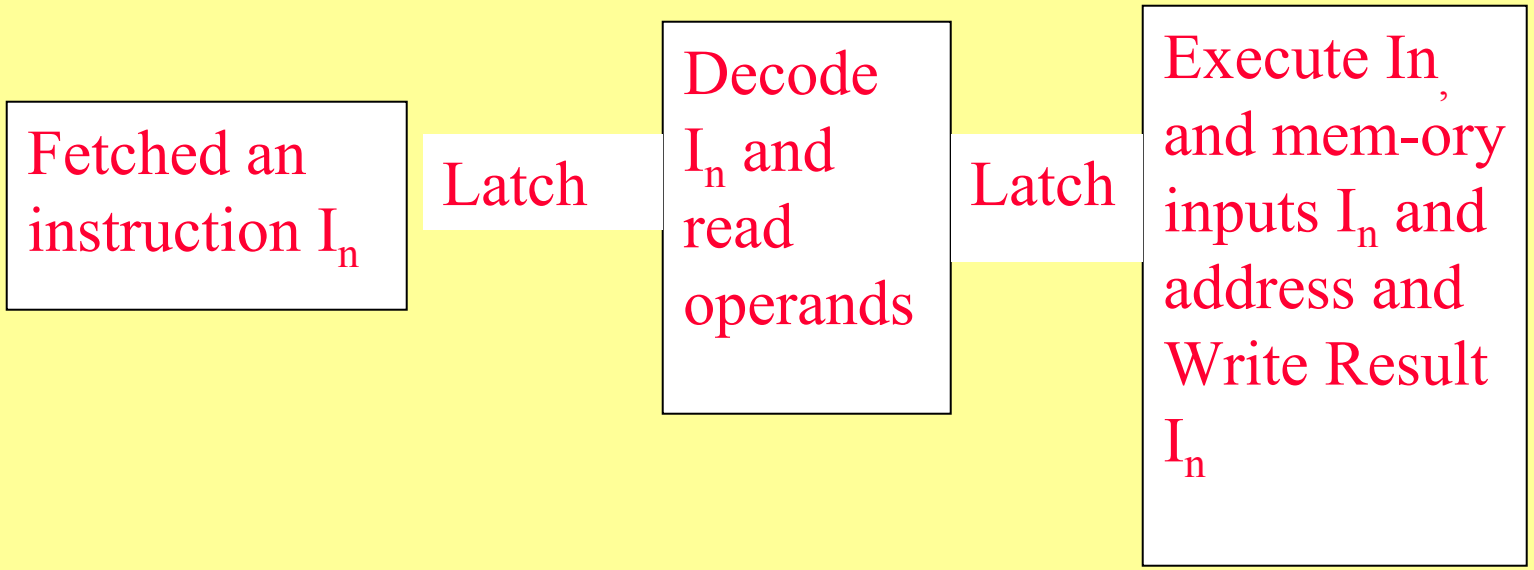
AHB

- Provides a high-performance and fully synchronous back plane. (Back plane means additional set of controllers, which can access another common bus, which is distinct from system bus in a multilevel buses in the system.)
- Multi-layer AHB in version ARM926EJ-S and all members of the ARM10 family represents a significant advancement. It reduces access latencies and increases the bandwidth available to multi-master systems

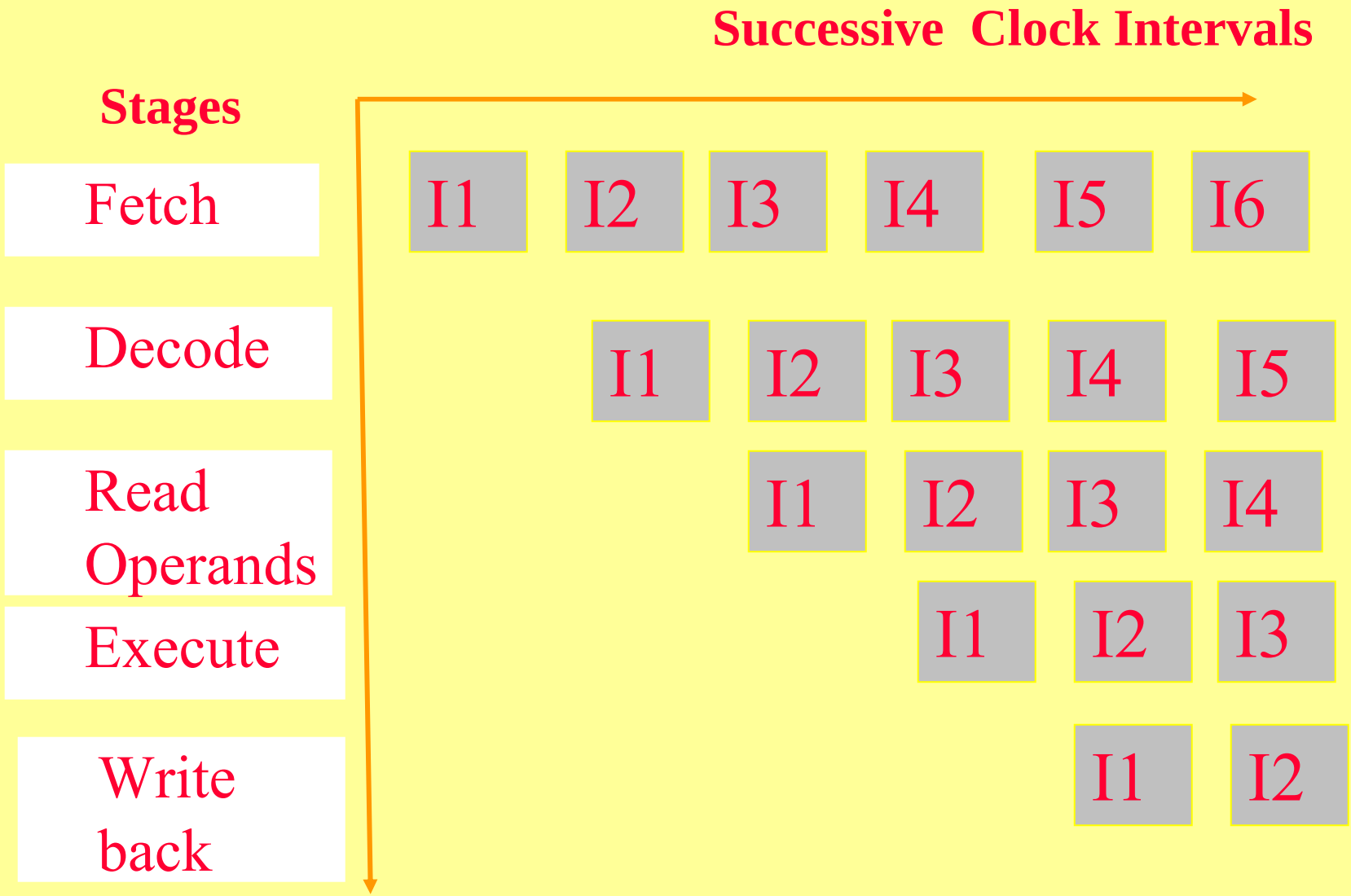
3- stage pipeline in ARM7



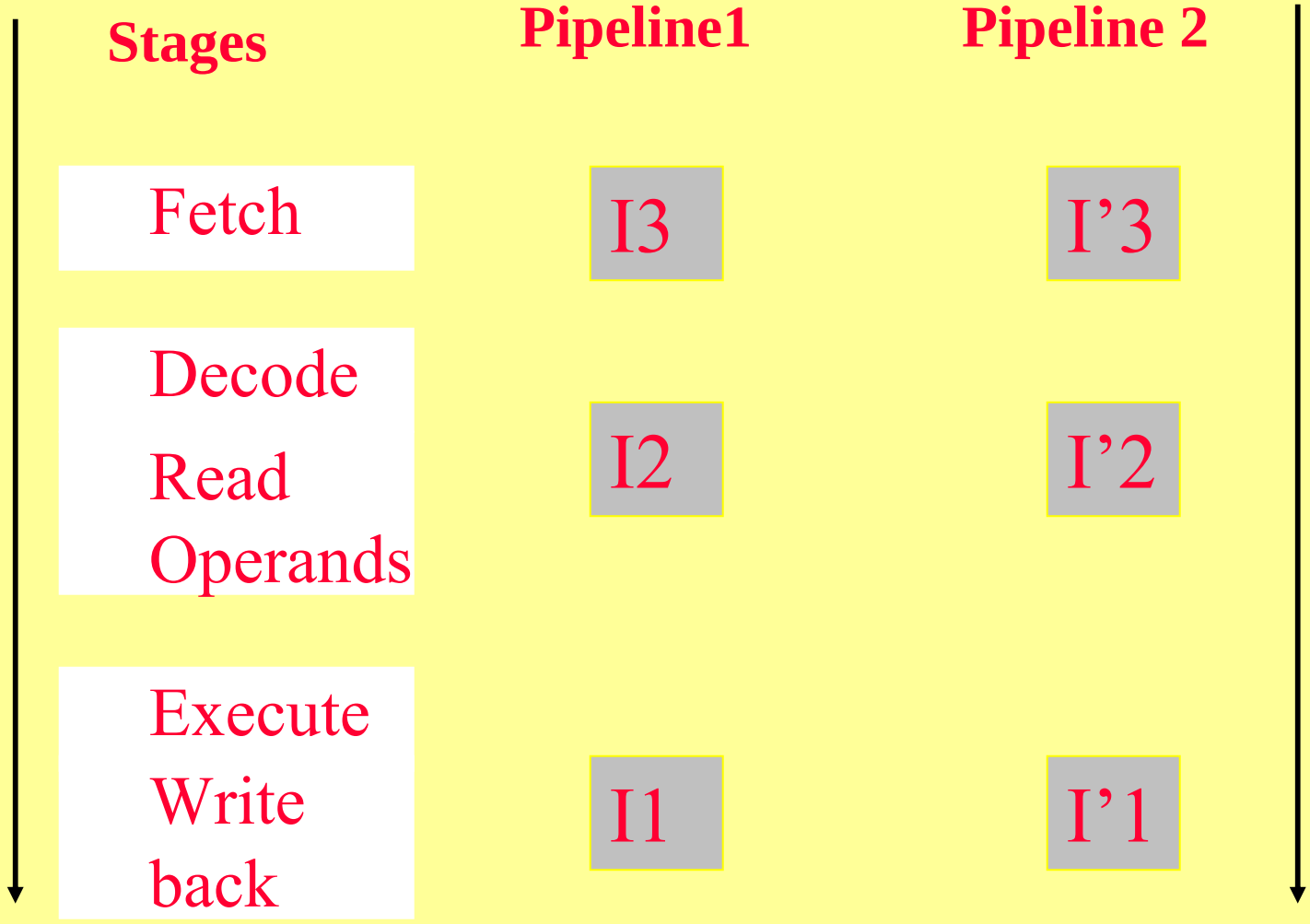
Pipeline and Latch



5- stage pipeline in ARM 9



Super scaling in ARM



Summary

We learnt

- ARM Architecture
- 32- address bus and 64-bit data bus
- Programmability as Little endian or Big endian
- Princeton Memory in ARM7 and Harvard in ARM9
- 16 Registers with R15 as Program counter

Summary

We learnt

- 16-bit Thumb set for 16-bit instructions to reduce external memory requirement
- AHB
- 3 stage pipeline in ARM7 and 5 in ARM9

End of Lesson 12 of Chapter 2