ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION –

Lesson-11: 80x86 Architecture

The 80x86 architecture processors popular since its application in IBM PC (personal computer).

First Four generations of 80x86

- Four generations are 8086, 80286, 80386, 80486 generations.
- The 80x86 family of processors first processor 16-bit 8086 (1981).
- 80x86 has 32-bit architecture since 80386.

Next four generations of 80x86

- Pentium is fifth generation architecture (1994) based on 32-bit 80386.
- Pentium 4 is seventh and Xeon and Core2 eighth-generation architectures.
- Core2 means dual core architecture.
- Itanium is based on 64-bit architecture, which simulates the 80x86 architecture by software

80x86 architecture Registers

- The original 8086 architecture consists of general purpose registers AX, BX, CX and DX. Each can be considred as two 8-bit registers. For example, AX as AL (A lower byte) and AH (A upper byte)
- 32-bit extension has EAX, EBX, ECX, EDX. EAX register. Each can be considred as two 16-bit registers. AX then has lower 16-bit of EAX

80x86 processor architecture registers

16- bits registers

CS, DS, SS, ES, FS and GS

16-, 32- or 64 bit registers

IP Instruction (code) pointer

SI Source index pointer

DI Destination index pointer

SP Stack pointer

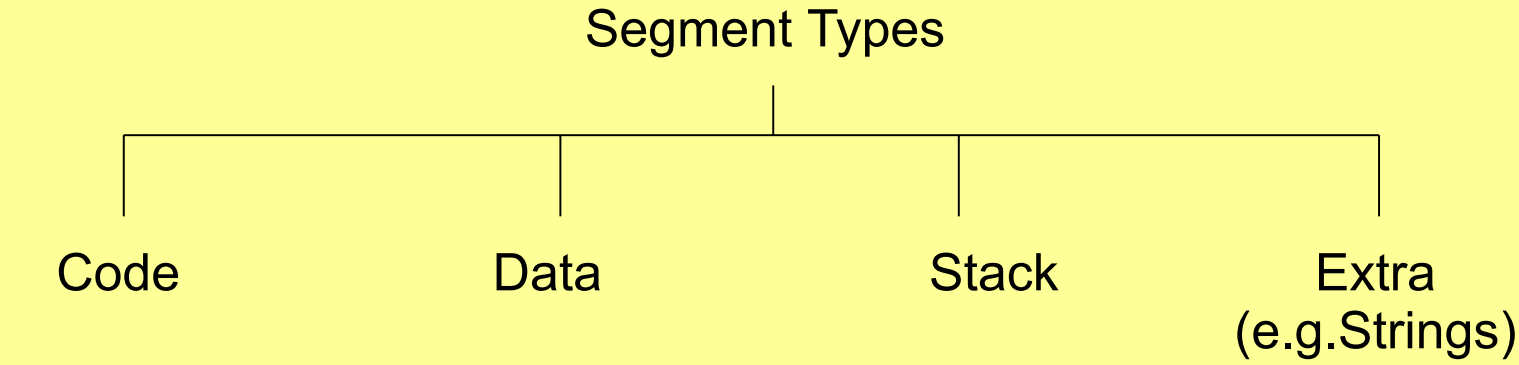
BP Base pointer

8-, 16-, 32- or 64 bit general purpose registers

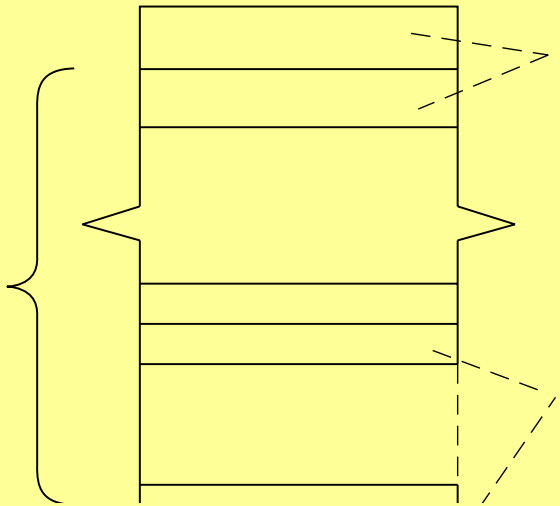
A, B, C and D

For example, 16-bit AX, BX, CX, DX

Code, data, stack and stack segmentations



A
Segment
of
Length
1 B to
4 GB
(Overlapping among
segments permitted)



Fixed size 4 kB
Pages

Pages Frames

Pointers

IP ─ for instruction of 16-bits address and

CS ─ for 16-bit program code segment address upper bits.

SI ─ for index of source operand and

DI ─ for 16-bit index of destination.

BP ─ for memory offset of 16-bits address and

DS ─ for 16-bit data memory segment address upper bits.

Little Endian and Unaligned data in Memory

- 16-bit or 32-bit or 64-bit words store as little endian.
- Data need not by aligned at the in addresses in multiples of 2 or 4 and can start from any address.

8086 Interrupt levels

- Supports 256 for the hardware as well as software interrupts and supports nested interrupts.
- ISR can be interrupted and higher priority ISR can execute in between.

Characteristics of CISC addressing modes in 80x86

- First or second operand a memory address
- Present generation 80x86 architecture decodes a CISC instruction and create mico-operations, which implement on a microarchitecture of RISC.
- Register-relative addressing (using small immediate offsets) an important method of accessing operands, especially on the stack. Much work has therefore been invested in making such accesses as fast as register accesses, i.e. a one cycle instruction throughput in most circumstances.

IO Features in 80x86

- IO mapped IO.
- IO address of 16-bit for an IO byte.
- Access the I/O by separate IN and OUT instructions.
- Four input and output instructions
- A separate set of addresses from memory for accessing inputs and outputs.
- It simplifies the I/O units interfacing circuit that connects the processor.

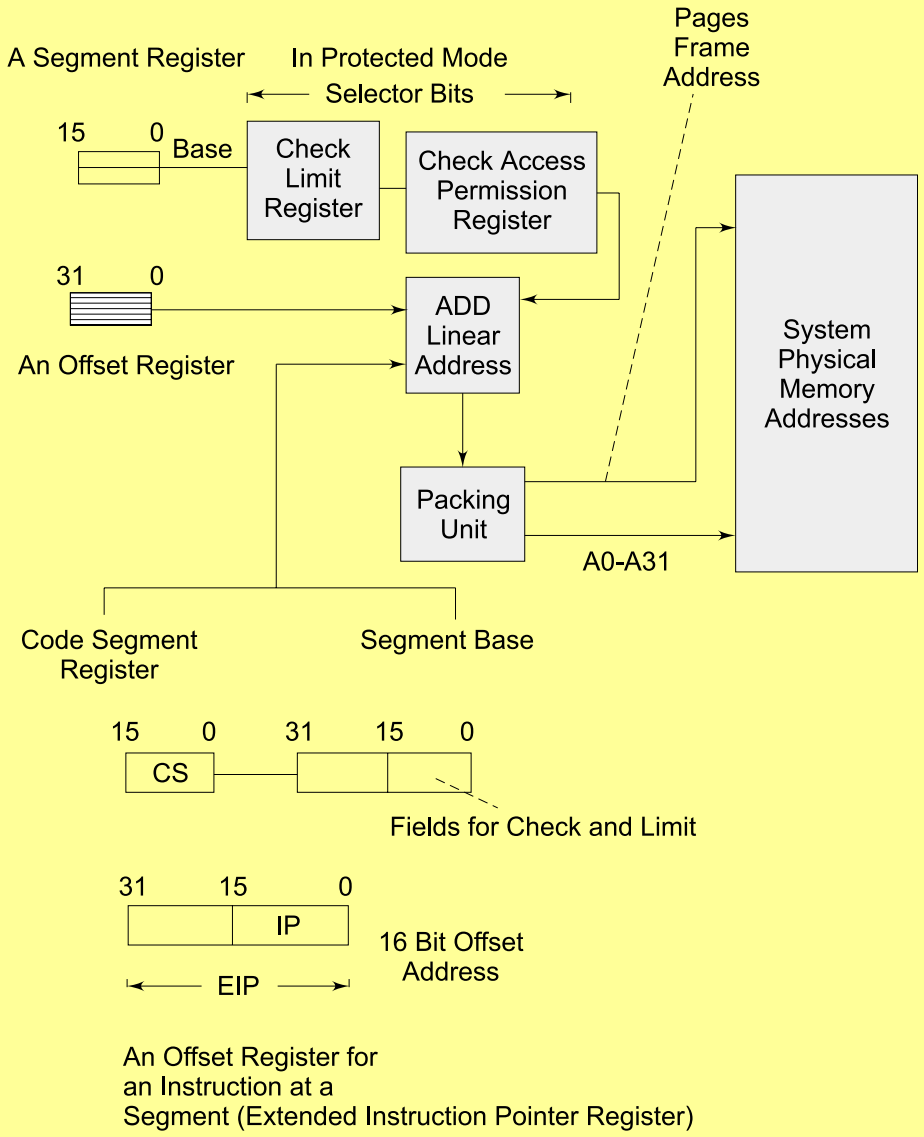
Real mode

- New generation 8086 architecture supports Real mode
- Supports direct access without segmentation to peripheral devices and basic input output subroutines (BIOS)
- Real mode support 20 bit segmentation in stead of 16-bit earlier. Segmnet register has upper 16-bits only. Lower bits are 0s.

Protected mode

- 32- bit protected mode is also provided and support pages in memory.

Physical Addresses from Virtual addresses



(b)

Physical Addresses from Virtual addresses

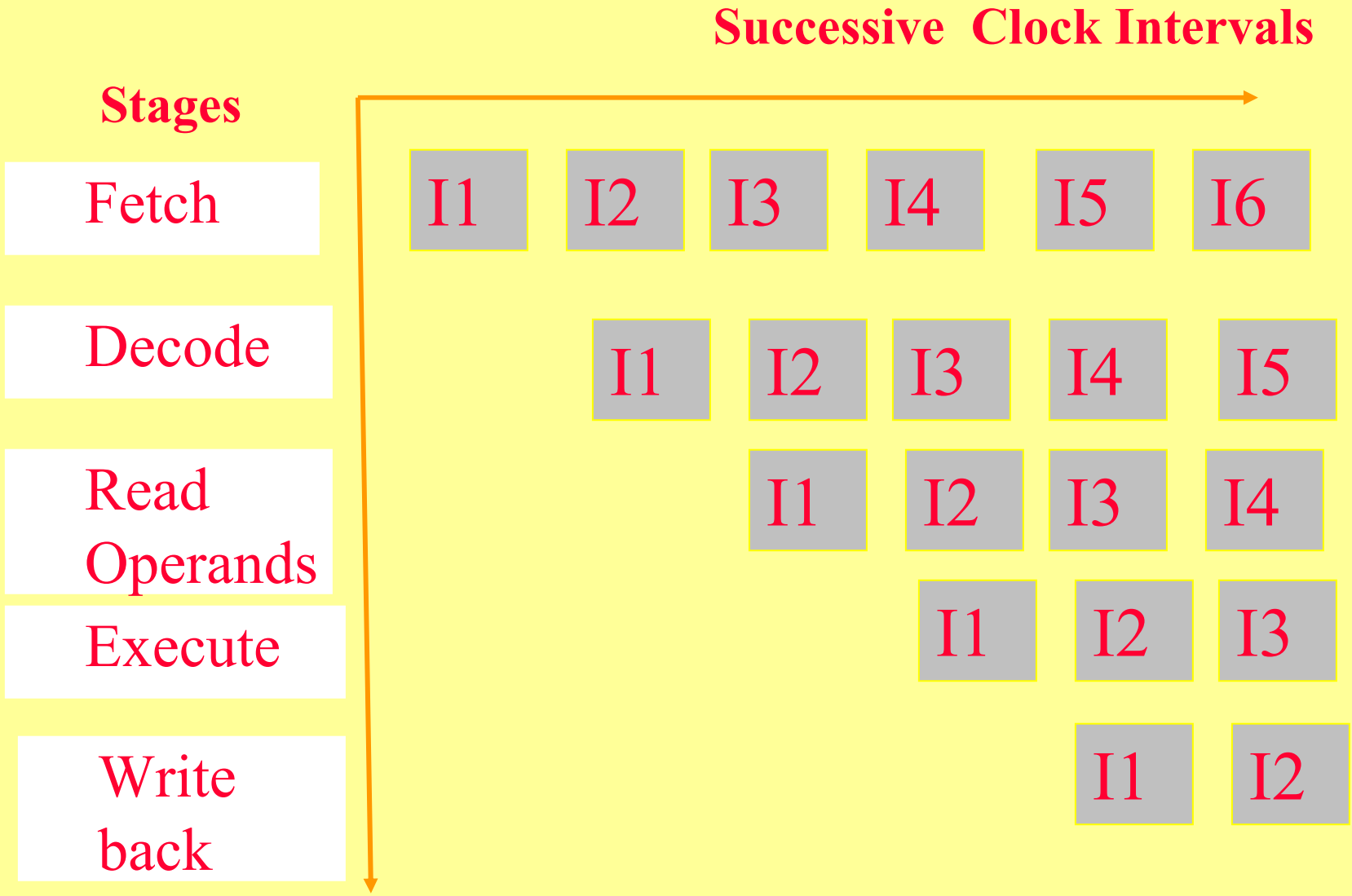
Features in 8086architectures

- Instruction, Branch Target and Data Cache
- Memory-Management unit (MMU)
- Floating Point Processing unit
- System Register Set

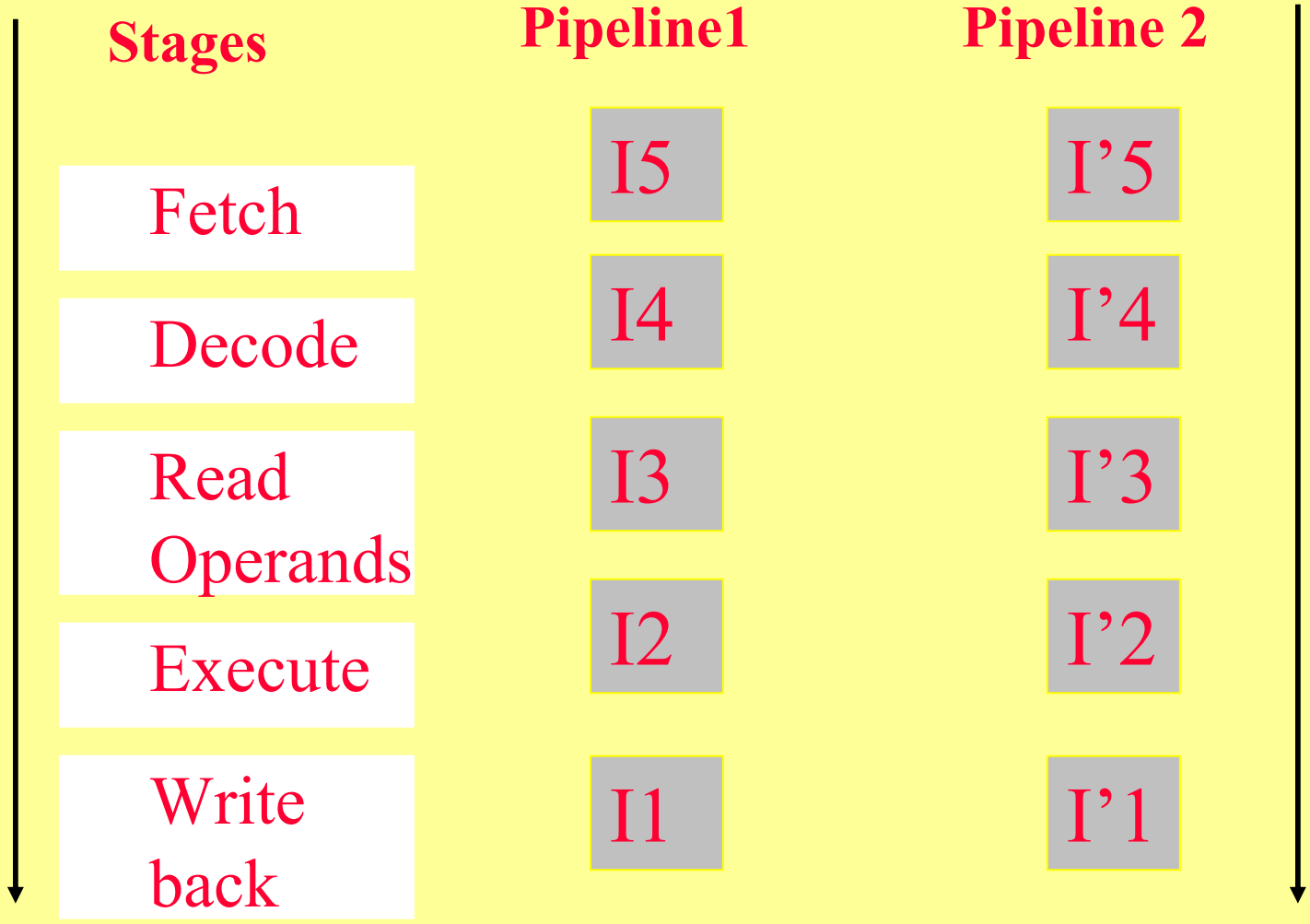
Features in 80x86

- 8086 supports may OSs including Windows and and multitasking operating systems.
- Latest 80x86 architectures support thread handling, integer SIMD and SIMD extension instruction sets.

5- stage pipeline in Pentium



Super scaling in Pentium



Summary

We learnt

- 80x86 Architecture
- 32- or 64-bit address bus and 8-, 16-, 32 and 64-bit data bus
- Segment registers
- 8-, 16-, 32- and 64-bit Registers
- Little Endian
- No data alignment need
- Virtual Memory Support

Summary

We learnt

- IO mapped IOs
- 256 Interrupt modes
- Real and protected Mode working

End of Lesson 11 of Chapter 2