ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION –

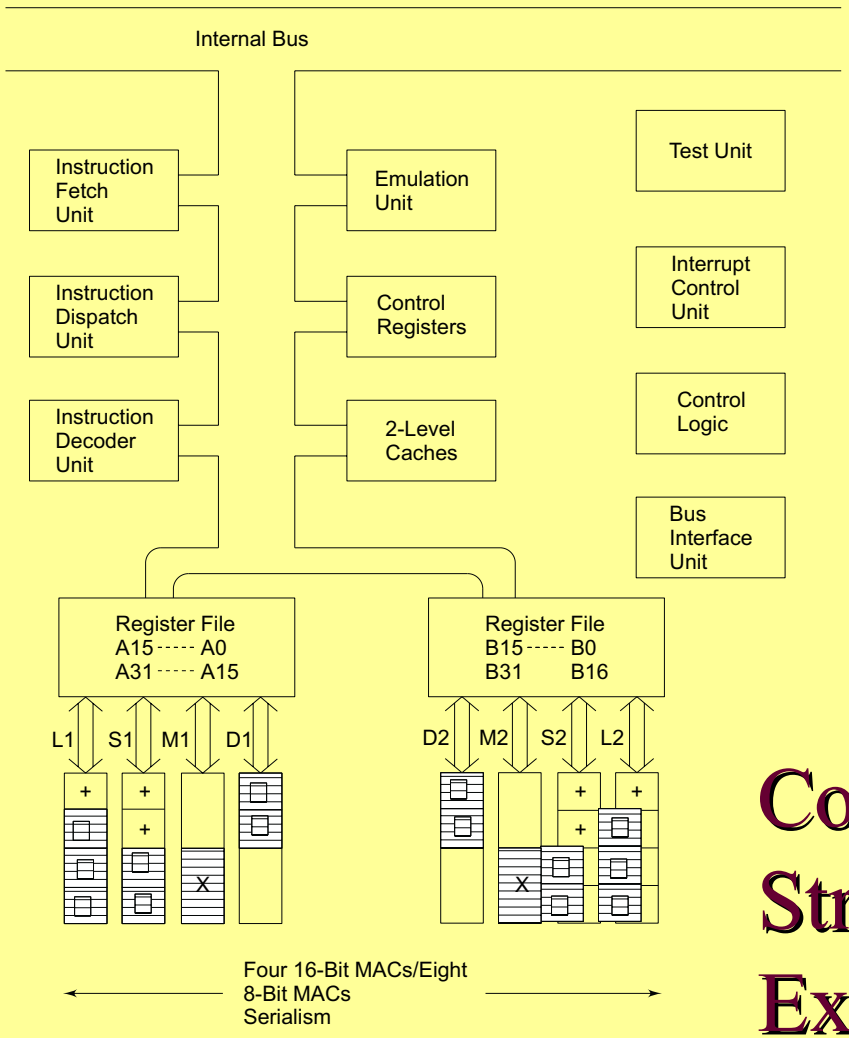
Lesson-15: DSPs

DSP

- Advanced signal processor circuits
- MAC (Multiply and Accumulate) unit (s)─ provides fast multiplication of two operands and accumulating results at a single address.
- MAC unit computes fast an expression such as the following summation. $y_n = \Sigma(a_i \times x_{n-i})$ where the sum is made for $i = 0, 1, 2, \ldots, N\text{-}1$. Here i, n and N are the integers, a_i is a coefficient, x_j is independent variable or an input element and y_k is the dependent variable or an output element.

DSP

- DSP processors invariably have Harvard architecture.
- Caches are organized in Harvard architecture (separate I-cache and D-Cache
- Basic Units: MDR, Internal Bus, Data bus, Address bus, control bus, Bus Interface Unit, Instruction fetch register, Instruction decoder, Control unit, Instruction Cache, Data Cache, multistage pipeline processing, multi-line superscalar processing for obtaining processing speed higher than one instruction per clock cycle, Program counter



L1 : ALU Auxiliary Logic Unit L2 : ALU S2 : Auxiliary

M1: Multiplier Unit M2: Multiplier
D1 :Divider Unit D2 :Divider Unit

Eight 32-Bit Instruction

RIS Parallelism/
Note: Floating Point Units in C67x

Core and Special Structure units in an Exemplary DSP, TMS320C64x DSP

DSP special structural units

- Packed Data processing
- Parallel Execution MAC units
- Special Instructions
- Instruction Packing unit

Parallel Processing features

- Supports processing instruction level parallelism as well as memory access parallelism.
- Multiple data accesses in a single instruction

Summary

We learnt

- DSP for digital signal processing
- Harvard architecture
- MAC (Multiply and Accumulate) unit
- VLIW (instruction packaging unit)
- TMS320C64x

End of Lesson 15 of Chapter 2