8051 AND ADVANCED PROCESSOR ARCHITECTURES –

Lesson-5: Hardware Interrupts of 8051

Interrupt Sources

- External INT0 interrupt
- T0 overflow interrupt
- External INT1 interrupt
- T1 overflow interrupt
- SI serial UART or Synchronous mode interrupt
- SI synchronous serial mode interrupt (separate in few families of 8051)
- Timer 2 interrupt in 8052

SFR IE for interrupts enabling bits

SFR to mask (disable) or unmask (enable) the interrupts in 8051

- Programming of SFR IE (Interrupt Enable) register at address 0xA8 for the byte or
- Programming of IE using Bit addresses 0xA8 to 0xAF for the individual bits

SFR IP for interrupt priority bits

- Individual interrupt priorities set high or low bits
- Set priorities in IP override default priorities for executing the ISRs
- Byte address 0xB8 for the byte and at bit addresses 0x88 to 0x8C or 0x8D or 0x8E for the individual bits in the register, an instruction can define that a given interrupt is of higher (=1) or lower priority (=0) among the various interrupts

8051 system Interrupt Features

- 8051 permits when executing low- priority ISR the in-between program flow on interrupt to higher priority ISR
- Permits masking all by a primary level bit or individual sources by secondary level bits by setting bits in SFR IE
- Assigns default priorities
- Permits overriding of default priorities by setting bits in SFR IP

Vector Addresses

- An address from where either an ISR of maximum 8-bytes executes or a Jump to a programmed ISR starting address takes place
- When EA bit (primary level interrupt bit) is set as well as specific interrupt bit (secondary level interrupt bit) is set

External hardware Interrupts INT0 and INT1

programmable for

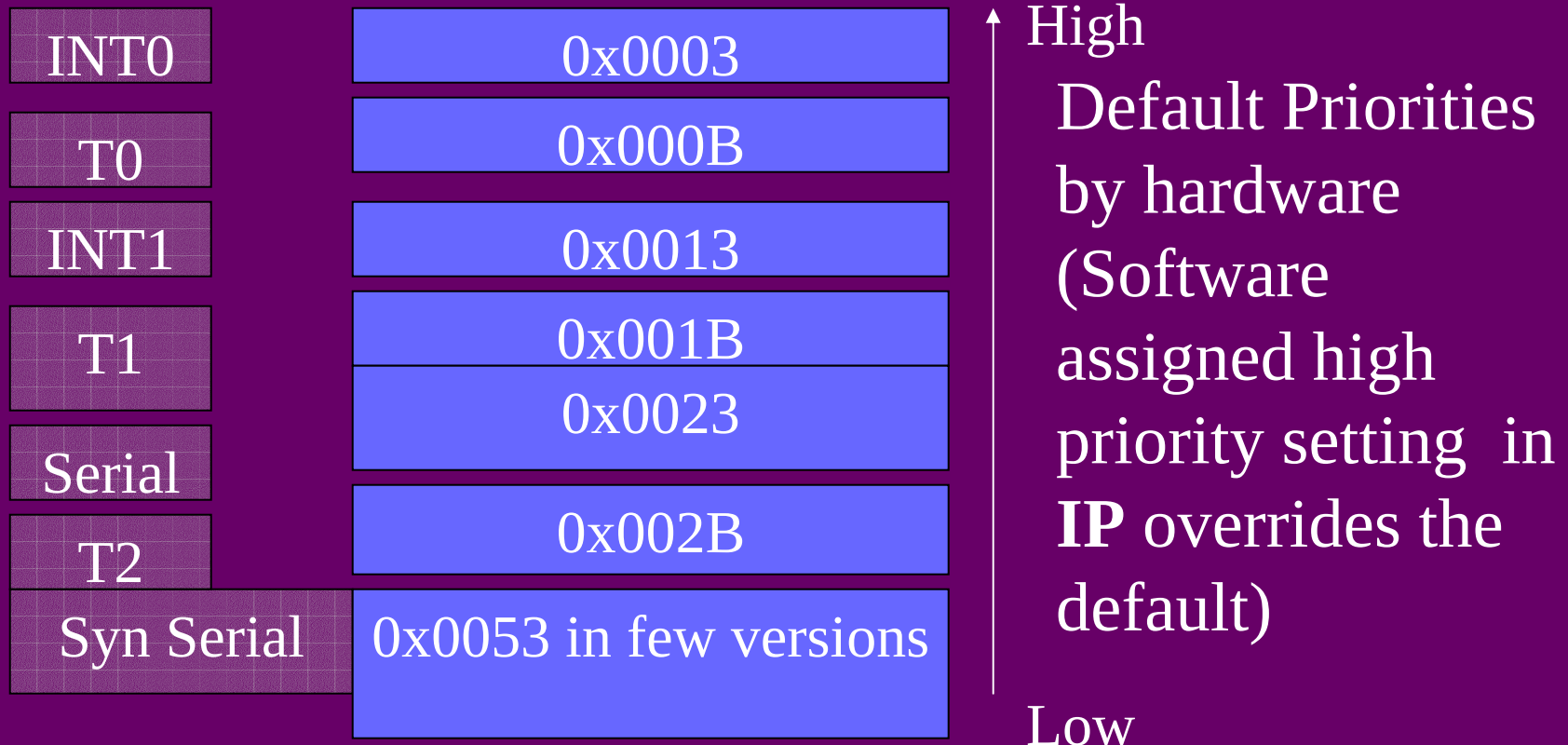
- Two external interrupt pins, INT0 and INT1 at P3.2 and P3.2 used for interrupt
- P3.2 and P3.3 as pins for INT0 and INTI external interrupt pins when bit 7 IE (interrupt enable SFR) EA (enable all) bit is 1, and bits 0 and 2 are 1 and 1, respectively
- Programmed by TCON lower 4 bits and the IE register bits IE.2 and IE.0

INT1 and INT0 status bits

- Status bit TCON.3 for status of interrupt at INT1
- TCON.3 auto resets to 0 when ISR for servicing INT1 interrupt starts.
- Status bit TCON.1 for status of interrupt at INT0 and
- TCON.1 auto resets to 0 when ISR for servicing INT0 starts.

INT1 and INT0 Edge or level type control bits

- TCON.2 for type of interrupt at INT1 and is 1 if it is edge-triggered type else 0.
- TCON.0 for type of interrupt at INT0 and is 1 if it is edge-triggered type else 0.



Vector Addresses and Default priorities

Summary

We learnt

- Interrupt sources
- Interrupt system features
- Vector addresses
- Default priorities
- SFR IE for enabling all and enabling individual sources
- SFR IP for setting priority low or high for individual sources of interrupts

End of Lesson 5 of Chapter 2