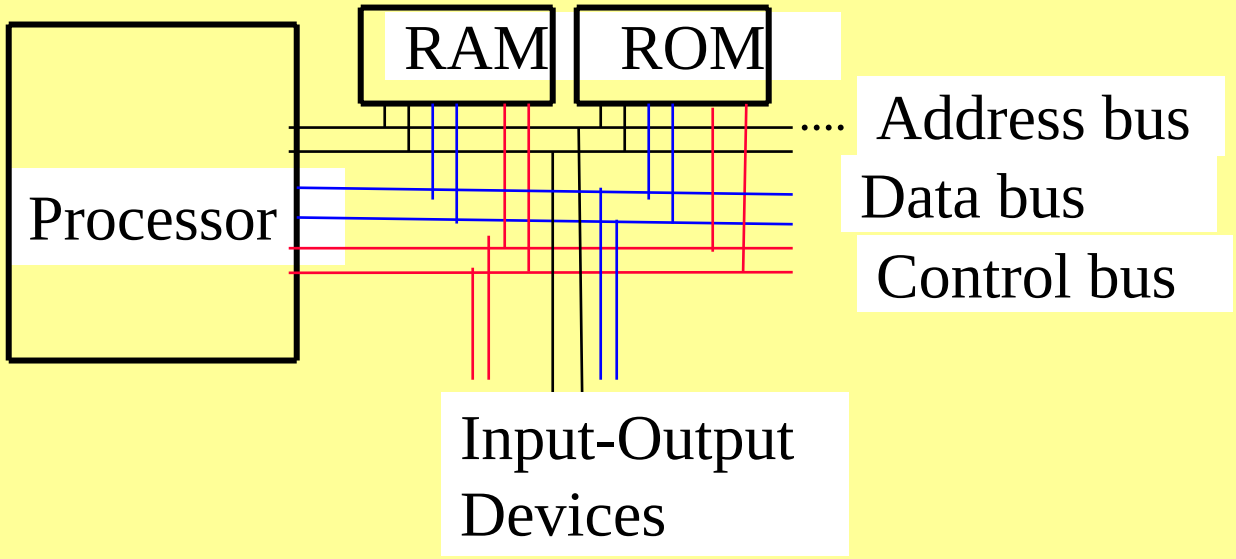
ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION –

Lesson-16: Processor organisation and Performance Metrics

1. Processor Organisation

Processor, Memory and buses



Processor

- *ALU*.
- Processor circuit does sequential operations and a *clock* guides these.
- P*rogram counter* and *stack pointer*, which points to the instruction to be fetched and top of the data pushed into the stack.
- Certain processor have on-chip memory management unit (MMU).

Registers

- General-purpose registers.
- Registers organize onto a common internal bus of the processor. A register is of 32, 16 or 8 bits depending on whether the ALU performs at an instance a 32- or 16- or 8-bit operation

CISC

- Processor may have CISC (Complex Instruction Set Computer) or RISC (Reduced Instruction Set Computer) architecture may affect the system design.
- *CISC* has ability to process complex instructions and complex data sets with fewer registers as it provides for a large number of addressing modes.

RISC

- Simpler instructions and all in a single cycle per instruction.
- New RISC processors, such as ARM 7 and ARM9 also provide for a few most useful CISC instructions also.
- *CISC converges to a RISC implementation* because the most instructions are hardwired and implement in single clock cycle

Interrupts

- Processor provides for the inputs for *external interrupts* so that the external circuits can send the interrupt signals
- May possess an *internal interrupt controller* (handler) to program the service routine priorities and to allocate vector addresses.

DMA (Direct Memory Access) Controller

- External Devices can directly write and read into the blocks of RAM using the DMA controller, when the buses are not in use of the processor

Direct memory access (DMA) Controller

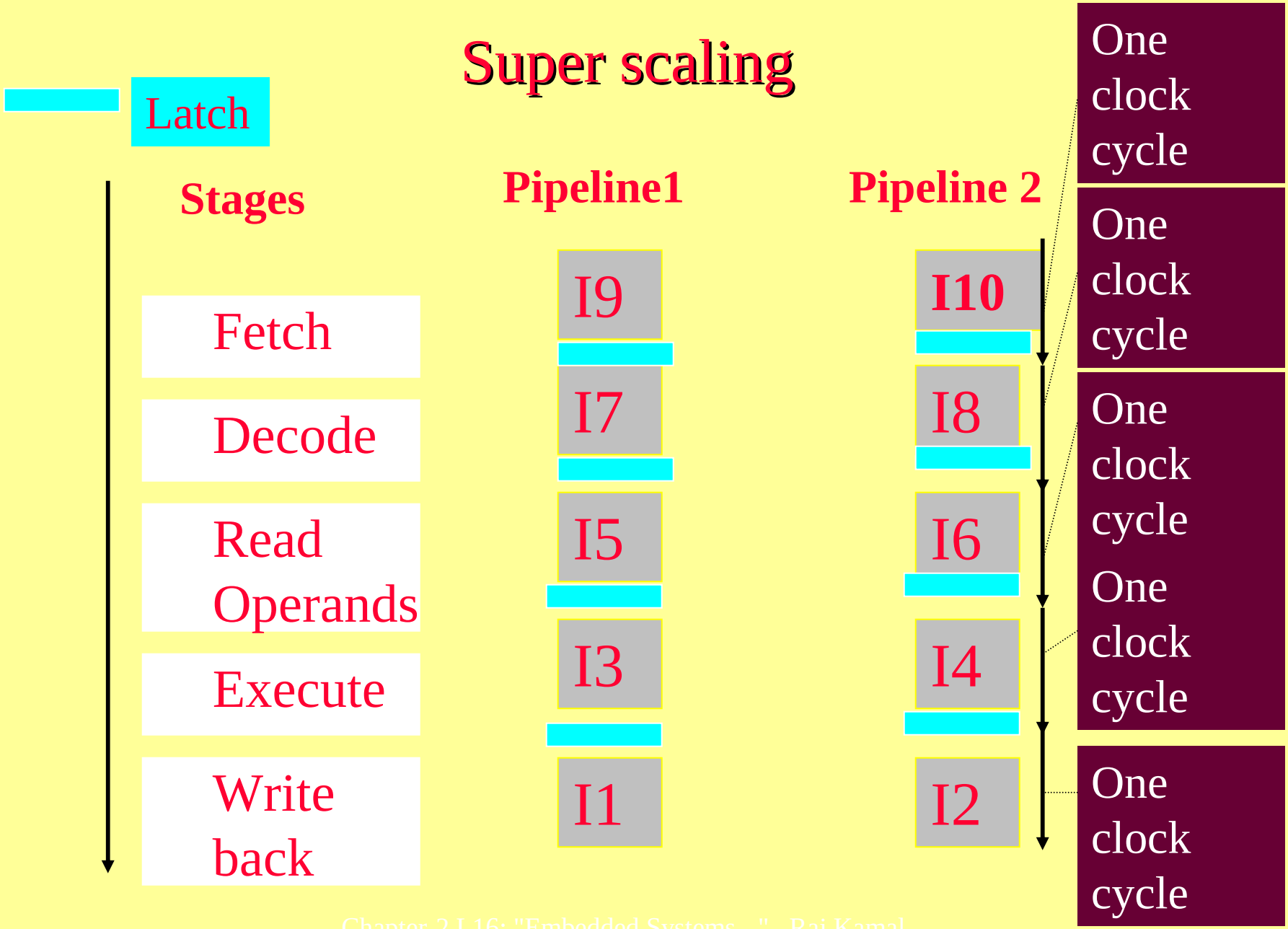
- Multiple DMA channels on chip.
- When there are number of I/O devices and an I/O device needs to access a multi byte data set_fast, the system memory on-chip DMA controller help greatly

2. INSTRUCTION LEVEL PARALLELISM

Instruction level parallelism (ILP)

- Execute several instructions is parallel. Two or more instructions execute in parallel as well as in pipeline.
- During the in which two parallel pipelines in a processor and two instructions I_n and I_n+1 executing in parallel at the separate execution units

Super scaling



3. Processor Performance Metrics

Metrics

1) MIPS – Million Instructions Per Second
2) MFLOPS – Million Floating Point Operations Per Second
3) Dhrystone/s – Number of times a benchmark program called Dhrystone program can run per second.[1MIPS = 1757 Dhrystone/s]

Embedded Benchmark Consortium (EEMBC) five-benchmark program suites

- Telecommunications
- Consumer Electronics
- Automotive and Industrial Electronics
- Consumer Electronics
- Office Automation.

Summary

We learnt

- Processor, address, data and control buses and Memory
- CISC and RISC
- Instruction Level Parallelism
- Performance Metrics

End of Lesson 16 of Chapter 2