8051 AND ADVANCED PROCESSOR ARCHITECTURES – Lesson-6: REAL WORLD INTERFACING - Part 1

1. Interfacing Using System Bus

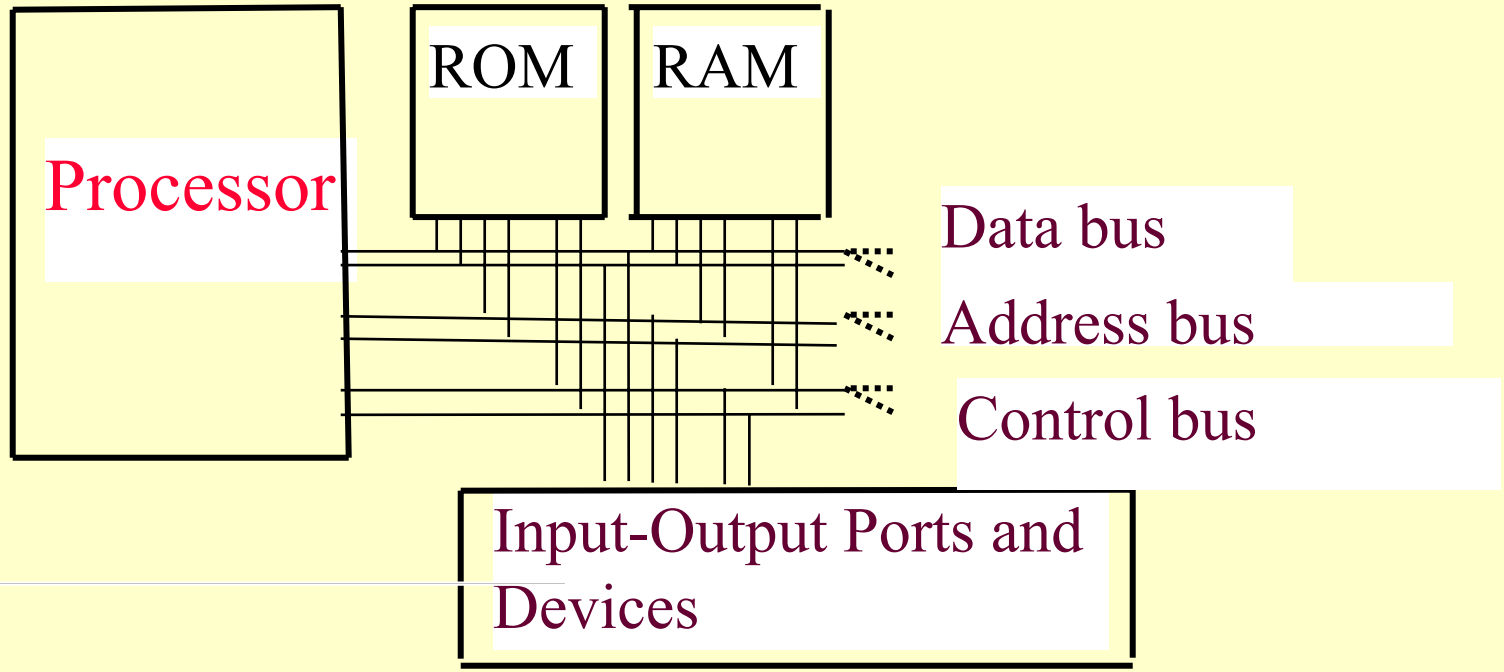
Interfacing of processor, memory and IO devices using memory system bus

- System bus ─ interconnections for a simple bus structure has three sets of signals
- System bus ─ defines by address bus, data bus, and control bus
- A system-bus interfacing-design is according to the timing diagrams of processor signals, speed, and word length for instructions and data.

Processor internal bus(es) and external bus(es).

- Characteristics differ in the system

Interconnections for a simple bus structure



Interfacing of processor, memory and IO devices using memory system bus

Address Bus

- Processor issues the address of the instruction byte or word to memory system through the address bus.
- Processor execution unit, when required, issues the address of data (byte or word) to be read or written using the memory system through address bus.
- The address bus of 32-bits used to fetch the instruction or data from an address specified by 32-bit number.

EXAMPLE

- Let a processor at the start reset the program counter at address 0. Then the processor issues address 0 on the bus and the instruction at address 0 is fetched from memory on reset
- Let a processor instruction be such that it needs to load register r1 from the memory address M. The processor issues address M on the address bus and data at address M is fetched.

Data Bus

- Instruction fetch— Processor issues the address of the instruction, it gets back the instruction through the data bus.
- Data Read— When it issues the address of the data, it loads the data through data bus.
- Data Write— When it issues the address of the data, it stores the data in the memory through the data bus. A data bus of 32-bits fetches, loads, or stores the instruction or data of 32-bits.

EXAMPLE

- Processor issues address *m* for an instruction, it fetches the instruction through data bus from address *m*. [For a 32-bit instruction, word at data bus from addresses m, m + 1, m + 2, and m + 3.]
- Instruction executes for store of register r1 bits to the memory address M, the processor issues address M on the bus and sends the data at address M through the data bus. [For 32-bit data, word at data bus sent to the memory addresses M, M + 1, M + 2, and M + 3.]

Control Bus

- Issues signals to control the timing of various actions during interconnection.
- Signals synchronize all the subsystems.
- *address latch enable* (ALE)[Address Strobe (AS) or address valid, (ADV)],
- memory ‘read’ (RD) or ‘write’ (WR) or IO ‘read’ (IORD) or ‘write,’(IOWR) or ‘data valid’(DAV)
- Other control signals as per the processor design.

Interrupts and DMA Control Signals

- Interrupt acknowledge (INTA) [on a request for drawing the processor attention to an event]
- INT (Interrupt) from external device interrupt to the system
- Hold acknowledge (HLDA) [on an external hold request for permitting use of the system buses]
- HOLD when external device sends a hold request for direct memory access (DMA).

EXAMPLE

- Processor issues the address, it also issues a *memory-read* control signal and waits for the data or instruction.
- Memory unit must place the instruction or data during the interval in which memory-read signal is active (not inactivated by the processor).

EXAMPLE

- Processor issues the address on the address bus, and (after allowing sufficient time for the all address bits setup) it places the data on the data bus, it also then issues *memory-write* control signal (after allowing sufficient time for the all data bits setup) for store signal to memory.
- Memory unit must write (store) the data during the interval in which memory-write signal is active (not inactivated by the processor).

Program memory access and data buses multiplexed for memory access in Harvard Architecture

- Address and data buses are multiplexed
- Control signal PSEN active when accessing program memory using the address and data buses
- Control signal Read or Write active when accessing data memory using the address and data buses

Time division multiplexed (TDM) address and data bits for the memories

- TDM ─ Different time slots, there are is a different set sets (channel) of the signals. Address signals during one time slot t. and data bus signals in another time slot.
- Interfacing circuit for the demultiplexing of the buses uses a control signal in such systems.

Time division multiplexed (TDM) address and data bits for the memories

- Control signal Address Latch Enable (**ALE)** in 8051, Address Strobe (AS) in 68HC11 and address valid (ADV) in 80196.
- ALE or AS or ADV demultiplexes the address and data buses to the devices

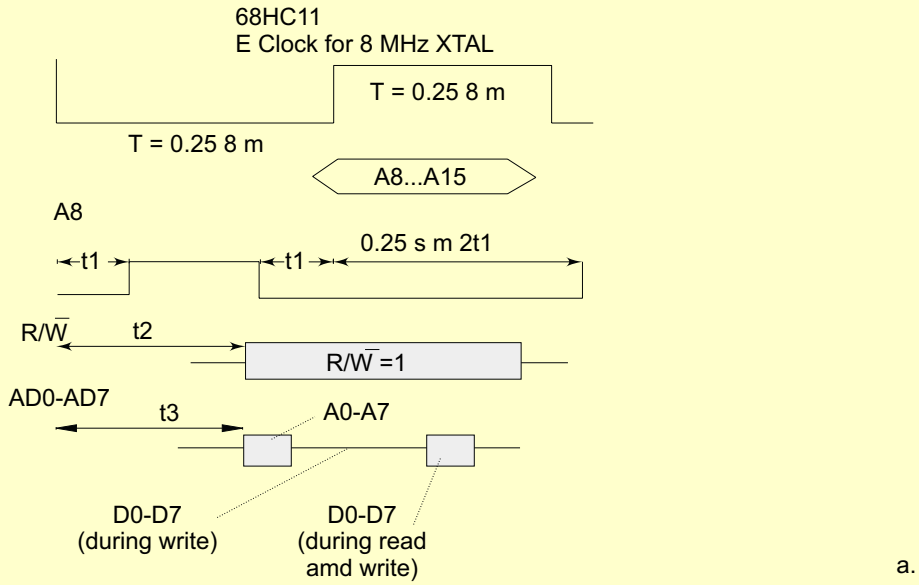
Interfacing circuit using Latch and decoders,

- ALE for latching the address
- PSEN for program memory read using address-data buses
- Each chip of the memory or port that connects the processor has a separate chip select input from a decoder.
- Decoder is a circuit, which has appropriate signals of the address bus at the input and control circuit signals to generate corresponding CS (chip select) control signals for each device (memory and ports)

Interfacing- circuit

- Consists of latches, decoders and demultiplexers
- Designed as per available control signals and timing diagrams of the bus signals.
- Circuit connects all the units, processor, memory and the IO device through the system buses.
- Also called *glue circuit* used as it joins the devices and memory with the system bus and processor
- Can be designed using a GAL (generic array logic) or FPGA

68HC11 Bus signals and Interfacing to memory



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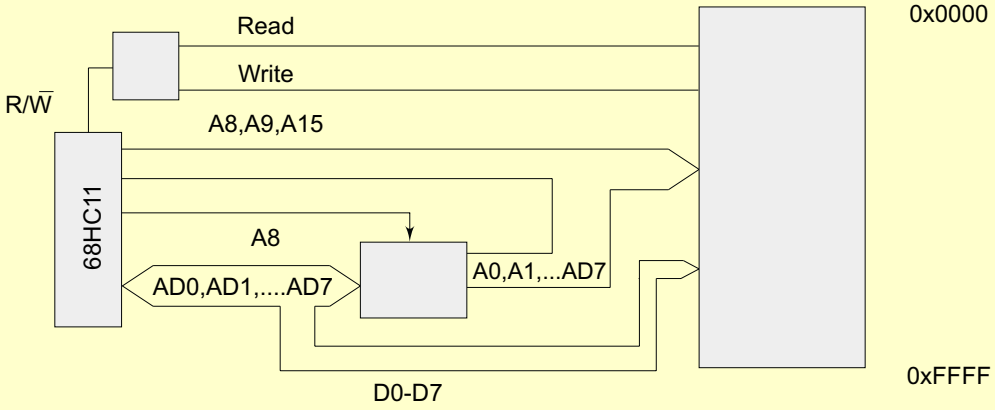

b.

2. Interfacing Using System and IO Buses

System Bus and IO Bus

System bus interconnects

- processor
- memory systems and
- subsystems
- Another set of signals called I/O bus
- Interfacing of processor with system bus at first level and IO bus at second level

Popular IO buses and wireless communication

- PCI Bus interfaces to devices designed to meet the PCI standard.
- USB interfaces to devices designed to meet the USB IOs

Popular IO buses and wireless communication

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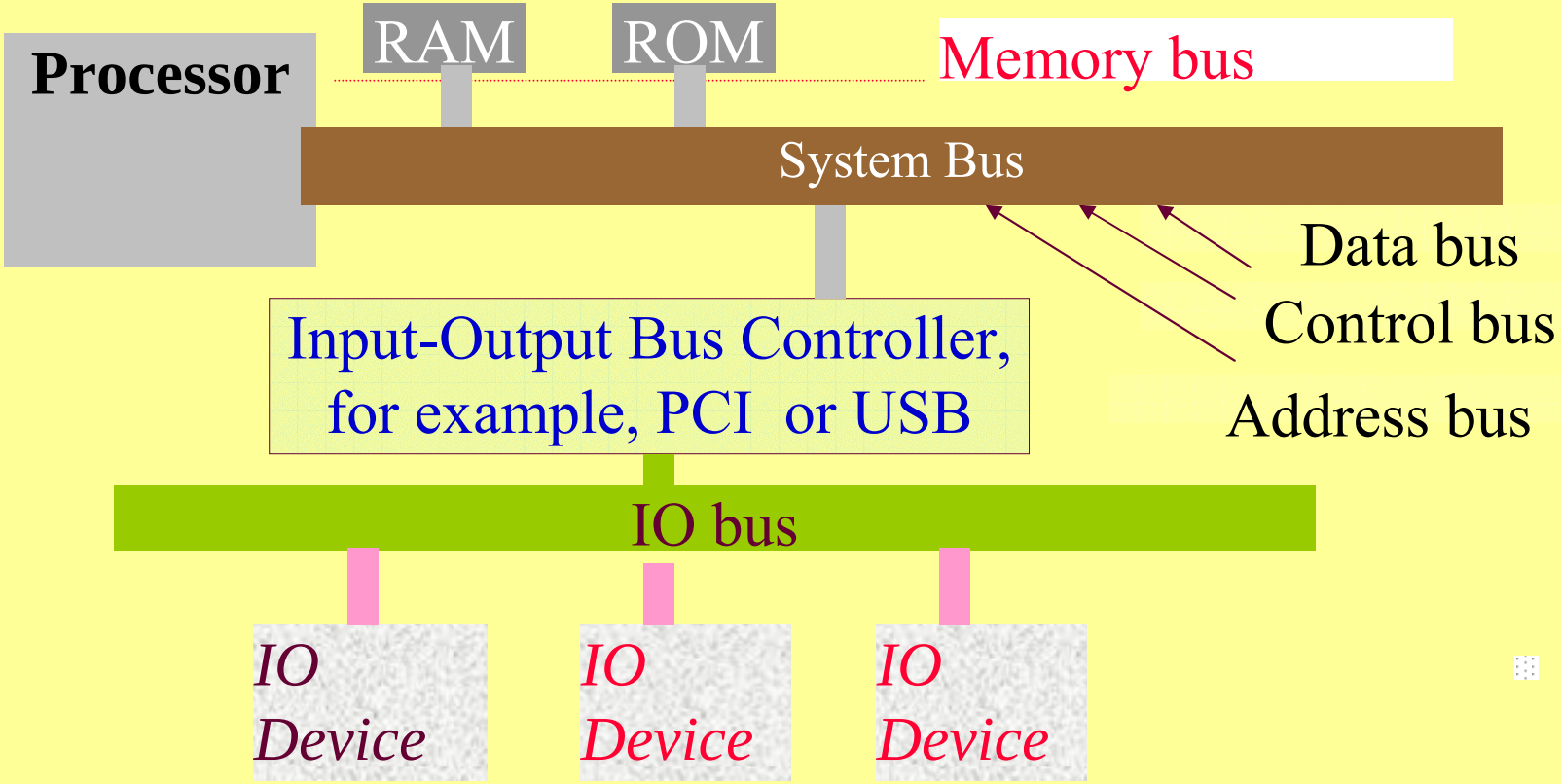
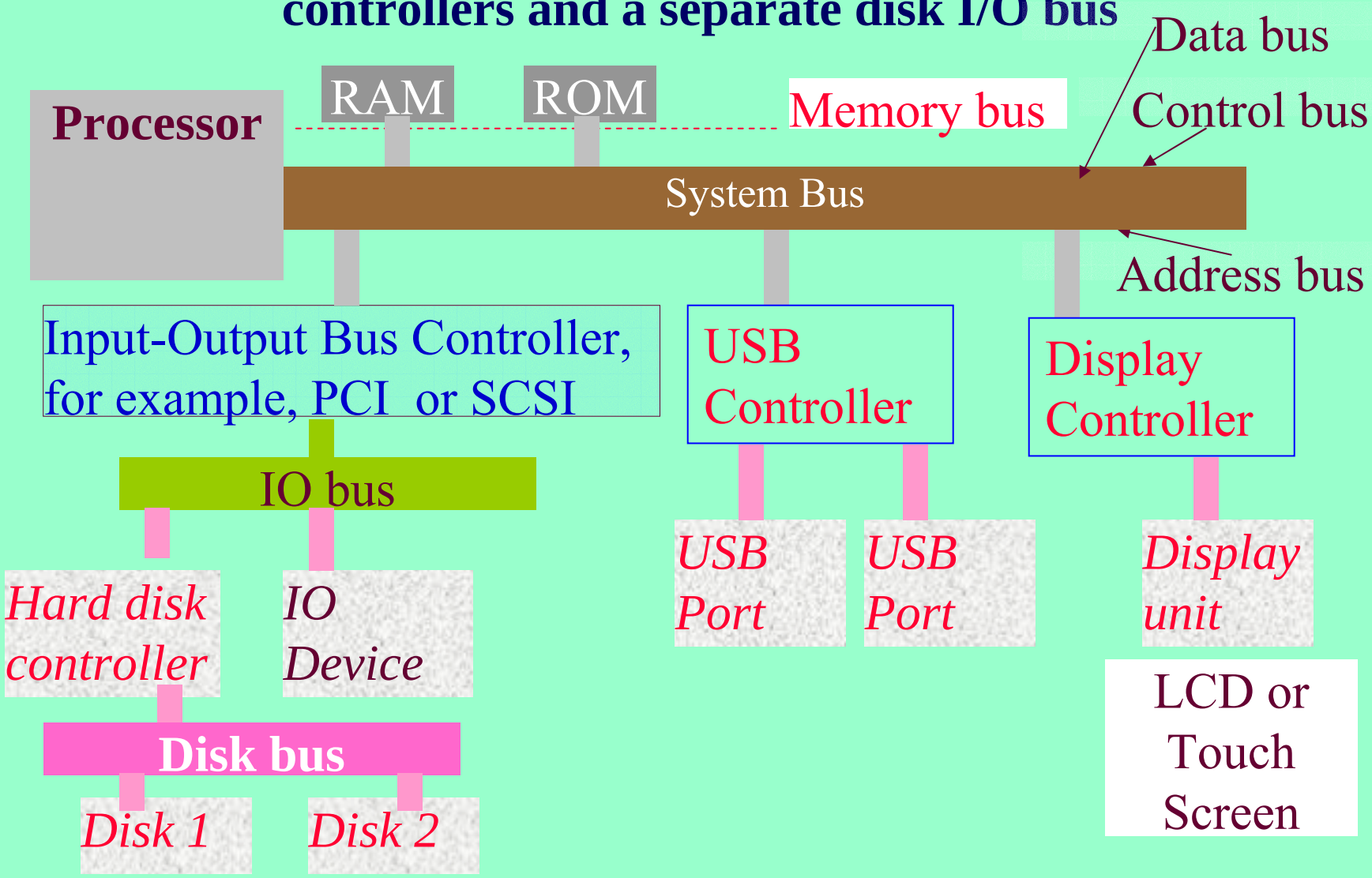
Memory system bus and I/O bus interconnections in a bus structure



3. Multilevel Buses

Separate memory and I/O buses using PCI and USB bus controllers and a separate disk I/O bus



Summary

We learnt

- Interfacing processor with memory, ports and devices using system bus
- System bus consisting of Address, data and control buses
- Latches, decoders and multiplexers
- Interfacing using system bus at first level and IO bus at second level
- Multilevel interfacing

End of Lesson 6 of Chapter 2