DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-5: SPI, SCI, SI and SDIO Port/devices for Serial Data Communication

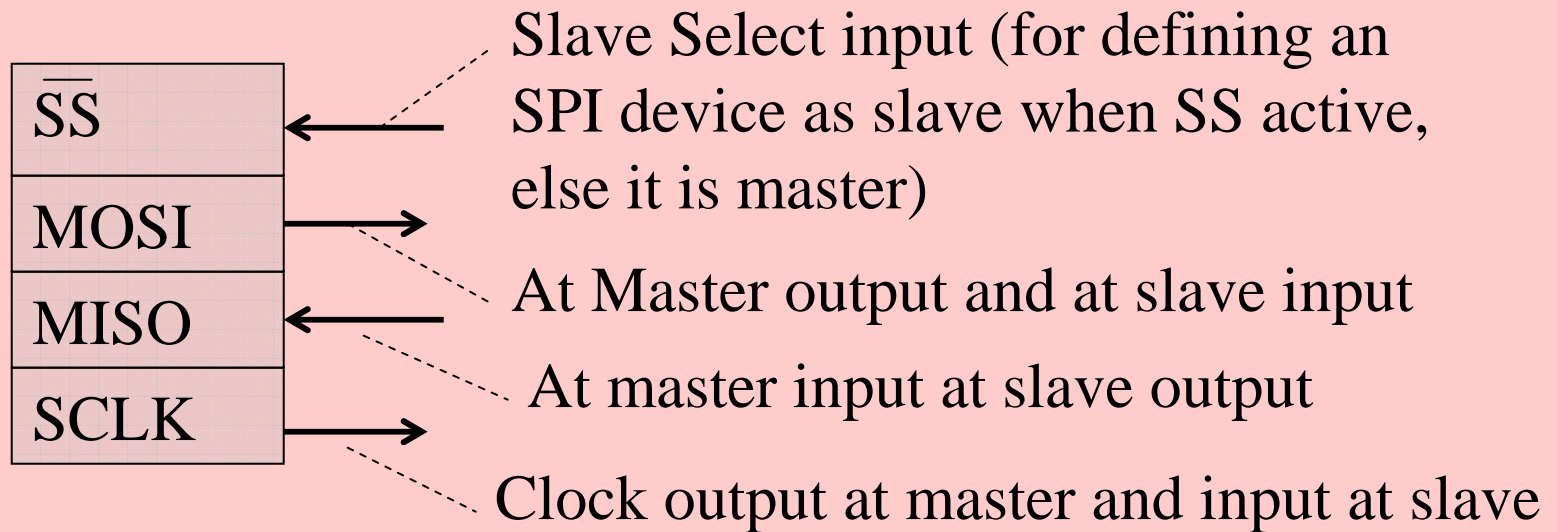# Microcontroller internal devices for SPI or SCI or SI

- Synchronous Peripheral Interface (SPI) Port, for example, in 68HC11 and 68HC12 microcontrollers

- Asynchronous UART Serial Connect Interface (SCI), for example, SCI port in 68HC11/12

- Asynchronous UART mode Serial Interface (SI), for example, SI in 8051

1. SPI

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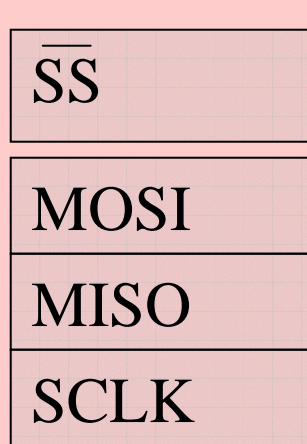Publs.: McGraw-Hill Education

SPI

- Full-duplex Synchronous communication.

- SCLK, MOSI and MISO signals for serial clock from master, output from master and input to master, respectively.

- Device selection as master or slave can be done by a signal to hardware input SS. (Slave select when 0) pin
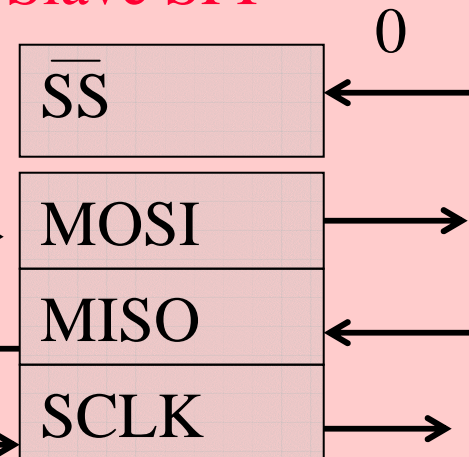
SPI signals

$\overline{SS}$

MOSI

MISO

SCLK

Slave Select input (for defining an SPI device as slave when SS active, else it is master)

At Master output and at slave input

At master input at slave output

Clock output at master and input at slave

Master SPI

$\overline{SS}$

MOSI

MISO

SCLK

1

Slave SPI

$\overline{SS}$

MOSI

MISO

SCLK

0

SPI Control Bits Programming

- Programmable for defining the instance of the occurrence of -ve negative edges and +ve positive edges within an interval of bits at serial data *out* or *in*
- Programmable for open-drain or totem pole output from a master to a slave.
- Programmable by the device selection as master or slave

SPI Control Bits Programming

- Programmable for the clock bits, and therefore of the period T of serial out data bits– down to the interval of 0.5μs for an 8 MHz crystal at 68HC11

68HC11/12 synchronous serial communication

- SPI (Serial Peripheral Interface)

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68HC11/12 SPI signals at Port PD

Programmable
data direction
register for
port D

DDR.2	PD.2	$\overline{SS}$
DDR.3	PD.3	MOSI
DDR.4	PD.4	MISO
DDR.5	PD.5	SCLK

DDRD   PD

68HC11/12 SPI Features

1. Programmable rates for the clock

2. Programmable as slave or master or by SS input bit

3. Programmable for the instance of the occurrence of <u>negative</u> or positive clock edge and <u>positive</u> edges

4. Programmable for open-drain output or totem pole output

2. SCI

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Serial Connect Interface (SCI) Port

- UART asynchronous mode port
- Full-duplex mode
- SCI programmable for transmission and for reception

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SCI Full duplex signals

Transceiver

RxD
TxD

At receiver input from a transmitter output

At transmitter output for a receiver input

Transceiver

RxD
TxD

Transceiver

TxD
RxD

UART

UART

SCI Control bits Programming

- Programmability for SCI baud rates are fixed as per rate and prescaling bits

- Serial *in* and *out* lines baud rate not separately programmable

- Baud rate is selectable among 32 possible ones by the three- rate bits and two prescaling bits.

- SCI two control register bits, T8 and R8 for the inter-processor communication in 11-bit format.

# SCI Control bits Programming

- SCI receiver *wake up* feature programmable by RWU (Receiver wakeup Unavailable bit)

- Feature enabled if RWU (1st bit of SCC2, Serial Communication Control Register 2) is set, and is disabled if RWU is reset.

- If RWU if set, then the receiver of a slave does not interrupt by the succeeding frames.

- Number of processors can communicate on the SCI bus using control bits RWU, R8 and T8

68HC11/12 asynchronous serial communication

- One SCI and standard baud rates can be set up to 9.6 kbps only in 68HC11

- 68HC12 provides two SCIs that can operate at two different clock rates.

- 68HC12 baud rates can be set up to 38.4 kbps.

68HC11 SCI signals at Port PD

UART

Programmable
data direction
register for
port D

DDR.1	PD.1	RxD
DDR.0	PD.0	TxD

DDRD   PD
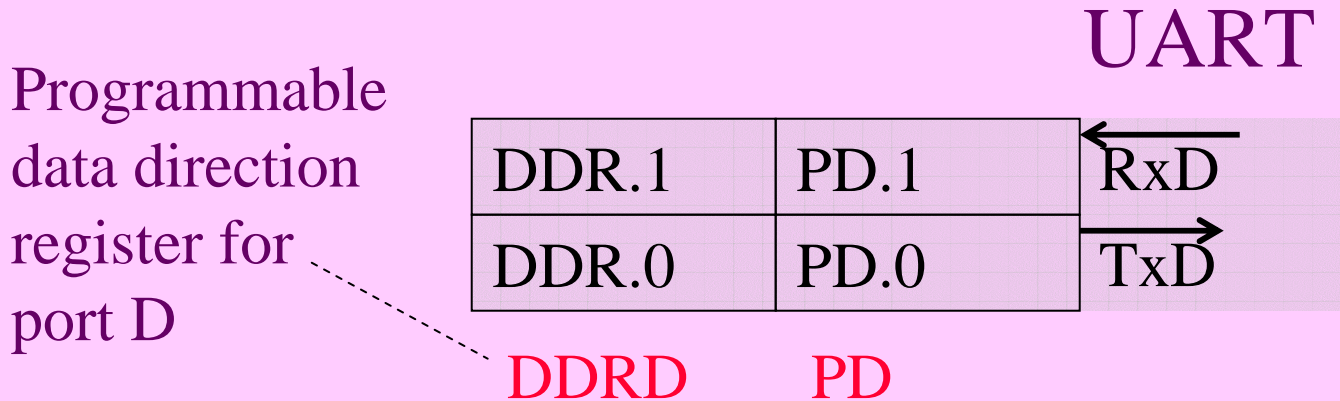
68HC11/12 SCI Features

1. SCI baud rates are fixed as per rate and prescaling bits

2. T8 and R8 for the inter-processor communication in 11-bit format

3. receiver *wake up* feature programmable by RWU

4. Signals programmable for RxD or TxD using DDR

3. SI

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Serial Interface (SI) Port

- UART 10T or 11T mode asynchronous port interface.

- Functions as USRT (universal synchronous receiver and transmitter) also.

- SI is therefore synchronous- asynchronous serial communication port called USART (universal synchronous-asynchronous receiver and transmitter) port.

- SI is an internal serial IO device in 8051.

SI Full duplex signals Mode 1, 2 or 3

SBUF Serial
transmit/receive data
buffer

TxD/CLK, RxD/Data pins

TxD

RxD
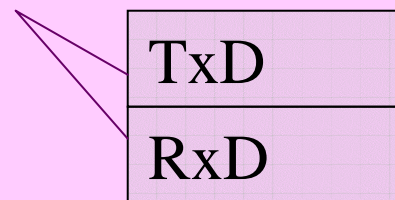
At receiver input from a transmitter output

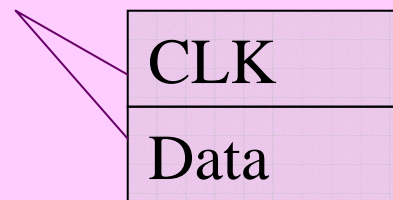At transmitter output for a receiver input

Processor
Processor

UART

Processor

TxD

RxD

TxD

RxD

UART

SI Half duplex signals Mode 0

SBUF Serial transmit/receive data buffer

TxD/CLK, RxD/Data Pins

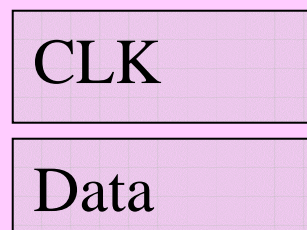| CLK |
|-----|
| Data |

From a transmitter Processor output at receiver input

At transmitter output for a receiver Processor input
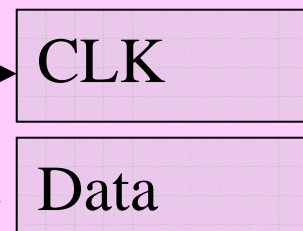
Processor

Processor

UART

CLK
Data

Processor

CLK
Data

UART

SI Control bits programming

- Mode 0– Half- duplex synchronous mode of operation, called. When a 12 MHz crystal is at 8051, and is attached to the processor, the clock bits are at the intervals of 1 μs.

- Mode 1 or 2 or 3– Full- duplex asynchronous serial communication.

- Modes 1 and 3 baud rate programmed– Using the timer bits.

SI Control bits programming

- Mode 2 baud rate programming using SMOD bit at an SFR called PCON, when is used, the rate is programmable at 1/64 or 1/32 of oscillator frequency at 8051.

- T8 and R8 programming, when using 11-bit format, provides the 10th bit for error-detection or for indicating whether the sent data byte is a command or data for the receiving SI device

8051 SI signals at Port P3.1 and P3.0

TxD/CLK, RxD/Data Pins

SBUF Serial transmit/receive data buffer

Programmed as per mode selected and SBUF read or write instruction executed

P3.1	TxD/CLK
P3.0	RxD/Data
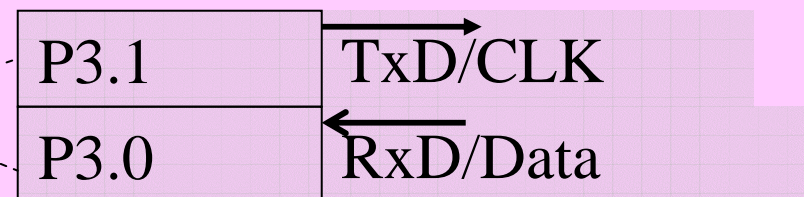
P3

8051 SI Features

1. Mode 0– Half-duplex synchronous mode of operation

2. T8 and R8 for the inter-processor communication in 11-bit format

3. Mode 1 or 2 or 3 – Full-duplex asynchronous serial communication

4. Signals not programmable for RxD or TxD no DDR in 8051

80196 On-chip common hardware device SI

- Programmable-rate register after loading the 14-bits at BAUD_RATE register twice.

3. SDIO

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Secure Digital Association (SD)

- SD– an association of over 700 companies started from 3 companies in 1999

- Created a new flash memory card format, called SD format for IOs

- SDIO card has become popular feature in handheld mobile devices, PDAs, digital cameras and embedded systems.

SDIO Card

- SD card size– just 0.14 cm $\times$ 2.4 cm $\times$ 3.2 cm.

- Allowed to stick out of the handheld device open slot, which can be at the top in order to facilitate insertion of the SD card

SDIO card host controller

- A processing element functions used SDIO host controller to process the IOs.

- Controller may include SPI controller to support SPI mode for the IOs and also supports the needed protocol functionality internally

SD card IO functionalities

- SDIO (Secure Digital Input Output) card
- Can have upto eight logical functions.
- provides additional memory storage in SD format
- Functions include IOs with several protocols, for example, IrDA adapter, Ethernet adapter, GPS or WiFi, Bluetooth, WLAN, digital camera, barcode or RFID code readers

SCI Control bits Programming

- For single byte transactions, SDIO card may include a UART 16550 mode communication over the SD

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SDIO 9 pins

- SDIO has 9 pins.

- Total 6 pins are for SPI and SD

SDIO Functions and Card

1. SDIO (Secure Digital Input Output) up to eight logical functions during communication

2. CRC checks on the transferred data and

3. Specifies capabilities for additional tries by retransmission on error

4. Data communication 48-bit command/ request format for 48-bit control register/ status register bits

5. Supports data transfer in block of bytes

SDIO Card

SDIO host controller

9-pin Connector

6. Programmable or SPI (20 Mbps) or 1-bit SD (25 Mbps) or 4-bit SD (100 Mbps by 4 serial bits in parallel) communication

Summary

We learnt

- SPI serial synchronous transmitting /receiving device, for example, in 68HC11/12

- SCI serial asynchronous UART mode transmitting /receiving device, for example, in 68HC11/12 with inter-processor on SCI bus

We learnt

- SI serial synchronous half duplex/asynchronous full duplex device , for example, in 8051

We learnt

- SDIO IO card with (i) host controller for 8 logic functions, 48-bit control/command register, flash memory and 9 pins

- (ii) SD 1-bit serial transfer, 4-bit mode serial-cum-parallel and optional UART modes for the IOs

- (iii) Support to transmission of data with many protocols

End of Lesson 5 of Chapter 3