REAL TIME OPERATING SYSTEMS

Lesson-15:
Power Optimization

1. Memory Optimization

Power Optimization

- Saving power and energy requirement for a given set of codes, while finishing instructions in the scheduled time-slot

2. Power Saving Methods

Switch to standby and Stop Modes

- Wait and Stop instructions and operation in power-down mode.
- One way to do this is to cleverly incorporate into the software the Wait and Stop instructions.
- For example, a program can be such that it reduces the brightness level of the LCD panel so that it takes less power when the system is used in fully lighted room. [A sensor senses the light level at specific intervals]

Stop instructions

- Mobile phone auto-switch off the LCD lights when not using for 5 or 10 or 20 s.
- A call attend mode can be switched off if there is not talk for over a minute

Current Requirements

- (*i*) 75 mA when the processor plus the external memories and chips are in running state
- (*ii*) 50 mA– when only the processor running

Current Requirements

- (*iii*) 15μA– when only the processor is in stop state, clock has been disabled from all structural units within the processor.
- (*iv*) 15 μA– when the processor plus the external memories and chips are in stop state, the clock disabled from all system units.

Current Requirements

- (*v*) 10 μA— when the processor in waiting state, the external memories and the chips are in waiting state; but the clock has not been disabled
- (*vi*) 5 μA— when only the processor is in waiting state, the clock has not been disabled from the structural units of the processor, such as timers

Disable Caches and other Units Mode

- Disable use of certain structural units of the processor—for example, caches—when not necessary and to keep in disconnected state those structure units that are not needed during a particular software-portion execution, for example timers or IO units

Reduce Circuit Glitches

- In a CMOS circuit, power dissipates only at the instance of change in input.
- Therefore, unnecessary glitches and frequent input changes increase power dissipation.
- VLSI circuit designs optimized to eliminate all removable glitches, thereby eliminating any frequent input changes

Low Voltage operation Mode

- to operate the system at the lowest voltage levels in the idle state by selecting power-down mode in that state
- LVCMOS circuits

Power saving mode by clock rate reduction

- Power dissipation reduces typically by 2.5 mW per 100 kHz reduced clock rate.
- So reduction from 8000 kHz to 100 kHz reduces power dissipation by about 200 mW, which is nearly similar to when the clock is non-functional

Summary

We learnt

- Clever real-time programming by using 'Wait' and 'Stop' instructions and disabling certain units when not needed is one method of saving power during program execution.
- Low voltage LVCMOS circuits
- Reduced clock rate when needed in order to control power dissipation.
- Good design must optimize the conflicting needs of low power dissipation and fast and effective program execution

End of Lesson 15 of Chapter 8