DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-6: Parallel port at devices

Parallel Port

- 8-bit IOs
- Short distances, generally within a circuit board or IC or nearby external devices

Parallel port in the devices

- Advantage– Number of 8 bits over the wires in parallel.
- High data transfer rate
- Disadvantage– More number of wires
- Capacitive effect in parallel wires reduces the length up to which communication in parallel can take place.
- High capacitance results in delay for the bits at the other end undergoing transition from 0 to 1 or 1 to 0.

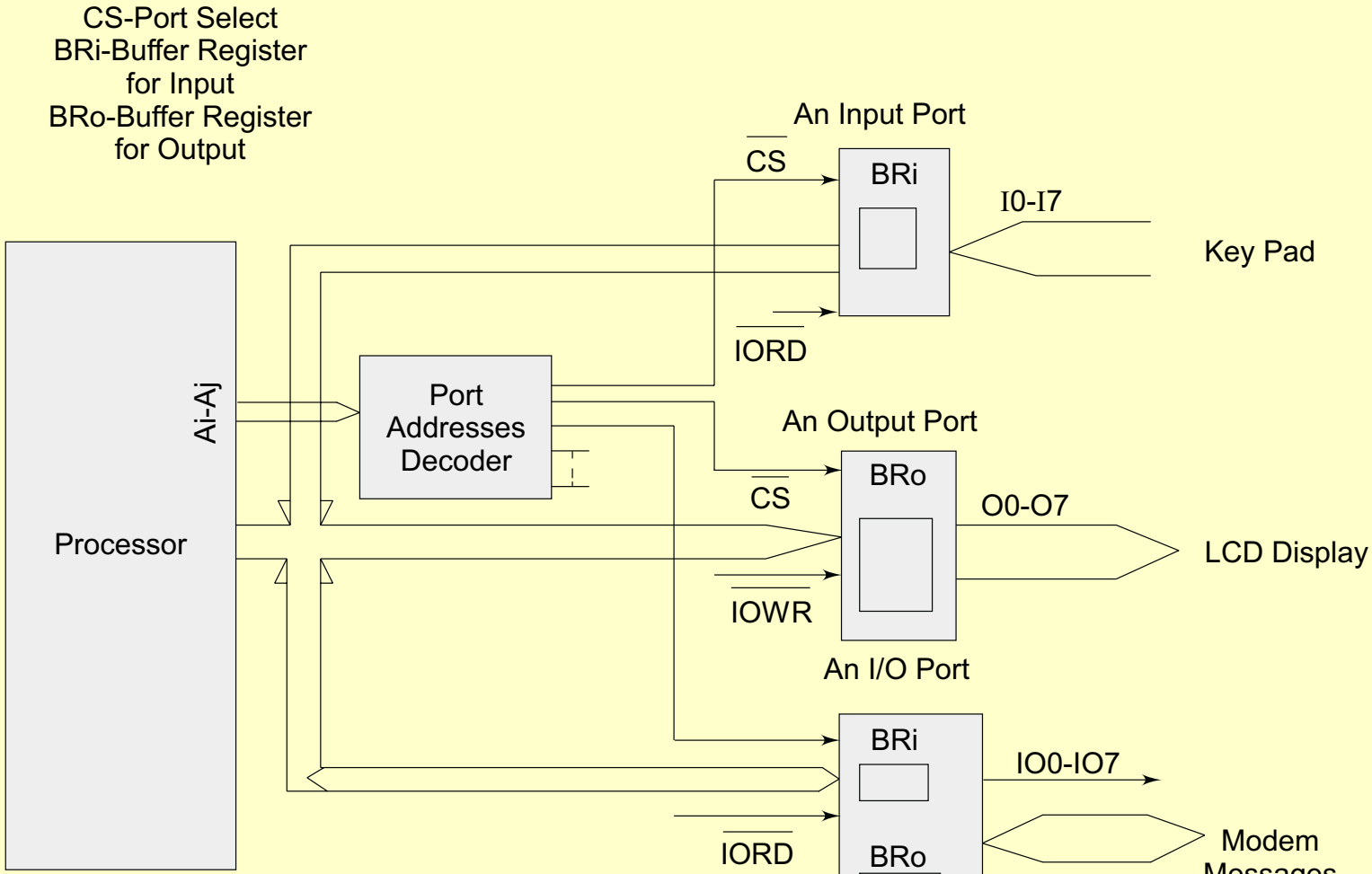
Parallel port in the devices

- Disadvantage– High capacitance can also result in noise and cross talk (induced signals) between the wires.

Port Interfacing

- IO device interfacing-circuit with the processor and system buses and connections to external peripherals/systems
- Parallel port inputs I0 to I7 may be from a keypad controller.
- Parallel port outputs O0 to O7 may be output bits to LCD display output controller.
- Br_i and Br_o buffers may be provided at bi-directional I/O port

Parallel port interfacings for keypad, LCD display and modem



(a)

Handshaking signals to and from an external peripheral device for input at port

- Device makes a strobe request to port, *STROBE* after it is ready to send the byte and
- System I/O port sends the acknowledgement, *PORT READY*.
- System I/O port receives data in buffer and then issues an interrupt signal, INT to processor to enable an ISR execution

Handshaking signals to and from an external device for output at port

- Device sends the message *ACKNOWLEDGE* when and the I/O device port ends the *BUFFER FULL* signal to inform that the is buffer full.
- The processor is sent the *INTERRUPT REQUEST* message, when the transmitting-buffer is empty (available for next write)

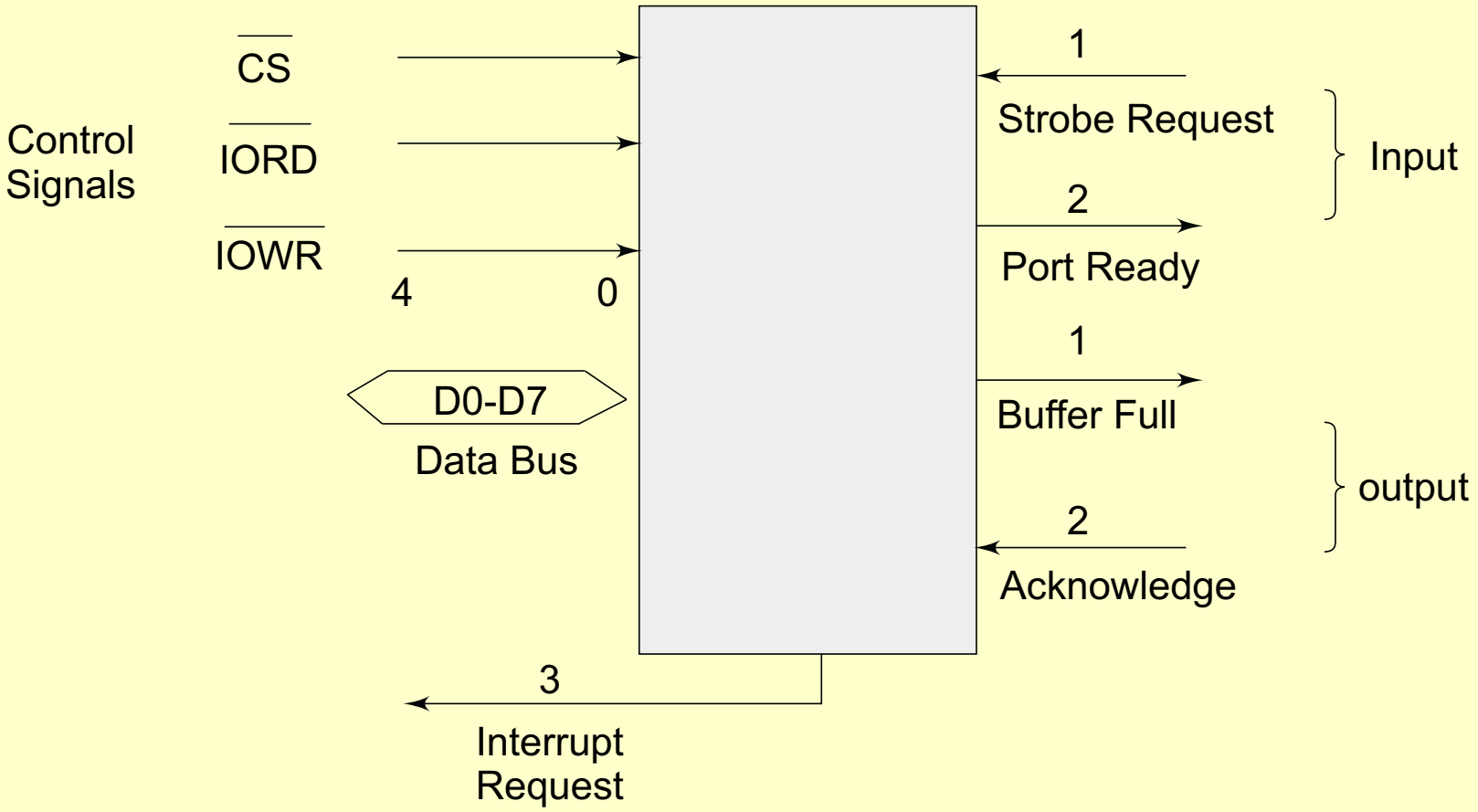
Port Interrupt to processor

- When receiving-buffer is full (available for next read)
- When transmitting-buffer is empty (available for next write)

Bidirectional Port Handshaking signals

- STROBE
- PORT READY
- BUFFER-FULL
- ACKNOWLEDGE
- INTERRUPT REQUEST

Parallel IO port handshaking and Interfacing



(b)

Parallel port at IBM PC using 25 pins connector

- 8 I/O pins
- 8 ground pins– (pins at 0 V)
- Status pins and control pins –for handshaking
- 5 input pins for status signals (four active high S3 to S6, one active low S7) from external device (for example, printing device)
- 4 output pins for control signals (one active high C2 and three active low $\overline{C0}$, $\overline{C1}$ and $\overline{C3}$

Intel 8255 programmable peripheral interface (PPI)

- Four addresses for the PPI port, three for the ports and one for the control word.
- Three 8-bit ports– port A, B and C.
- Port C programmable to function in bit set-reset mode.
- Each bit of port C can be set to 1 or reset to 0 by an appropriate control word.
- Alternatively, the ports can be grouped as Group A (Port A and Port C upper four bits) or Group B (Port B and Port C lower four bits).

Mode 0 Groups A and B Programming

- In mode 0 programming for a group such that the group does not use handshaking signals.
- Group A mode 0, Port A input or output and PC.7-PC.4 input or output
- Group B mode 0, Port B input or output and PC.0-PC.3 input or output

Mode 2 Group A Programming

- Mode 2 programming is for port A as bidirectional as input as well as output.
- Handshaking signals at Port C– STROBE, PORT READY, BUFFER FULL, ACK and INTERRUPT when port A functions as bi-directional I/O port.

Mode 1 programming for Groups A and B

- Port as either input or as output with handshake
- Group A or B, port A or B use at an instance only one of the two handshaking signal pairs, either (STROBE, PORT READY) or (BUFFER FULL, ACK) plus one INTERRUPT signal at Port C pins.

Port Multiple features

- A port may have provision for multiplexed output to connect to multiple systems or units.
- Port may have provision for de-multiplexed inputs from the multiple systems or units
- Special functionalities
- Alternative use– External address, data and control buses

External Address and data buses

- 8051-family two ports– abbreviate as P0 and P2.
- Alternate function (AD0-AD7 and A8-A15) to bring out when needed, the internal multiplexed buses
- For the external program and memories whenever the internal memory is insufficient.

External Address and data buses

- 68HC11 ports B and C alternative uses of for the port pins – bring out the internal address and data buses, respectively

Special functionalities

- A device or port may have multi-byte data input buffer(s) and data output buffer(s).
- Eight-byte buffer in 80196 microcontroller port can generate three interrupts, one on receiving a byte, one on receiving the fourth byte and one on when the buffer full.
- Deadline increases for servicing these interrupts up to eight times compared to the case when then there is a single byte register instead of 8-bit buffer with buffer-full interrupt

Special functionalities

- A port may be with a DDR (Data Direction Register) (for example, in 68HC11 microcontroller).
- Advantage 1 – Each bit of the port is now programmable. It can be set as input or output.
- Advantage 2 – Same Port pin can be used by changing direction of bits transfer when sending signals as master or receive signals as slave

Port driving and loading capabilities

- Port LSTTL driving capability
- Port loading capability are important characteristics.

Parallel Port special functionalities

- *Quasi bi-directional* port (for example, in 80196)– port limited driving capability for a period of one or a few clock cycles and for one or a few LSTTL gates only.
- When the port connects to more than one LSTTL then an appropriate pull-up circuit will be required for each port pin.

Parallel Port special functionalities

- Port may be an O.D. (open drain) port– zero driving capability unless the drain connects +ve supply voltage. If the given port has the O.D. gates, appropriate pull-up resistance or transistor is connected to each port pin to provide the driving capability. The drain or collector connects to the supply voltage to provide the pull-up.

Multiple or alternate functionality for analog inputs in the port pins

- 80196 input port pins. Each pin of P2 has alternative use as a multi-channel analog input facility for 8 analog inputs.

Multiple or alternate functionality for PWM output

- A port pin can alternatively be PWM output to enable DAC operation
- PWM connects to integrator and integrator provides analog output

Multiple or alternate functionality for Time capture inputs

- A port pin can alternatively be a time-capture input to enable the internal timing device to load the time (counts) at the captured instance

Multiple or alternate functionality for Time compare outputs

- A port pin can alternatively be a time-compare output to enable the internal timing device to compared preload time (counts) with the present counts to enable sending output at the instance of their equality
- For alarm like action from timing device

Multiple or alternate functionality in the port pins

- 8051 each pin of P3 in, has the alternative multiple uses– during the serial communication, timer/counter signals, interrupt-signals, and $\overline{RD}$ and $\overline{WR}$ control signals for external memories.

Summary

We learnt

- Parallel port in IBM PC
- Programmable Peripheral Interface –PPI 8255
- Multiple functionalities at port pins
- Data direction register– DDR
- Multiplexed/de-multiplexed outputs and inputs at the ports
- Handshaking signals.
- Several alternate uses of port pins

End of Lesson 6 of Chapter 3