DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-15: Watchdog Timer

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Watchdog timer

- A timing device such that it is set for a preset time interval and an event must occur during that interval else the device will generate the timeout signal on failure to get that event in the watched time interval.

- On that event, the watchdog timer is disabled to disable generation of timeout or reset

- Timeout may result in processor start a service routine or start from beginning

Example

- Assume that we anticipate that a set of tasks must finish in 100 ms interval.
- The watchdog timer is disabled and stopped by the program instruction in case the tasks finish within 100 ms interval.
- In case task does not finish (not disabled by the program instruction), watchdog timer generates interrupts after 100 ms and executes a routine, which is programmed to run because there is failure of finishing the task in anticipated interval.

Watchdog timer application

- An application in mobile phone is that display is off in case no GUI interaction takes place within a watched time interval.
- The interval is usually set at 15 s, 20 s, 25 s, 30 s in mobile phone.
- This saves power.

Watchdog timer application

- An application in temperature controller is that if controller takes no action to switch off the current within preset watched time interval, the current is switched off and warning signal is raised as indication of controller failure. Failure to switch off current may burst a boiler in which water is heated.

Provisioning of watchdog timer

- A software task can also be programmed as a watchdog timer

- Microcontroller may also provide for a watchdog timer.

68HC11 microcontroller watchdog timer

- There are two registers, CONFIG (system configuration control register) and COPRST (computer operating properly and processor reset on failure).

- They are for programming the interrupts of the watchdog timer.

68HC11 microcontroller watchdog timer

- CONFIG has a bit, NOCOP. It configures when processor writes the configuration word at the address 0x003F. NOCOP is the 2nd bit of CONFIG

- If NOCOP is reset to 0 the COP facility is enabled.

- [COP means computer (68HC11 watchdog timer operating properly]. COP facility provides for keeping a watch on the user program execution time

Computer-reset control register COPRST

- When the user program takes a longer time in routine than planned or expected by the user software the user provides for storing at desired intervals; firstly, the 0x55 and then the 0xAA at the COPRST.

Watchdog timer overflows (time outs)

- 68HC11 program counter is reset according to the 16 bits (lower and higher bytes) preloaded at the addresses 0xFFFA and 0xFFFB, respectively. If these 16 bits are the same as the bits in 0xFFFE and 0xFFFF, then the microcontroller executes instructions as when it resets on power up or else executes the routine at the 16-bit address fetched from 0xFFFE and 0xFFFF on failure within the watched time interval.

Option register, OPTION

- The 0th and 1st bit of OPTION at the address 0x0039 are the CR1 and CR0 bits.

- IF NOCOP resets ('0') and CR1-CR0 =0-0, watchdog timer time out occurs after every 2^{16} E-clock pulses.

- As T = 0.5μs for the processor E clock output at 2 MHz, the WDT time-out will occur every 16.384 ms ($2^16 \times 0.5$μs) unless the user software stores at desired intervals before a time out, first the 0x55 and then the 0xAA at the computer reset control register COPRST. [After 2^{15} pulses if CR1-CR0 = 0-1, 2^{14} pulses for 1-0, 2^{13} pulses for 1-1].

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Summary

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We learnt

- A watchdog timer number of applications

- It is timing device such that it is set for a preset time interval and an event must occur during that interval and program instuction must disable the watchdog timer else the device will generate on the timeout signal an interrupt for the failure to get that event in the watched time interval

End of Lesson 15 of Chapter 3