DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-22: PARALLEL BUS DEVICE PROTOCOLS – PCI Bus

PCI Parallel Bus

- Parallel bus enables a host computer or system to communicate simultaneously 32-bit or 64-bit with other devices or systems, for example, to a network interface card (NIC) or graphic card

Computer system PCI

- When the I/O devices in the distributed embedded subsystems are networked all can communicate through a common parallel bus.
- PCI connects at high speed to other subsystems having a range of I/O devices at very short distances (<25 cm) using a parallel bus without having to implement a specific interface for each I/O device.

PCI bus Applications

connects

- display monitor,
- printer,
- character devices,
- network subsystems,
- video card,
- modem card,
- hard disk controller,

PCI bus

connects

- thin client,
- digital video capture card,
- streaming displays,
- 10/100 Base T card,
- Card with 16 MB Flash ROM with a router gateway for a LAN and
- Card using DEC 21040 PCI Ethernet LAN controller.

Computer system PCI

- When the I/O devices in the distributed embedded subsystems are networked, all can communicate through a common parallel bus.
- PCI connects at high speed to other subsystems having a range of I/O devices at very short distances (<25 cm) using a parallel bus without having to implement a specific interface for each I/O device.

PCI Bus Feature

- 32- bit data bus extendible to 64 bits.
- PCI protocol specifies the ways of interaction between the different components of a computer.
- A specification version 2.1— synchronous/asynchronous throughput is up to 132/ 528 MB/s [33M × 4/ 66M × 8 Byte/s], operates on 3.3V to 5V signals.

PCI bus feature

- PCI driver can access the hardware automatically as well as by the programmer assigned addresses.
- Automatically detects the interfacing systems and assigns new addresses
- Thus, simplified addition and deletion (attachment and detachment) of the system peripherals.

FIFO in PCI device/card

- Each device may use a FIFO controller with a FIFO buffer for maximum throughput.

Identification Numbers

- A device identifies its address space by three identification numbers, (i) I/O port (ii) Memory locations and (iii) Configuration registers of total 256B with a four 4-byte unique ID. Each PCI device has address space allocation of 256 bytes to access it by the host computer

PCI device identification

- A sixteen16-bit register in a PCI device identifies this number to let that device auto- detect it.
- Another sixteen16-bit register identifies a device ID number. These two numbers let allow the device to carry out its auto-detection by its host computer.

Peripheral Component Interconnect (PCI) Bus

- Independent from the IBM architecture.
- Number of embedded devices in a computer system use PCI
- Three standards for the devices interfacing with the PC

Peripheral Component Interconnect (PCI) Standards

- PCI 32bit/33 MHz, and 64bit/66 MHz
- PCI Extended (PCI/X) 64 bit/100 MHz ,
- Compact PCI (cPCI) Bus

Two super speed versions

- PCI Super V2.3 264/528 MBps 3.3V (on 64- bit bus), and 132/264 (on 32-bit bus) and
- PCI-X Super V1.01a for 800MBps 64- bit bus 3.3Volt.

PCI bridge

- PCI bus interface switches a processor communication with the memory bus to PCI bus.
- In most systems, the processor has a single data bus that connects to a switch module PCI bridge
- Some processors integrate the switch module onto the same integrated circuit as the processor to reduce the number of chips required to build a system and thus the system cost.

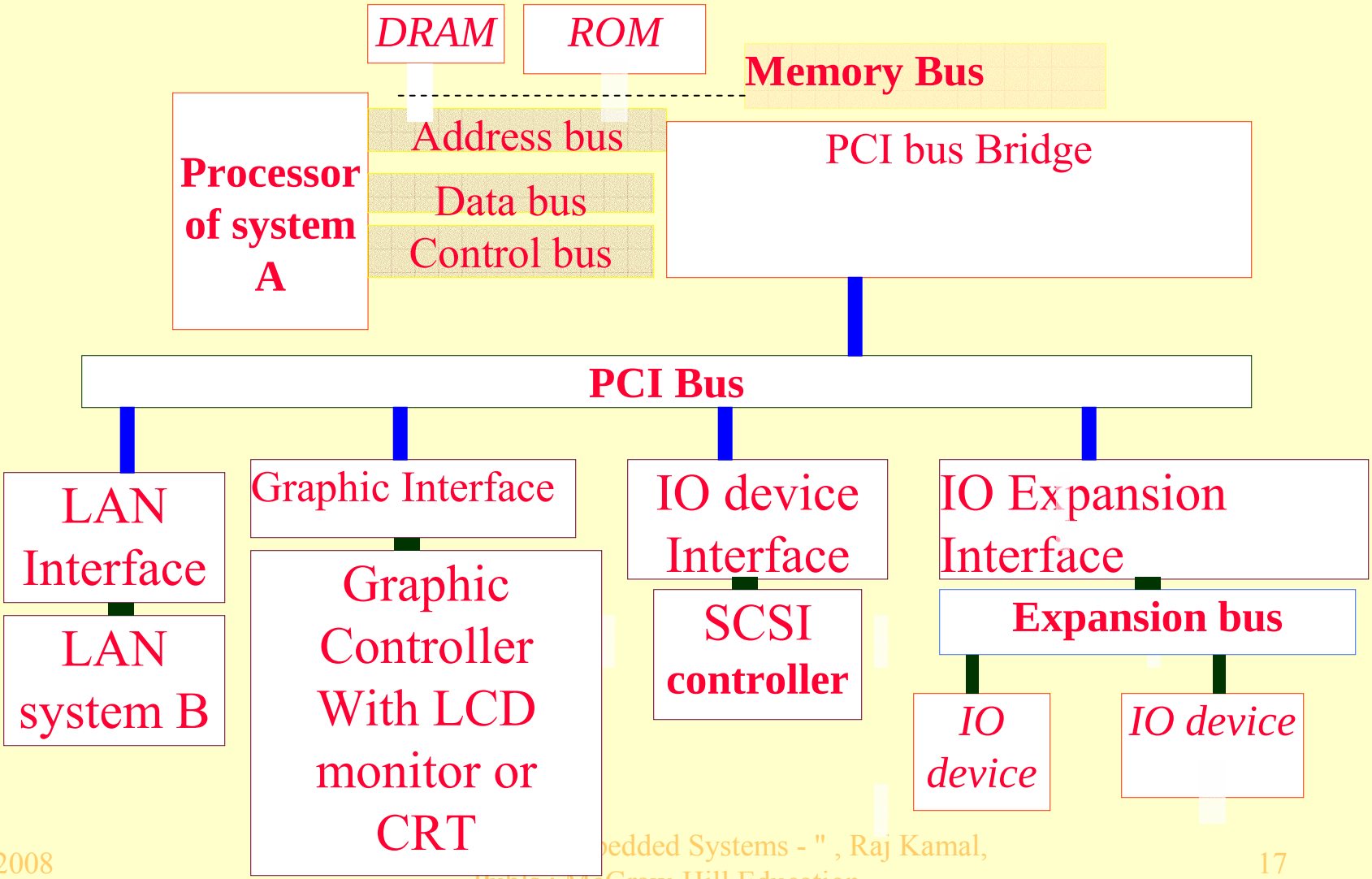
PCI bridge/switch

- Communicates with the memory through a *memory bus* (a set of address, control and data buses), a dedicated set of wires that transfer data between these two systems.
- A separate *I/O bus* connects the PCI switch to the I/O devices.

Advantage of Separate memory and I/O buses

- I/O system generally designed for maximum flexibility, to allow as many different I/O devices as possible to interface to the computer
- Memory bus is designed to provide the maximum-possible bandwidth between the processor and the memory system.

PCI Bridge and Buses



PCI

- 32-bit 33 MHz throughput = 133 MBps,
- full component level, Connector (94-pin connector with 50 signals)
- 64-bit bus, 66 MHz option

PCI 2.2
Board specifications

- Board specifications, multiplexed AD0-AD31 bus, dual address 64-bit support,
- An un-terminated bus,
- Signal relay reflected on signal to attain the final value

PCI-X (PCI extended)

- 133 MBps to as much as 1 GBps
- Backward compatible with existing PCI cards
- Used in high bandwidth devices (Fiber Channel, and processors that are part of a cluster and Gigabit Ethernet)

PCI-X (PCI extended) option

- Maximum 264 MBps throughput, uses 8, 16, 32, or 64 bit transfers
- 6U cards contain additional pins for user defined I/Os
- Live insertion support (Hot-Swap),
- Supports two independent buses on the back plane (on different connectors)

PCI-X (PCI extended) option

- Supports Ethernet, Infiniband, and Star Fabric support (Switched fabric based systems) Compact PCI (cPCI)

Each PCI device on Bus

- Perform a specific function,
- May contain a processor and software to perform a specific function.
- Each device has the specific memory address-range, specific interrupt-vectors (pre-assigned or auto configured) and the device I/O port addresses.
- A bus of appropriate specifications and protocol interfaces these to the host computer system or compute

Configuration address space

- Unique feature of PCI bus unique feature is its configuration address space.

PCI controller Features

- Accesses one device at a time
- All the devices within host device or system can share the I/O port and memory addresses, but cannot share the configuration registers
- Device cannot modify other configuration registers but can access other device resources or share the work or assist the other device

PCI driver Features

- If there are reasons for doing it so, a PCI driver can change the default boot up assignments on configuration transactions.

PCI Device Initialization

- A device can initialize at booting time
- Avoids any address collision
- Device on boot up disables its interrupt and closes its door to its address space except to the configuration registers space

PCI BIOS (Basic Input-Output System)

- Performs the configuration transactions and then, memory and address spaces automatically map to the address space in the device hosting system

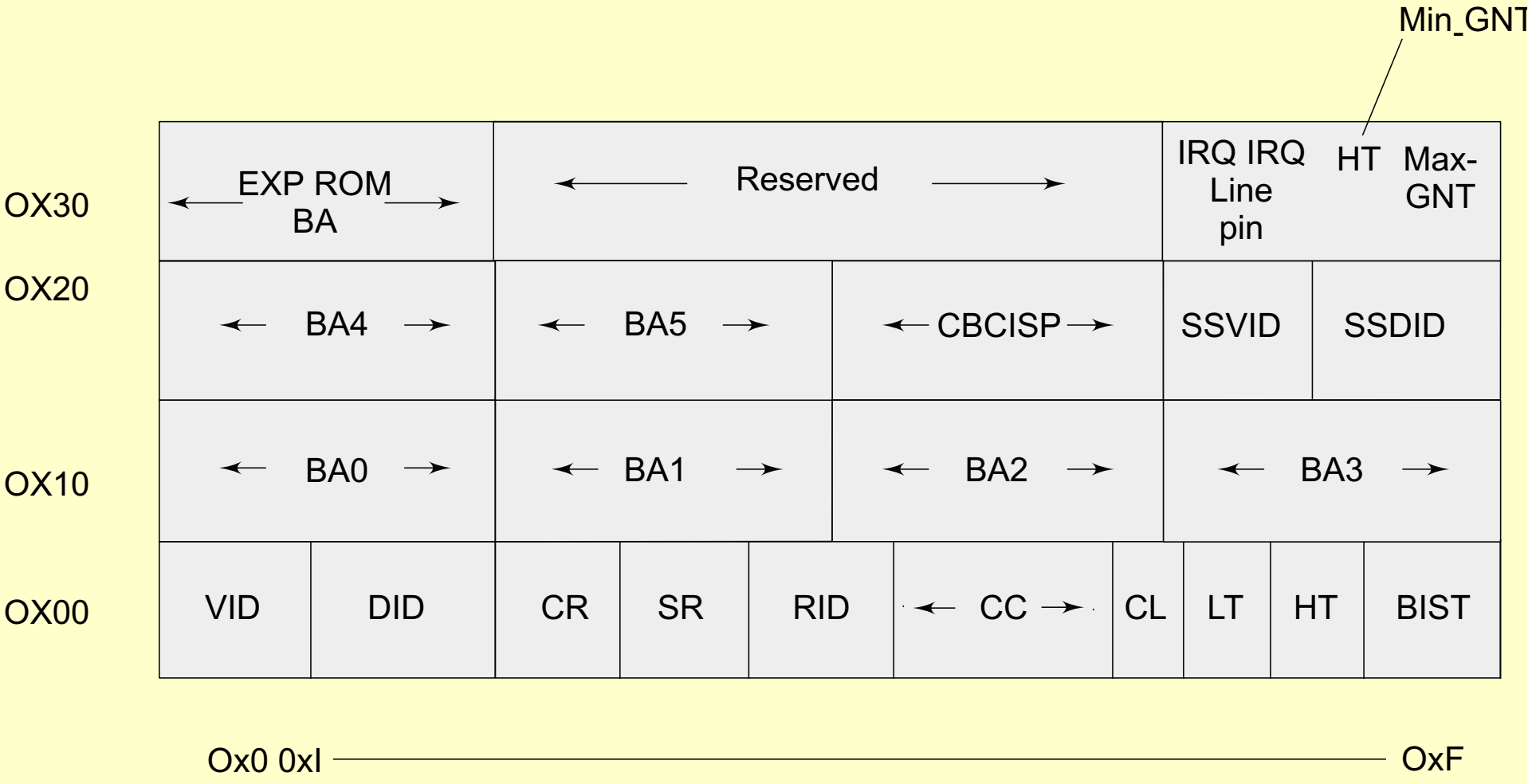
PCI device Interrupt Handling

- A uniquely assigned interrupt type (a number) handles an interrupt.
- For example, interrupt type 3 has the interrupt vector address 0x0000C and four bytes at the address specify the interrupt service routine address.
- Interrupt type can be a number between 0x00 and 0xFF.

Configuration register number 60

- Stores the one byte for the interrupt type *n* (pci)
- The PCI device when interrupted handles the interrupt of type *n*(pci)

64 bytes at the standard device independent configuration registers in a PCI device



Meaning of Terms in Figure

- *VID*: Vendor ID.
- *DID*: Device ID.
- *RID*: Revision ID.
- *CR*: Common Register.
- *CC*: Class Code.
- *SR*: Status Register.

Meaning of Terms in Figure

- *CL*: Cache Line.
- *LT*: Latency Timer.
- *BIST*: Base Input Tick.
- *HT*: Header Type.
- *BA*: Base Address.
- *CBCISB*: Card Base CIS Pointer.

Meaning of Terms in Figure

- *SS*: Sub System.
- *ExpROM*: Expansion ROM.
- *MIN_GNT*: Minimum Guaranteed time
- *MAX_GNT*: Maximum Guaranteed Time.

Summary

We learnt

- PCI a parallel bus
- PCI 32/33 MHz, and 64/66 MHz
- PCI/X buses 64/100 MHz transfers
- Independent from the IBM architecture.
- New versions have been introduced for the PCI bus architecture

End of Lesson 22 of Chapter 3