DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-11: Sophisticated Interfacing Features in Device Ports

Sophisticated Interfacing Features

- A device port may not be as simple as the one for a stepper motor port or for serial line UART
- May be a sophisticated I/O device or port
- Examples— I/O devices for fast I/Os, fast serializations and de-serializations, fast transceiver and real time video processing system I/Os.

Sophisticated Interfacing Features

Low voltage gates
Schmitt trigger gates
Power managing gates
Dynamically controlled impedance matching
SerDes subunit
PCS subunit
PCM subunit

In-built Schmitt trigger at Port

- Conditioning of the signal by noise-elimination
- Example, 5V Schmitt trigger circuit property— On a transition from 0 to 1 occurs, if the voltage level exceeds 2/3 of 5V level, then only then there is transition to 1.
- When a transition from 1 to 0 occurs, if the voltage level lowers below 1/3 of 5V level, then only then there is there a transition to 0

Xilinx new technology

- DataGate at the ports
- DataGate ─ a programmable ON/OFF switch for power management
- Makes it possible to reduce power consumption by reducing unnecessary toggling of inputs when the device port is operated at fast speeds and not in use

Gates at Ports

- LVTTL (Low Voltage TTL) and LVCMOS (Low Voltage CMOS) gates may be used at the device ports for 1.5 V I/O
- HSTL (High Speed Trans-receiver Logic) and SSTL (Stub-series Terminated Logic) standards.
- HSTL for high-speed operations.
- SSTL when the buses are to be isolated from relatively large stubs

I/O device Special support circuits

- Multiple gigabit (transceiver(s) (MGTs)
- 622 Mbps to 3.125 Gbps(MGTs.
- Device for I/O may integrate a SerDes (serialization and De-serialization) subunit
- SerDes is a standard subunit at in a device where the bytes placed at 'transmit holding buffer' serialize on transmission and once the bits are received these de-serialize

I/O device integration to a digital Physical Coding Sub-layer (PCS).

- Analog audio and video signals ─ pulse code modulated (PCM) at the sub-layer.
- PCS sub-layer directly provides the codes from the analog inputs within the device itself
- The codes then saved in the device data buffers
- Advantage of an in-built PCS ─ No need of external PCM coding, in background operations, fast coding
- High System's performance for multimedia inputs at the devices.

I/O integration to an analog Physical Media Attachment (PMA)

- Unit for connecting direct inputs and outputs of voice, music, video and images.
- In-built PMA— the device directly connects to the physical media.
- PMA is needed for real- time processing of video and audio inputs at the device

Summary

We learnt

- Schmitt trigger inputs
- Low voltage gates
- Power managing gates
- Dynamically controlled impedance matching to eliminate line reflections
- SerDes subunit serializes and de-serializes in outputs and inputs in the devices.
- PCS and PMA subunits for analog inputs for video and audio I/O device.

End of Lesson 11 of Chapter 3