8051 AND ADVANCED PROCESSOR ARCHITECTURES –
Lesson-1: 8051 Architecture and Instruction Set

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1. 8051 microcontroller architecture

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2

Reset

TO | T1 | SI | WDT | Osc

Port P1

IR | Execution unit

IO and internal devices SFRs

ID

A, B,PSW, SP SFRs

DPTR (2 SFRs)

Condition test branch logic

Register Banks of 8 registers and internal RAM

Internal ROM

Control and Sequencing Circuit

Port P3

PC

Port P2

Interrupt Control

Port P0

A8-A15 | AD0-AD8

8051 basic architecture of processing unit, special function registers, memory (in Harvard architecture), and port, counters/timer, watch dog timer, serial IO and interrupt handler devices

8051 microcontroller features

- 12 MHz clock. Processor instruction cycle time 1 μs. [in Classic version]

- An 8-bit ALU.

- Harvard memory architecture – the external program memory and data memory have separate address spaces from 0x0000 and separate control signal(s).

- 8-bit internal data bus width and 16-bit internal address bus – Harvard memory architecture

- CISC (Complex Instruction Set Computer)

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8051 microcontroller features (contd.)

- Special function registers (SFRs) –PSW (processor status word), A (accumulator), B register, SP (stack pointer) and registers for serial IOs, timers, ports and interrupt handler.

8051 microcontroller features (contd.)

- Special bit manipulation instructions.

- 16-bit Program counter with initial default reset value defined by processor is 0x0000.

- 8-bit stack pointer with initial default value defined by processor is 0x07

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8051 microcontroller features (contd.)

Classic 8051 simple architecture

- no floating-point processor,

- no cache,

- no memory management-unit,

- no atomic operations unit,

- no pipeline and

- no instruction level parallelism.

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8051 microcontroller features (contd.)

- on-chip RAM of 128 bytes. [8052-version RAM 256 bytes.]

- 32 bytes of RAM also used as four banks (sets) of registers. Each register-set (bank) thus eight registers.

- External data/stack memory can be added upto 64 kB in most version. In certain 8051 enhancements, this limit enhanced to 16 MB

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8051 microcontroller features (contd.)

- 8351 version on-chip ROM, 8751 version EPROM, 8951 version has on-chip EEPROM or flash memory of 4 kB.

- Several versions provide for higher capacity ROM. Additional program memory can be added externally upto 64 kB. In extended 8051 and unified address space versions (8051 EX and MX versions), this limit has been extended to 16 MB.

8051 microcontroller features (contd.)

- Two external interrupt pins, INT0 and INT1.

- Four ports of 8-bits each in single chip mode.

- Two timers

- Serial interface (SI)–programmable for three full duplex UART modes for serial IO. [IO with each bit of a word successive transmission on the data line for a time interval.] The same be programmable for half duplex synchronous IO

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8051 microcontroller features (contd.)

- In certain versions – DMA controller

- In certain versions– pulse width modulator and thus support to DAC, d.c. and servo motor controls.

- In Certain versions – modem, watchdog timer, ADC. Siemens SAB 80535-N supports ADC with programmable reference voltage. Advanced versions support these features and a version is selected as per the system requirement

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2. 8051 microcontroller instruction set

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Data Transfer Instructions

- Move byte between accumulator (an SFR) and register at a register bank
- Move byte from an SFR/Internal RAM to another *direct*
- Move *indirect*
- Move *immediate*, MOV *immediate* DPTR
- MOVC and MOVX *indirect*
- Exchange or Push or Pop *direct*

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Bit and Byte Manipulations and Logic instructions

Bit Manipulation

• Set, Complement, AND or OR or MOV the bit

Logic Instructions
• AND, XOR, OR Operation Instructions

Byte Manipulation
• Clear, Complement, or swap and Rotate Instructions

Arithmetic Instructions

- 8-bit Add, Subtract, Multiply and divide Instructions
- Increment-Decrement Instructions

Program Flow Control Instructions

- Branch instructions
- Conditional jumps
- Decrement and Jump conditional
- Compare and then conditional jump
- Subroutine Call Instructions
- NOP
- Delay

Interrupt Flow Control Instructions

- Interrupt flow control- mask bits, priority bits
- RETI

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Summary

We learnt

- 8051 architecture

- Instruction set of 8051

End of Lesson 1 of Chapter 2