Transistors

- The transistor is a main building block of all modern electronic systems.
- They are 3 terminal device and are of 2 types:

    1) Bipolar Junction Transistor (BJT)

    2) Field Effect Transistor (FET)

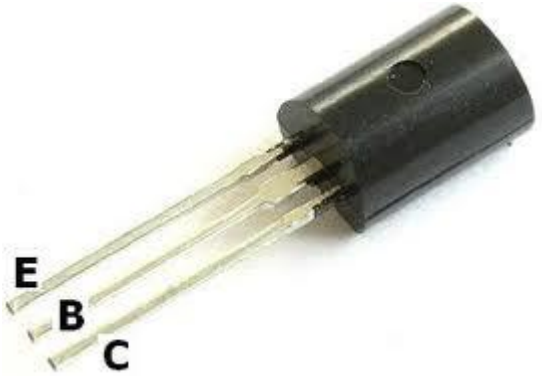
•BJT – output current, voltage and/or power is controlled by the input current. Conduction is due to **both e- and h+** so are called bipolar.

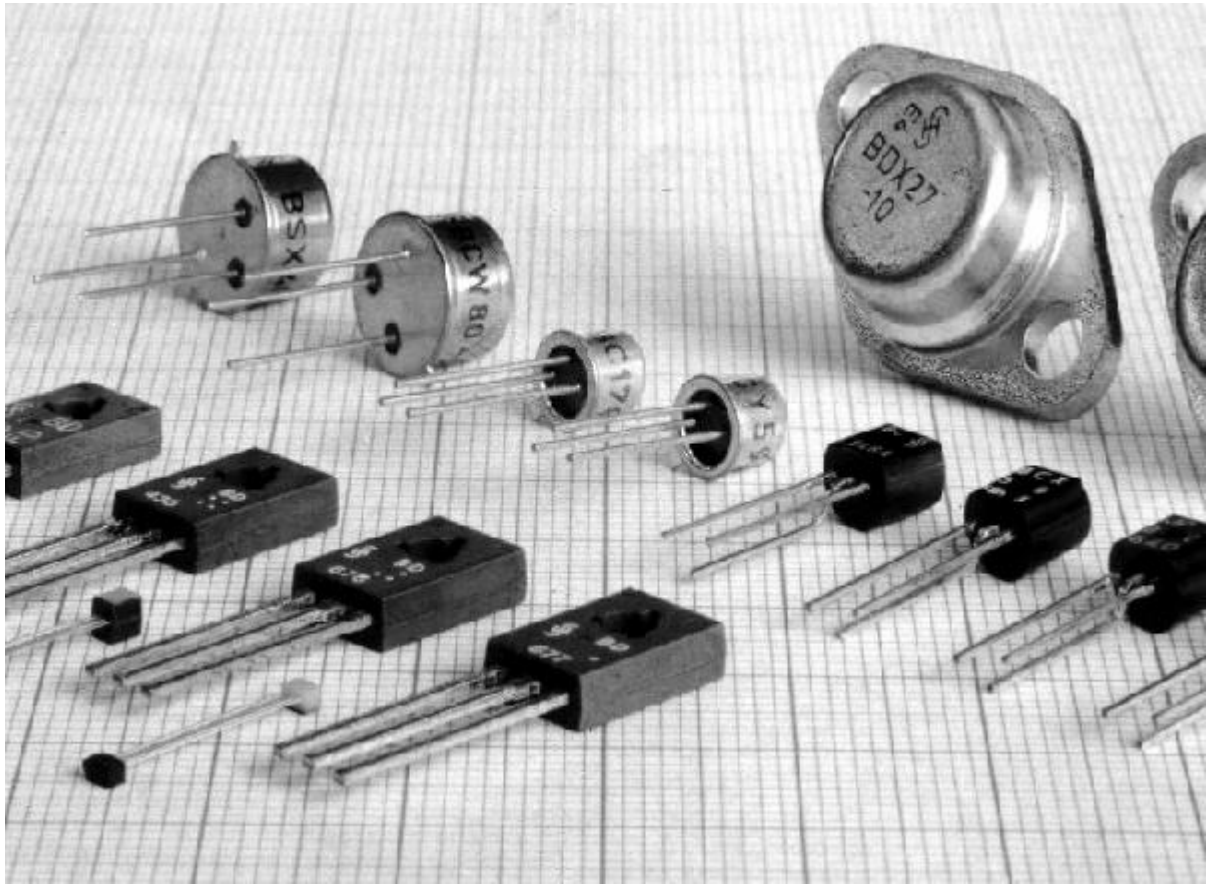
•FET- output characteristics are controlled by input voltage. Conduction is due to **either e- or h+** so are called unipolar.

•In communication systems transistors are widely used as the primary component in the Amplifier (circuit that is used to increase the strength ie: amplify, an ac signal).

•We will first consider BJT and look at FET later

Transistors

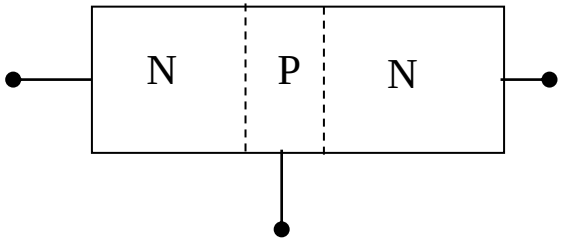




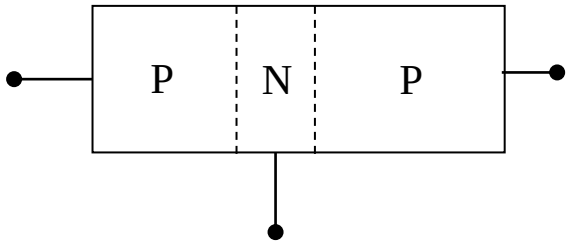
BJT

- The BJT transistor consists of 2 PN junctions and is formed from a single bar of for example Si (Group 14 SPT), that has been doped in the proper way.
- There are two ways to arrange the 2 PN junctions:

NPN Type

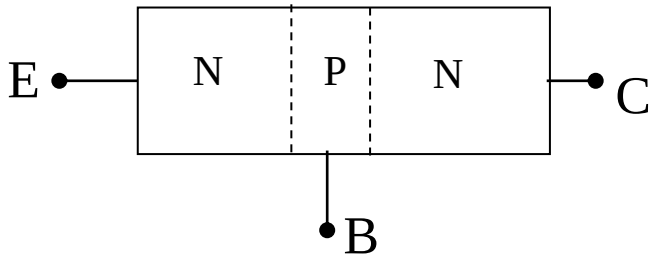


PNP Type

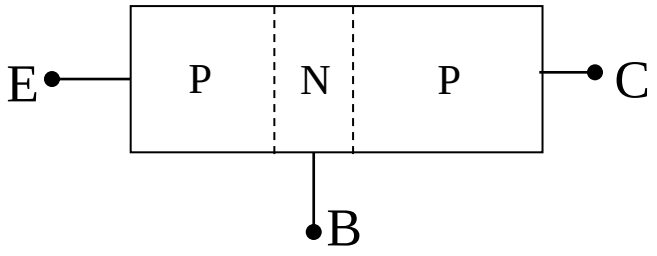


- The BJT has essentially 3 regions known as
  Emitter (E), Base (B) and Collector (C).
- All three regions are provided with terminals.
- The junction between the Emitter and Base is known as the Emitter-Base (E-B) junction
- The junction between the Collector and Base is known as the Collector-Base (C-B) junction

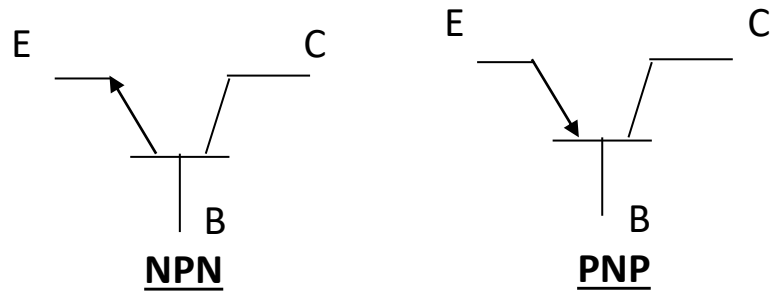
NPN Type



PNP Type



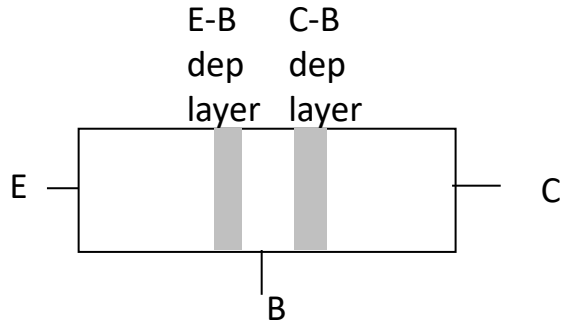
- **Emitter**: supplies charge carriers (e- and h+) to the other two regions – this is a heavily doped region
- **Base**: Middle region that forms the 2 PN junctions. The base of the transistor is thin as compared to the E and is a lightly doped region
- **Collector**: collects the charge carriers (e- and h+). Always larger than the E and B. Its doping is intermediate between the E and B.



- **Circuit Symbols:** (Arrow points from P to N and indicates direction of conventional current flow).
- PNP transistor is a complement of NPN.
- NPN- majority careers are free e-.
  PNP- majority careers are h+.
- We will discuss in terms of NPN. For PNP reverse direction of current and polarity of supplies

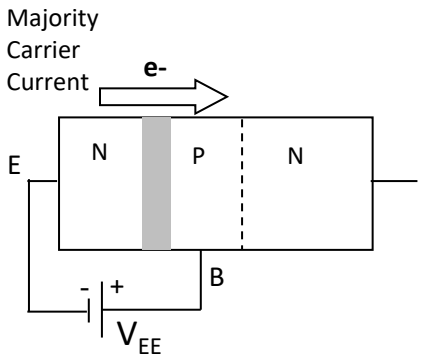
Unbiased Transistor

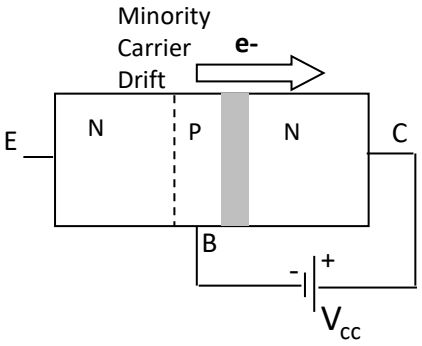
- Transistor with E, B and C terminals left open is called an unbiased transistor or open-circuited transistor.
- Diffusion across the PN junctions produce 2 depletion layers.
- **E-B depletion layer:** penetrates slightly into the Emitter (heavily doped) but deeply into the Base (lightly doped).
- **C-B depletion layer:** penetrates more into the Base (lightly doped) and less into the Collector (intermediate doping between E and B).
- E-B depletion layer width is smaller than that of the C-B depletion layer.



- An unbiased transistor is never used in practice.
- In practice all terminals are connected to DC voltage sources (or batteries).
- For proper transistor action it is necessary to bias both PN junctions.
- We first look at biasing the NPN transistor in Common Base configuration.

Common Base Configuration





i) E-B Junction – Forward Biased by DC source V_{EE}.

ii) –ve terminal of V_{EE} connected to N or E, +ve terminal of V_{EE} connected to P or B

iii) Substantial flow of diffusion current across junction due to flow of majority. carriers (e-) from N type E

C-B junction is reverse biased by DC source V_{CC}.

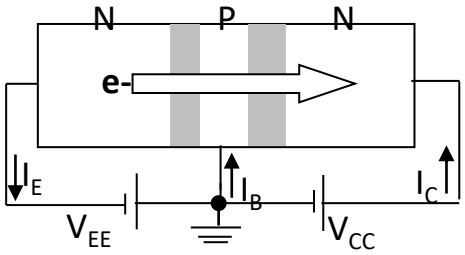
+ve terminal of V_{CC} to N or C,

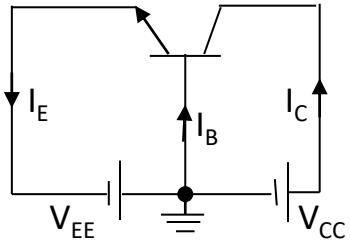
–ve terminal of V_{CC} to P or B

Depletion layer is widened and only current flow from B to C is due to the minority e- crossing the junction

Rule for Biasing: E-B junction FB; C-B junction RB

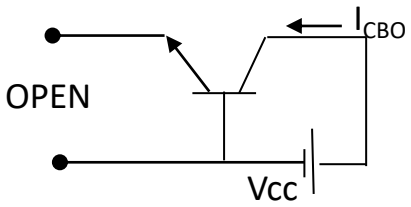
- Rule for Biasing: E-B junction FB; C-B junction RB





$$I_E = I_C + I_B$$

Common-Base Transistor Gain and I_{CBO}:



- If Emitter is open. No carriers injected to Base from E.
- The only current that flows is due to thermally generated carriers.
- This current is called reverse saturation current and designated as
  I_{CBO} the Collector to Base current with Emitter open.
- NB: I_{CBO} can be considered same as the reverse diode current.

- Total collector current I_c consists of
  1) current produced by normal transistor action called injected current $I_c(INJ)$, and
  2) Reverse saturation current I_{CBO}.
- Therefore total collector current Ic = Ic(INJ) + I_{CBO}

- Important parameter

  $$\alpha = I_c(INJ) / I_E$$

  measures portion of Emitter current that pass through the Base to become Collector current.
- α is always < 1
- Greater the value of α (the closer it is to 1) the better the transistor.
- For typical transistors $\alpha = 0.95$ to 0.995.

$I_c(INJ) = \alpha I_E$ and therefore $I_c = \alpha I_E + I_{CBO}$

- Value of I_{CBO} is usually very small compared to I_E, so
- $I_c = \alpha I_E$ or
- $\alpha = I_c / I_E$ and is called the Common-Base DC current gain

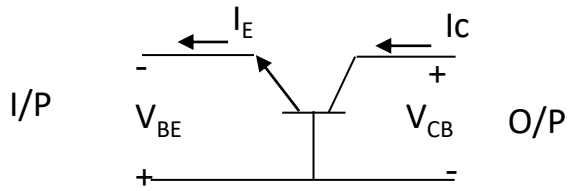
Transistor Characteristics

1) Input Characteristics: gives relationship between the input current and input voltage for a given output voltage,

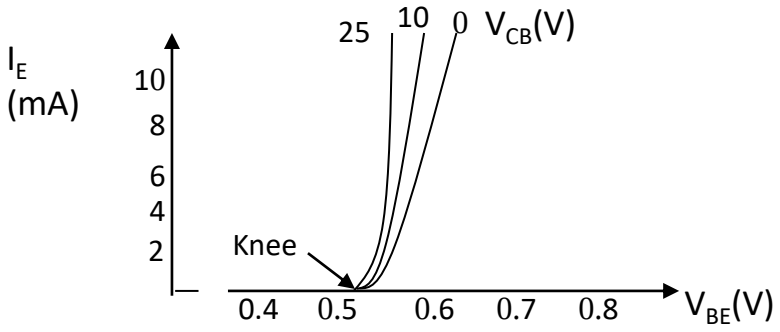
2) Output Characteristics: gives relationship between the output current and voltage for a given input current.

Common Base Characteristics

Input/output voltages and currents



Input Characteristics



(1) There is a threshold voltage (knee, offset, cut-in) below which Emitter current is very small [this voltage is 0.7V(Si), 0.3V(Ge)],

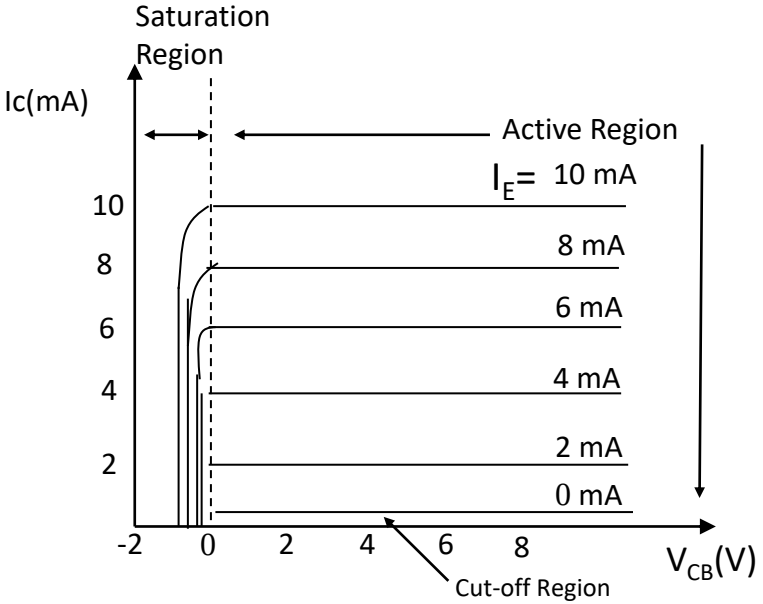
(2) Beyond the knee for fixed V_{CB}, I_E increase rapidly with V_{BE}

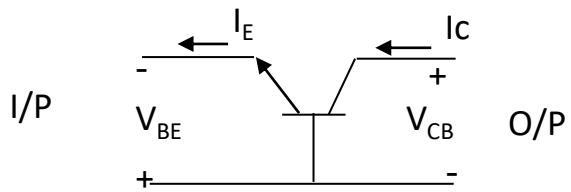
Means the input resistance is small

(3) As V_{CB} increases the curves shift upwards,

- Can determine the value of ac resistance $R_i = \Delta V_{BE} / \Delta I_E$
- The ac input resistance depends on the location of the operating point selected along the curve.

Common-Base Output Characteristics:





(1) Curves may be divided into three regions: saturation, active and cut-off regions.

(a) Saturation : V_{CB} is negative for NPN transistor. Means C-B junction is also FB.

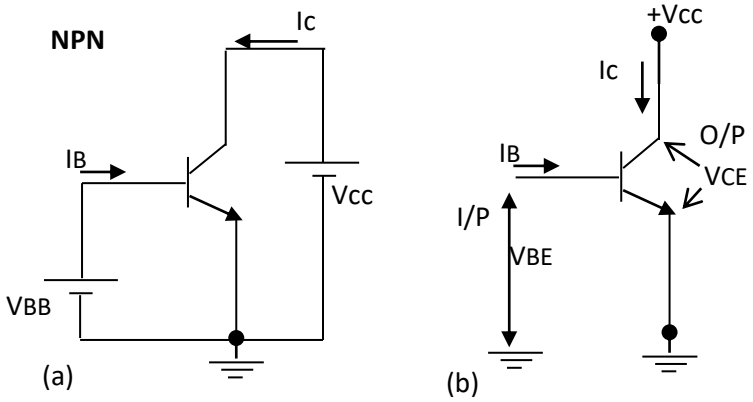
(b) Active : Collector current is constant and nearly equal to Emitter Current ($\alpha \approx 1$),

(c) Cut-off: Along the horizontal axis. Correspond to $I_E = 0$. Both junctions RB.

(2) Collector current flows even when V_{CB} is zero. This is due to e- being injected into the base under the FB E-B junction. These e- reach Collector due to internal junction barrier potential.

(3) A small current flows for I_E=0 this is the I_{CBO}

Common Emitter Configuration:



- Previous eqns

$$Ic = \alpha I_E + I_{CBO}$$

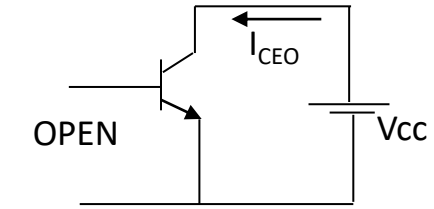
$$Ic/\alpha - I_{CBO}/\alpha = I_E = Ic + I_B$$

$$Ic(1/\alpha - 1) = I_B + I_{CBO}/\alpha$$

$$Ic = \alpha I_B/(1-\alpha) + I_{CBO}/(1-\alpha) = \beta I_B + I_{CBO}/(1-\alpha)$$

$\beta = \alpha/(1-\alpha)$ is the Common-Emitter DC current gain.

β is always > 1, and ranges from 20 to several hundred.

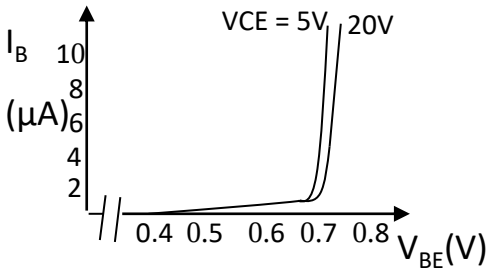


(c)

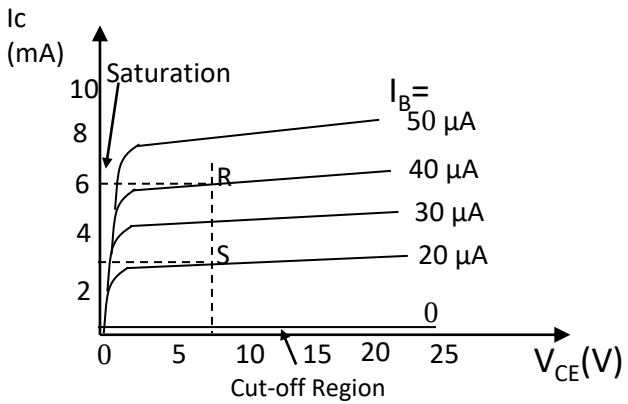
- Fig (c): Base-Emitter circuit left open while RB (V_{CC})remains connected.
- The only current that can flow is the reverse current across Collector-Base junction.
- Current flows from C through B to E.
- This is designated I_{CEO}, the Collector to Emitter current when Base is open.
- NB: I_{CEO} is in the same direction as Ic.
- Since $I_B = 0$, $I_{CEO} = [1/(1-\alpha)]\ I_{CBO}$.
- As α is close to 1, (1-α) is close to zero and 1/(1-α) can be quite large.
- So the Common Emitter leakage current >> Common Base leakage current.
- $Ic = \beta I_B + I_{CBO}/(1-\alpha) = \beta I_B + I_{CEO}$.
- Although $I_{CEO} >> I_{CBO}$, it is still very small compared to βI_B.
- Therefore, $Ic = \beta I_B$ and **$\beta = Ic/I_B$**

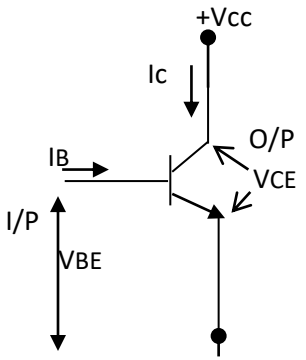
Common-Emitter Characteristics

Input Characteristics



Output Characteristics





- Note: I_B in μA and Ic in mA

(1) There is a threshold voltage (0.7 for Si,0.3 for Ge) below which Base current is very small.

(2) Can be used to find ac input resistance $R_i = \Delta V_{BE}/\Delta I_B$. R_i varies with location of operating point. Ranges from 600Ω-4kΩ

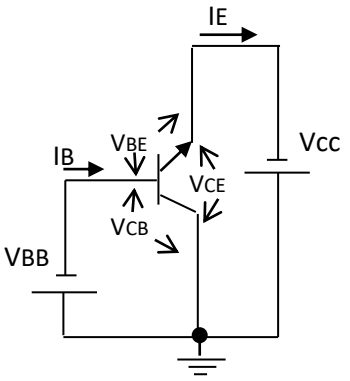
(1)Can be divided into 3 parts: saturation, active and cut-off regions.

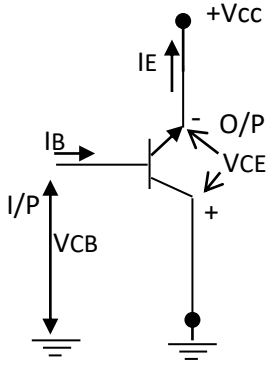
(2) Can be used to find ac output resistance $Ro = \Delta V_{CE}/\Delta I_B$. From 10kΩ-50kΩ

(3) Can find β. Ex: from points R and S

β = (6-3)mA/ (40-20)μA = 150

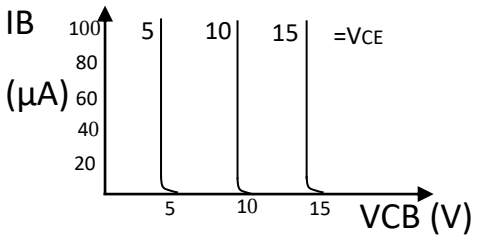
Common-Collector Characteristics: NPN



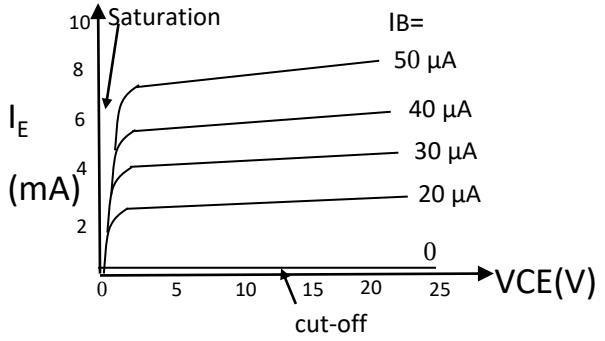


- From before $Ic = \beta I_B$
- but $I_E = Ic + I_B = \beta I_B + I_B$
- $I_E = (\beta + 1) I_B$

Input Characteristics



Output Characteristics



Example 1

A transistor has I_{CBO} = 48 nA and α = 0.992

1. Find β and I_{CEO}
2. Find its exact collector current when I_B = 30 µA
3. Find the approximate collector current, neglecting leakage current

Required equations $I_c = \alpha I_B/(1-\alpha) + I_{CBO}/(1-\alpha)$

$\beta = \alpha/(1-\alpha)$

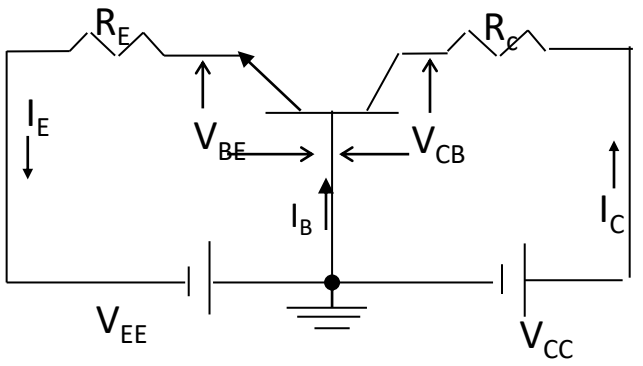
Bias Circuits

- So far we considered bias in terms of adjusting the DC supply voltages.
- In practice we do this by having resistors in series with the DC supplies.
- We consider adjusting the value of bias

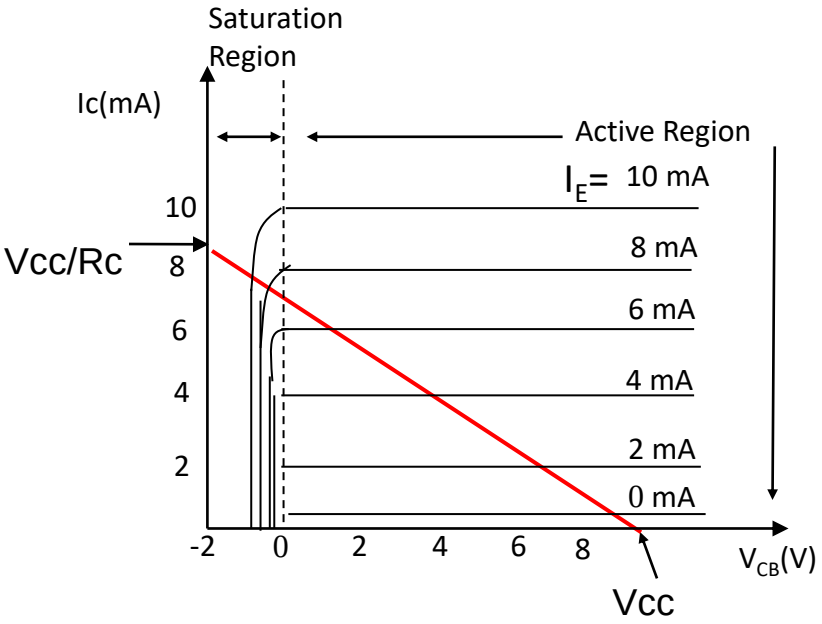
  (a) to obtain specific values of input and output current and voltages,

  (b) when we have achieved this we have set the bias point.

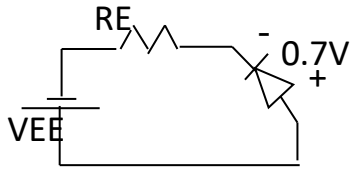
Common-Base Bias Circuit:

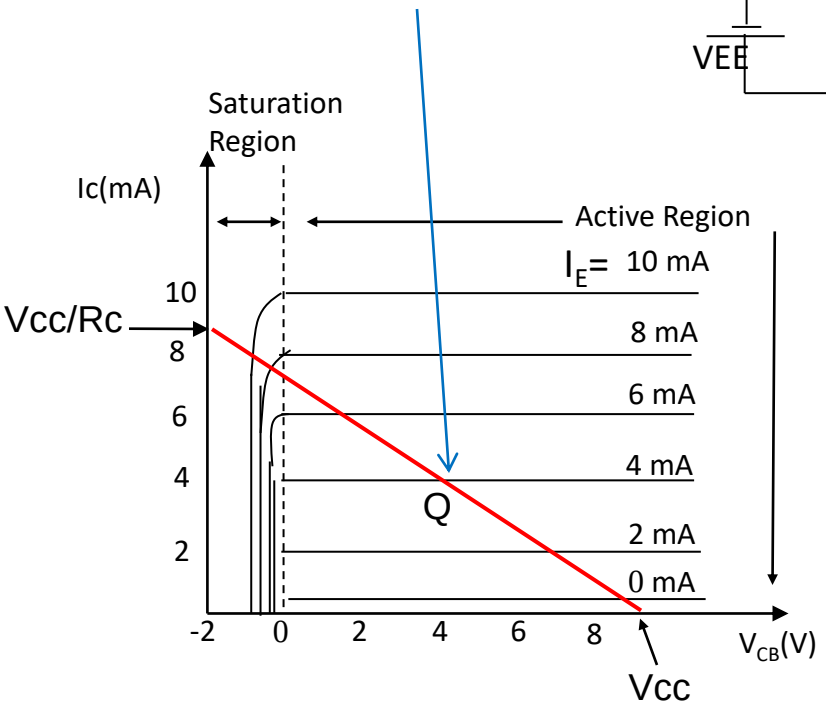


- Input voltage no longer V_{EE} because there is a voltage drop across R_E.
- Similarly for output.
- But characteristics are still valid
- Kirchoff's Law for the output loop $V_{cc} = I_cR_c + V_{CB}$
- Rearrange as: $I_c = -(1/R_c)V_{CB} + V_{cc}/R_c$
- Consider I_c and V_{CB} as variables and V_{cc} and R_c as constants.
- This is an equation of a straight line with slope $-1/R_c$
  and intercepts $V_{CB}=V_{cc}$ and $I_c=V_{cc}/R_c$
- This is the load line for the transistor and can be plotted in the
  Common-Base output characteristics to find the point of intersection Q or Bias point.


Saturation
Region
Ic(mA)
Active Region
I_E= 10 mA
8 mA
6 mA
4 mA
2 mA
0 mA
10
Vcc/Rc
8
6
4
2
-2
0
2
4
6
8
V_{CB}(V)
Vcc

- To determine the point of intersection we need to know the current I_E.
- Most practical way is to regard the B-E junction as a FB diode having a voltage drop of 0.7V (for Si) and solve for diode current.
- This gives $I_E = (V_{EE} - 0.7)/ R_E$





- But transistor output characteristics are seldom used to design or analyze transistor circuits because transistors of the same type have a wide variation in their characteristics.
- The entire bias circuit is analyzed by a set of equations, which can solve for all the input and output current and voltages.

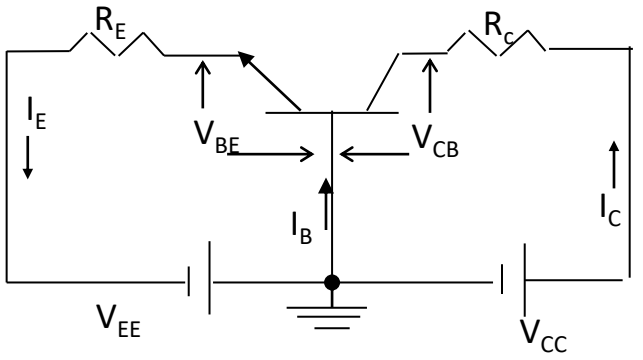
- **NPN C-B Circuit Equations**:

$$V_{BE} = 0.7 \text{ (Si)}, 0.3 \text{ (Ge)}$$

$$I_E = (V_{EE} - V_{BE})/R_E$$

$$Ic = I_E - I_B \approx I_E$$

$$V_{CB} = V_{cc} - I_c R_c$$

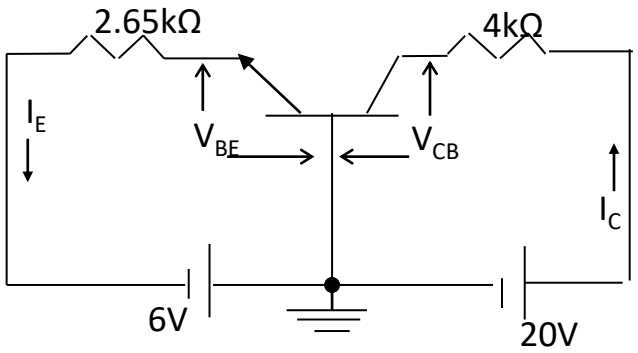


- We can also get expressions for R_E and Rc from these equations to chose R_E and Rc values for desired input and output current and voltages.

$$R_E = (V_{EE} - V_{BE})/ I_E$$

$$Rc = (Vcc - V_{CB})/ I_C$$

Example 2

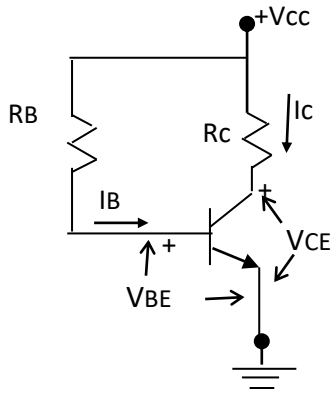


Determine the

1) equation of the load line for the circuit for the Si transistor

2) Operating point

Common-Emitter Bias Circuit



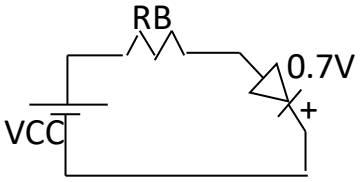
- It has only a single supply of voltage Vcc.
- * R_B and Rc must be chosen so that,

  voltage drop across R_B > voltage drop across Rc

  to keep C-B junction RB.

  $Vcc = IcRc + V_{CE}$ or $Ic = (-1/Rc)V_{CE} + Vcc/Rc$

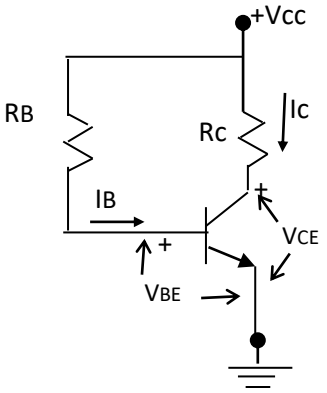
  We can again draw the load line on the output characteristics to find Q the bias point.
- Need to know I_B to determine Q
- I_B is given by (diode circuit) $I_B = (Vcc-V_{BE})/R_B$



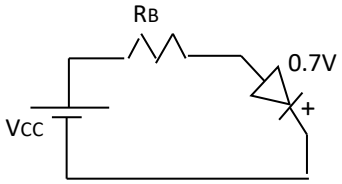
- The set of equations are

NPN C-E Circuit:

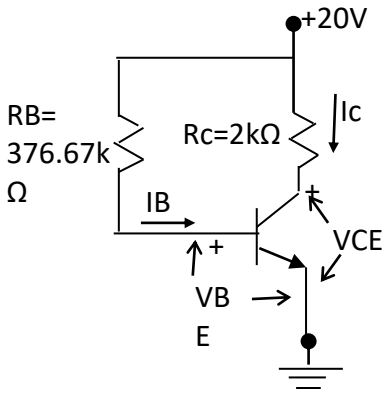
$$V_{BE} = 0.7 \text{ (Si)}, 0.3 \text{ (Ge)}$$
$$I_B = (Vcc - V_{BE})/R_B$$
$$Ic = \beta I_B$$
$$V_{CE} = Vcc - IcRc$$



$$R_B = (Vcc - V_{BE}) / (Ic/\beta)$$
$$Rc = (Vcc - V_{CE}) / Ic$$



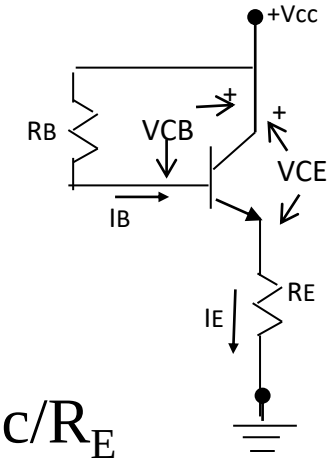
Example 3



The Si transistor in the CE bias circuit has β=100.

Find the bias point

Common-Collector Bias Circuit

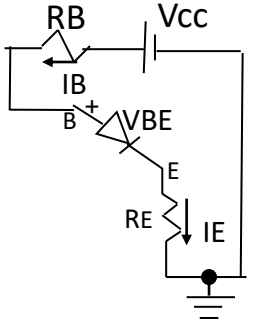


- $Vcc = I_E R_E + V_{CE}$ or $I_E = -(1/R_E)V_{CE} + Vcc/R_E$
- To find I_B to determine bias point (diode circuit)

  $Vcc = I_B R_B + V_{BE} + I_E R_E$

  But $I_E = (\beta+1)I_B$
- Substitute and rearrange to get

  $I_B = (Vcc - V_{BE}) / [R_B + (\beta+1)R_E]$



- **NPN C-C Circuit**

$V_{BE} = 0.7$ (Si), 0.3 (Ge)

$I_B = (Vcc - V_{BE}) / [R_B + (\beta+1)R_E]$

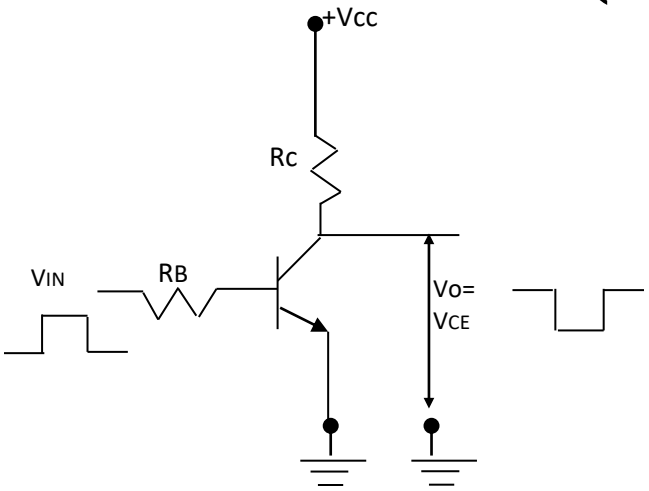
$I_E = (\beta+1)\, I_B$

$V_{CE} = Vcc - I_E R_E$

$R_E = (Vcc - V_{CE}) / I_E$

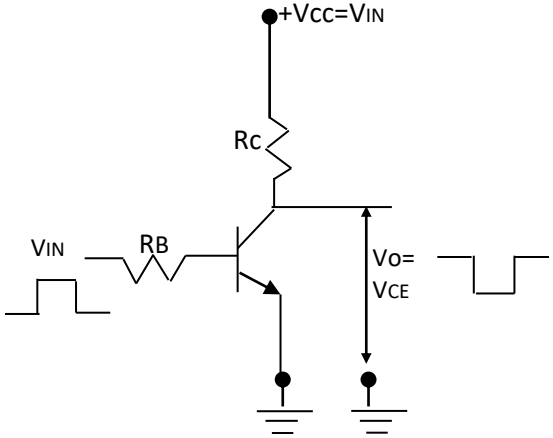
$R_B = (\beta+1)(Vcc - V_{BE} - I_E R_E) / I_E$

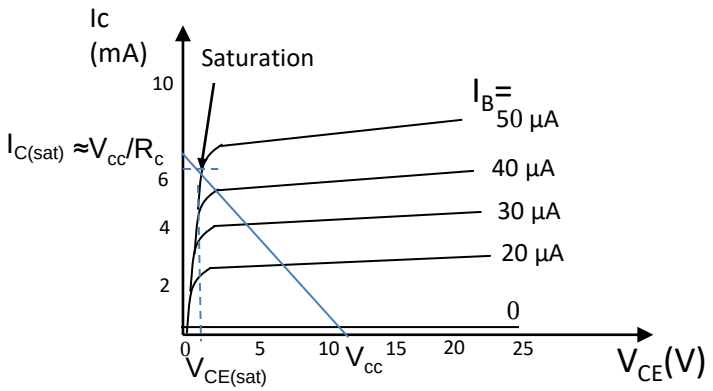
BJT Transistor as a switch (BJT Inverter)



- Widely used in digital circuits and switching applications.
- We will consider the NPN inverter.
- Transistor is in C-Econfiguration.
- No bias voltage is connected to the base.
- R_B is connected in series to base and then directly to a square or pulse type waveform that serve as inverter input.
- We make $V_{cc} = V_{in}$

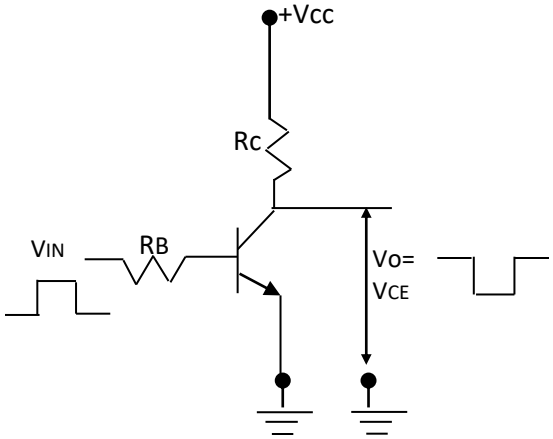
BJT Transistor as a switch (BJT Inverter)

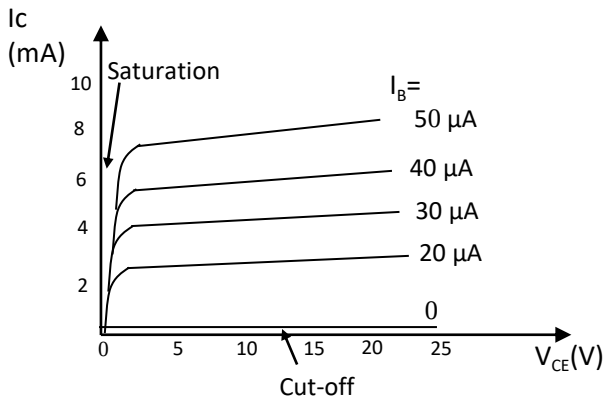




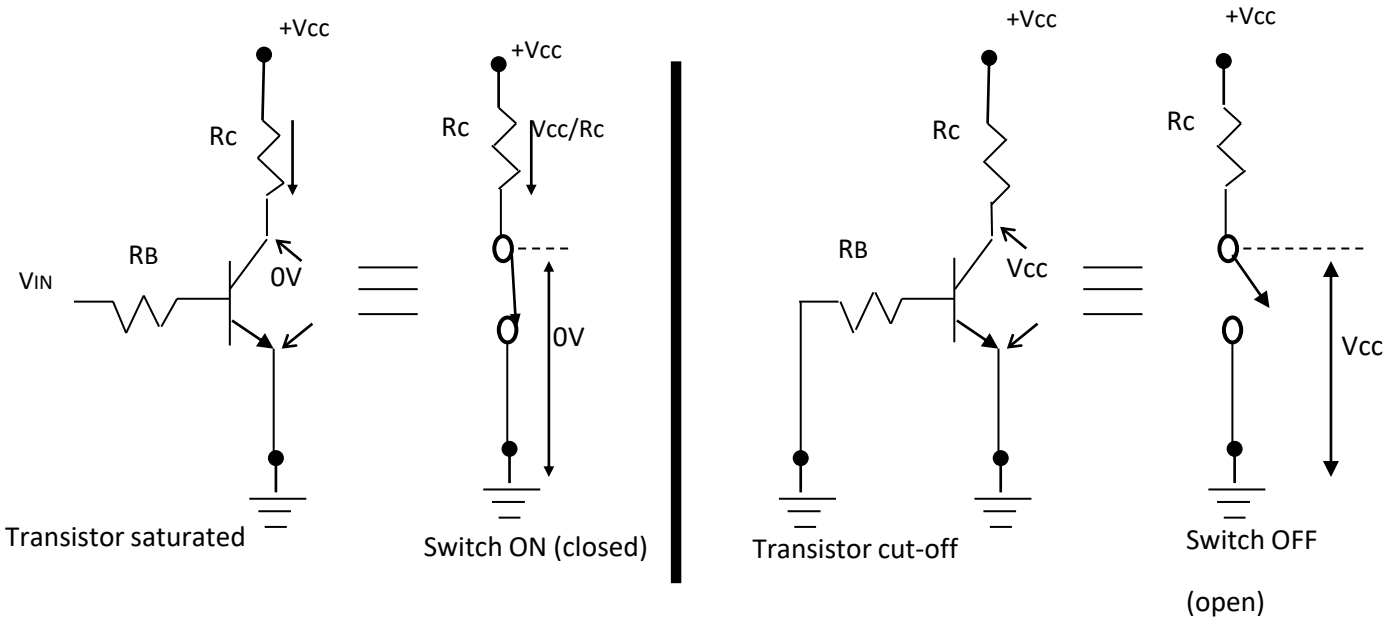
- When input to the inverter is High the B-E junction is FB and current flows through R_B to base.
- *We choose R_B and Rc so that amount of base current flowing is enough to **saturate** the transistor ie: drive the transistor to the saturation region.
- The value of V_{CE} corresponding to this point called $V_{CE(sat)}$ is very nearly zero (very small typically 0.1V). (see C-E charac. curve).
- Current at saturation point is called $I_{c(sat)} \approx Vcc/Rc$.
- When transistor is saturated it is said to be ON.
- Therefore High input to transistor results in Low output (0V).

BJT Transistor as a switch (BJT Inverter)

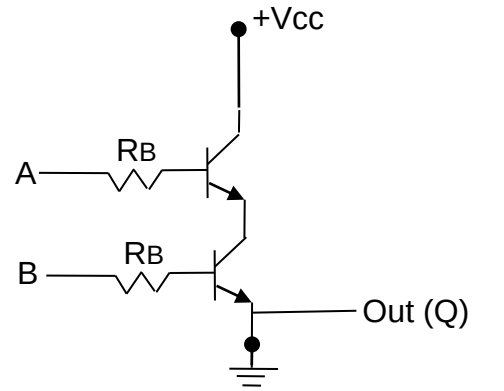


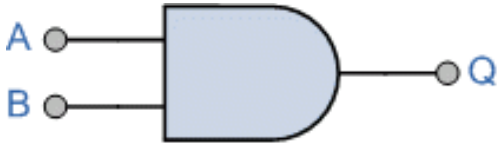


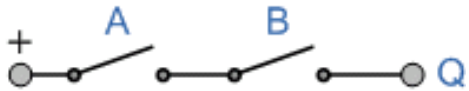
- When input to transistor is Low ie: 0V, B-E junction has no FB applied to it and hence no collector current flows.
- No voltage drop across Rc, and so V_{CE}=Vcc.
- In this situation transistor is in the cut-off region and is said to be OFF.
- A low input to the transistor results in a high output.


+Vcc
Rc
RB
VIN
0V
+Vcc
Rc
Vcc/Rc
0V
Transistor saturated
Switch ON (closed)
+Vcc
Rc
RB
Vcc
+Vcc
Rc
Vcc
Transistor cut-off
Switch OFF
(open)

AND Gate



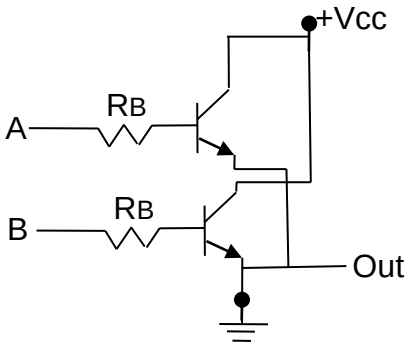


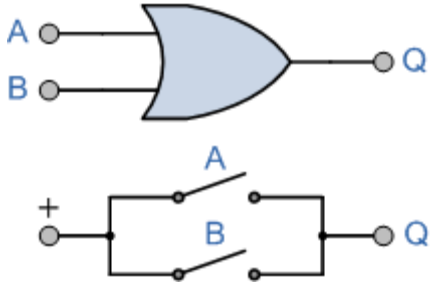


Truth Table

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate



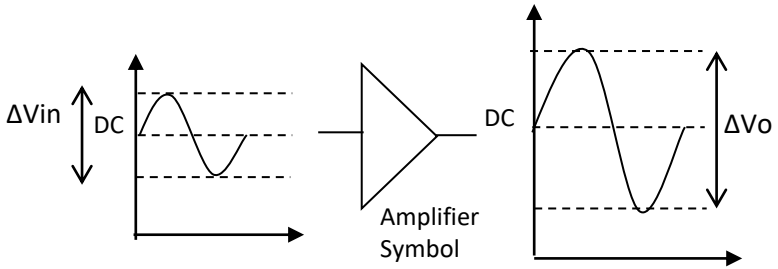


Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

BJT Transistor as Amplifier

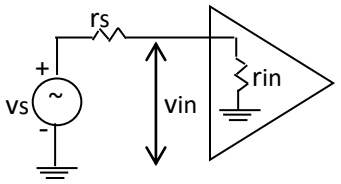
- Consider small signal operation which means that the output variations are small and that there is no change in the value of device parameters (α, β etc.).
- The transistor amplifier is studied from the standpoint of transistor behaviour as an AC amplifier.
- **Amplifier Gain:** AC voltage gain
- $A_v = \Delta V_o / \Delta V_{in}$



- For voltage amplifier $A_v > 1$.

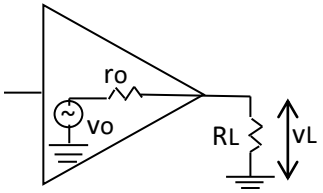
- Only the AC components of the input and output are used to compute voltage gain.
- DC values have no bearing on the value of gain.
- AC current gain $A_i = \Delta I_o / \Delta I_{in}$
- Device with $A_i > 1$ is a current amplifier.
- It is possible to have $A_v > 1$ and $A_i < 1$.
- Power Gain $A_p = P_o / P_{in} = A_v A_i$

Source Resistance:



- Every signal source has internal resistance called source resistance.
- If r_{in} is the amplifier input resistance, r_s and r_{in} are in series and form a voltage divider across the input of the amp.
- Input voltage $v_{in} = [r_{in} /(r_s+r_{in})]v_s$
- Output voltage $v_o = A_v\, v_{in}$
- Therefore $v_o / v_s = A_v\, [r_{in} /(r_s + r_{in})]$ **(Edit in handout)
- Thus the overall amp gain is reduced by a factor $[r_{in} /(r_s + r_{in})] < 1$
- If $r_{in} >> r_s$ then $[r_{in} /(r_s + r_{in})] \approx 1$ and there is little reduction in amp gain.
- Therefore for a voltage amplifier it is desirable to have a large input resistance.
- If current amplification is desired, $i_o / i_s = Ai\, [r_s /(r_s + r_{in})]$.
- Therefore the current amplifier should have a small input resistance.

Load Resistance:



- If r_o is output resistance of amp

$$v_L = [R_L/ (r_o + R_L)]\, v_o$$

- Therefore for a voltage amp $r_o << R_L$ so that $v_L = v_o$
- For current amp

$$i_L = [r_o/ (r_o + R_L)]\, i_o$$

- Therefore for current amp $r_o >> R_L$

- When both source r_s and load R_L are taken into account
- Overall voltage gain

$$v_L / v_s = A_v[r_{in} /(r_s + r_{in})][R_L/ (r_o + R_L)]$$

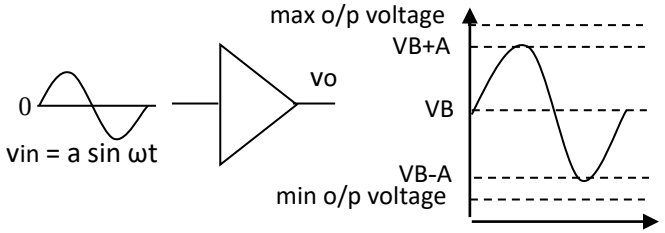
- Overall current gain

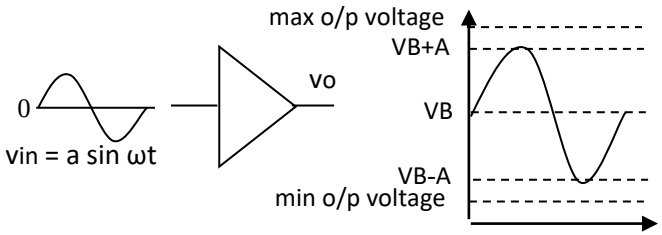
$$i_L / i_s = A_i [r_s /(r_s + r_{in})] [r_o/ (r_o + R_L)]$$

- If r_s is fixed, maximum power transferred from source to amp when $r_{in} = r_s$
- Amp is matched to the source.
- If r_o is fixed, maximum power transferred to load when $R_L = r_o$
- Amp matched to load.

Purpose of Bias:

- In most single transistor amplifiers, the output voltage must always be +ve for NPN (or –ve for PNP).
- When this is the case, it is not possible for the output to be a pure AC waveform.
- The purpose of bias in a transistor amplifier is to set a DC output level somewhere in the middle of the total range of possible output voltages so that an AC waveform can be superimposed on it.
- The AC input causes the output voltage to vary above and below the bias voltage, but the instantaneous values of the output are always positive, in this example.



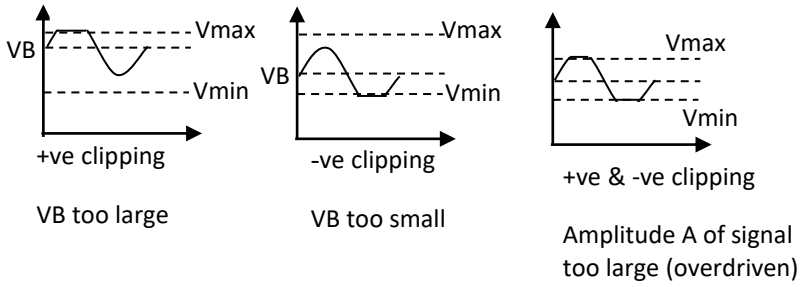


- Output voltage $vo = V_B + A \sin(\omega t)$ where V_B is bias voltage or DC component of the output.
- A is the peak value of the sinusoidal AC output
- Values of V_B and A must be such that:

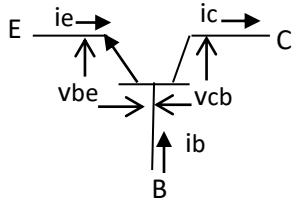
  $V_B + A$ is not greater than maximum o/p voltage and

  $V_B - A$ is not less than minimum o/p voltage.
- If this condition is not satisfied output voltage will reach its minimum or maximum extremes before the total AC variation take place.

- Result is a flattening of the output signal which is called ‘clipping’.
- Purpose of AC amp is to have as output an amplified version of the input.
- Clipping distorts the output signal and is an example of amplitude distortion.



Amplifier analysis:



- Small signal parameters are parameters whose values are determined under small signal (ac) operating conditions (we will use simple letters to signify ac).
- Ex: $\beta = i_c/i_b \mid V_{CE}$=constant; $\alpha = i_c/i_e \mid V_{CB}$=const.
- An important physical parameter is the small signal resistance from Emitter to Base called the emitter resistance r_e

  $$r_e = v_{be} / i_e \mid V_{CB} = \text{const}$$

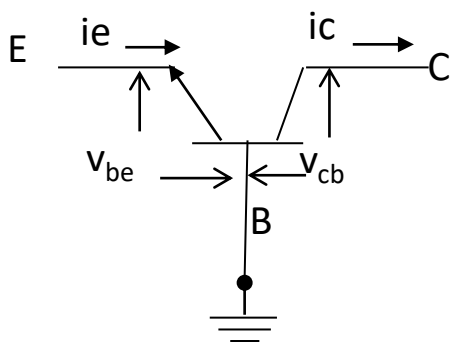
  * r_e is the same as the Common-Base input resistance
- Since E-B junction can be seen as a FB diode an approximate value of re can be found (same as dynamic resistance of a diode), $r_e = 0.026/I_E\ \Omega$, where I_E is the DC emitter current.
- Small signal collector resistance r_c is the ac resistance from collector to base (output resistance in Common-Base).
- Because it is across a reverse bias junction $r_c = v_{cb}/i_c \mid I_E$=const

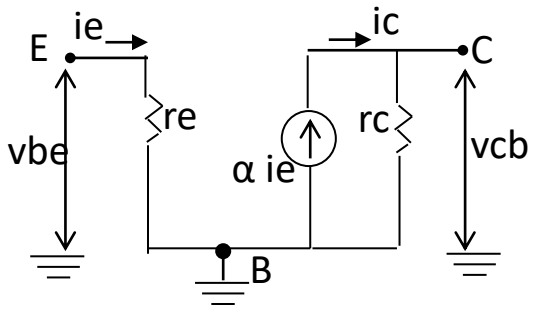
  it is of the order of several MΩ.

Equivalent Circuits: small signal model of transistor.

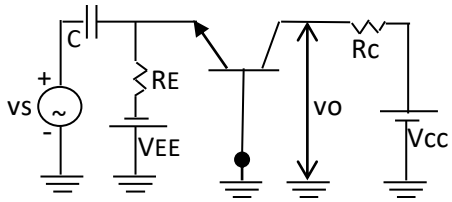
(We will only consider the simplified model that does not take into account reverse currents. There is a more accurate model called the Hybrid model)

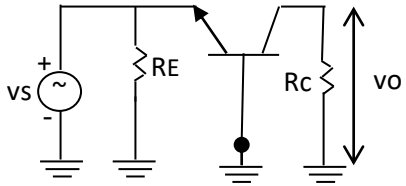
- **C-B Amplifier Model:** All voltages and currents are ac quantities, all polarities periodically alternate.
- **Equivalent Circuit:** Circuit model for C-B Transistor.
- Figure shows that an increase in current into E is accompanied by an increase of current out of Collector.





C-B Amplifier Model: **ac Equivalent:** of that is external to transistor.

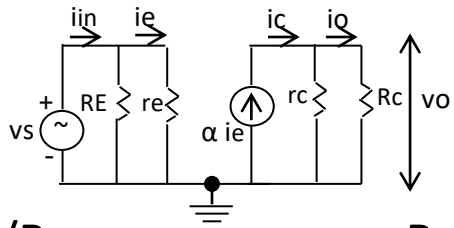


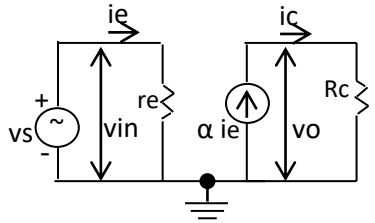


All DC sources (and C)are treated as ac short circuits to ground.

Replace transistor with small signal equivalent circuit.

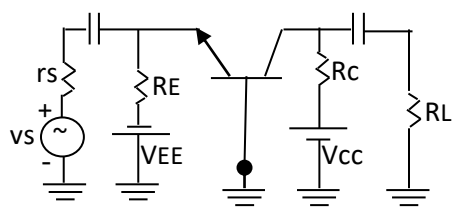
Practical C-B Equivalent circuit (// means in parallel)

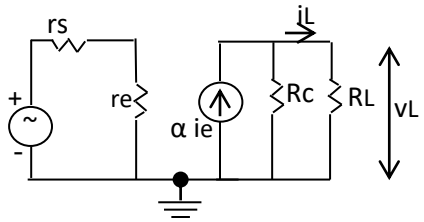




- $R_E >> r_e$: $r_e // R_E \approx r_e$ $r_c >> R_c$: $R_c // r_c \approx R_c$
- $v_s = v_{in} = i_e r_e$ $v_o = i_c R_c = \alpha i_e R_c$
- but $\alpha \approx 1$, $v_o = i_e R_c$ **Voltage Gain** $A_v = v_o/v_{in} = \alpha R_c / r_e \approx R_c / r_e$
- **Current Gain**: $A_i = i_o/i_{in} = i_c/i_e = \alpha$

C-B Amplifier with source and load: **ac equivalent:**

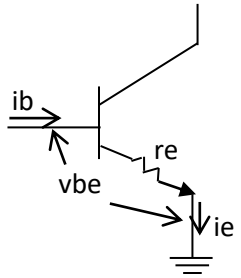




- $A_v = v_L / v_s = (R_c / r_e)[r_e /(r_s+r_e)][R_L /(R_c+R_L)]$

- $A_i = i_L / i_s = \alpha\,[r_s /(r_s+r_e)][R_c /(R_c+R_L)]$
  where $i_s = v_s / r_s$

Common-Emitter Amplifier model: Input resistance re drawn inside the emitter terminal to emphasize that it is an internal transistor parameter.



ac input resistance $r_{in} = v_{be} / i_b$

But $i_e = (\beta+1)\, i_b$ which can be derived from the DC relations.

Then $r_{in} = (\beta+1)\, v_{be} / i_e$

But $v_{be} / i_e = r_e$

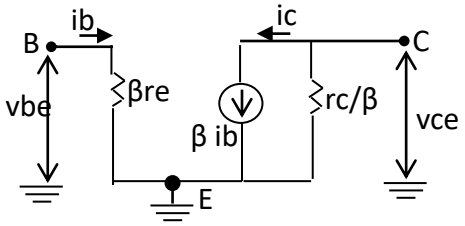
Therefore $r_{in} = (\beta+1)\, r_e \approx \beta\, r_e$ as $\beta >> 1$

Equation shows that for C-E configuration input resistance is β times greater than C-B configuration.

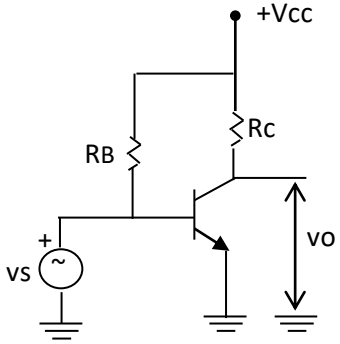
Similarly, output resistance is β times smaller than C-B configuration.

*Hence, C-E amplifier is inherently better suited for voltage amplification than the C-B counterpart (see slides 40 and 41).

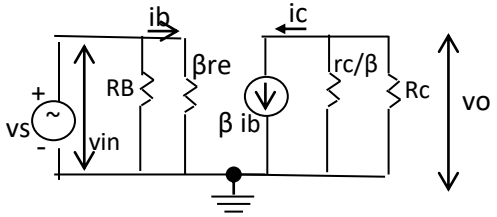
C-E Transistor Equivalent Model:



C-E Amplifier

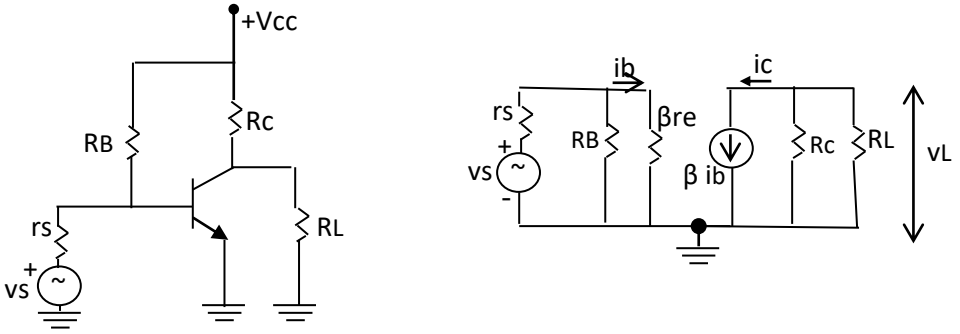


Equivalent Circuit



- r_c/β is in parallel with Rc.
- In most practical circuits $r_c/\beta >> Rc$ so that $r_c/\beta // Rc \approx Rc$
- Therefore output resistance $r_o = Rc$
- Output voltage $v_o = i_c\, r_o = \beta\, i_b\, Rc$.
- From equivalent circuit $v_{in} = \beta\, r_e\, i_b$.
- Therefore voltage gain $A_v = v_o/v_{in} = -Rc/r_e$
- Negative sign inserted to show ac output is 180° out of phase with ac input. Current gain $A_i = i_c/i_b = \beta$

C-E Amplifier with source and load

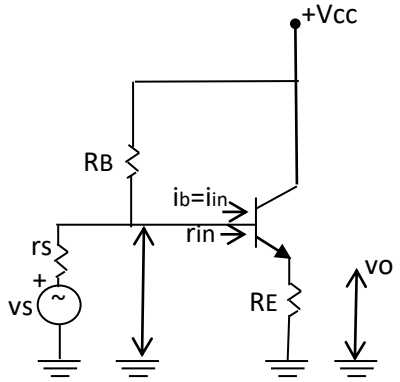


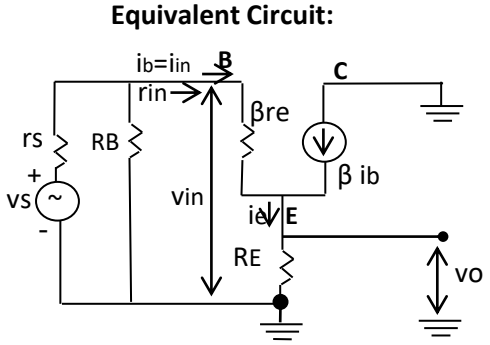
- $v_L/v_s = A_v\,[(R_B//\beta r_e)/(r_s+R_B//\beta r_e)]\,[R_L/(R_L+Rc)]$ where $A_v = -Rc / r_e$
- $i_L/i_s = A_i\,[(r_s//R_B)/(r_s//RB+\beta re)][Rc/(R_L+Rc)]$
- **Effect of ac load resistance:** using load resistance terms only
- $A_{vo} = v_L/v_s = -(Rc/r_e)[R_L/(R_L+Rc)] = -(1/re)[(R_L Rc/(R_L+Rc)]$

  $= -(1/r_e)(R_L//Rc) = -r_L/re$

  where r_L is ac load resistance.
- Therefore A_{vo} is proportional to $r_L = R_L//Rc$.
- Since $R_L//Rc < Rc$, the effect of connecting a load R_L to the amplifier is to reduce the voltage gain

Common-Collector Amplifier model:





- Collector shown grounded in ac equivalent as DC sources are treated as ac short circuits. Resistance between Base and Emitter is shown as $\beta r_e \approx (\beta+1)r_e$.
- The input resistance at the Base of the transistor (between Base and Ground)

  $r_{in} = v_{in}/ i_{in} = v_{in}/ i_b$

  $v_{in} = i_b(\beta+1)r_e + i_eR_E$ (we have replaced β with β+1).

  $= i_b(\beta+1)r_e + (\beta+1)i_bR_E = i_b(\beta+1)(re+R_E)$.

  Therefore $r_{in} = [i_b(\beta+1)(r_e+R_E)]/ i_b = (\beta+1)(r_e+R_E)$.

  Let $(\beta+1)\approx \beta$ so $r_{in} \approx \beta(r_e+R_E)$.
- In many practical cirCuits $R_E >> re$. So $r_{in} \approx \beta R_E$

- Voltage Gain $A_v = v_o / v_{in} = i_e R_E / v_{in}$
- Substituting for v_{in} and simplifying $A_v = R_E/(r_e+R_E)$
- Since $r_e+R_E > R_E$ equation shows that the Common-Collector Amplifier always has a voltage gain < 1
- Also as $R_E >> r_e$ then $Av \approx 1$ or $v_o = v_{in}$
- Therefore the ac output voltage ≈ ac input voltage in Common-Collector configuration.
- There is no phase change between the input and output and are separated only by the small resistance of the Forward Biased B-E junction.
- Since output voltage is the same as the input voltage in amplitude and phase, the Emitter is said to follow the Base and is known as the **Emitter Follower** rather the Common-Collector.
- Current Gain $A_i = i_e / i_b = (\beta+1) \approx \beta$. Therefore Current Gain can be >> 1 and so is the Power Gain $A_p = A_v A_i \approx A_i$

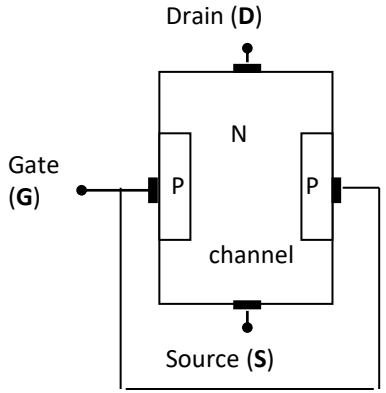
Field Effect Transistors (FETs)

- Like the BJT, **FET is a 3 terminal s-c device**.
- The current through a FET is due to either electrons **or** holes and therefore it is called a **unipolar** device.
- The current flow is controlled by an electric field set up in the device by an externally applied voltage.
- There are 2 main type of FETs:

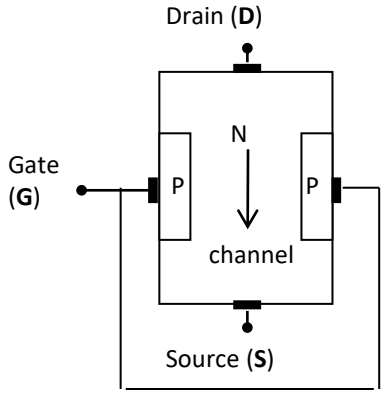
  (a) the **Junction Field Effect Transistor (JFET)** and

  (b) the **Metal-Oxide-Semiconductor FET (MOSFET).**

JFET:



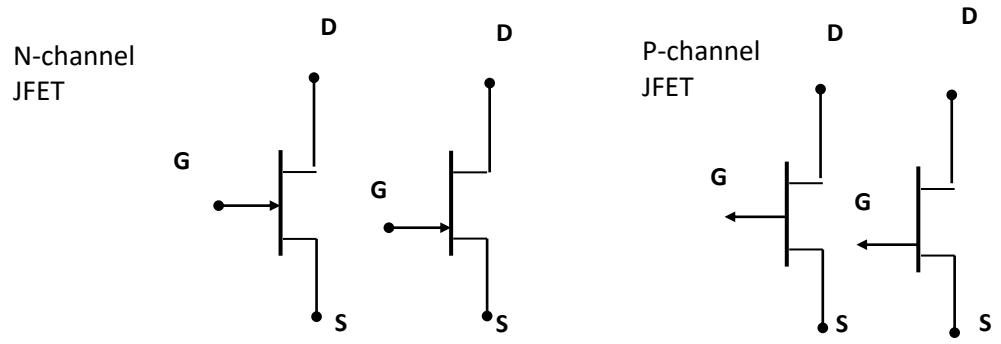
- Consists of a N- type s-c bar with two P- type heavily doped regions diffused on opposite sides of its middle part.
- The two P sides are joined electrically and the common connection between them is called the **Gate (G)**.
- Electrical connections (called ohmic contacts) are made to both ends of the N- type s-c and are taken out in the form of two terminals called **Drain (D)** and **Source (S)**.
- The region of N material between the two P regions is called the **channel**.



- For a N- channel JFET, D is the terminal through which electrons leave the s-c bar and S is the terminal through which electrons enter the s-c.
- Thus conventional current flow is from D to S.
- The voltage applied to G controls the flow of current between D and S (by changing the channel width).
- (For a P channel JFET where current flow is due to holes, N-type heavily doped regions are diffused into a P-type s-c bar).

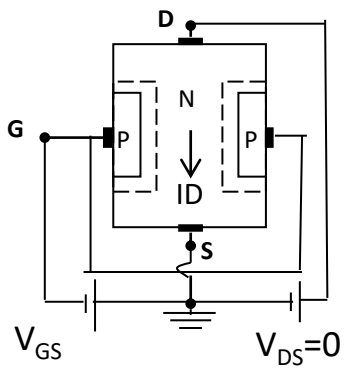
Circuit Symbols for JFET:

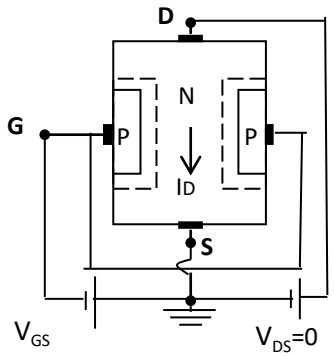
- The symbols showing the G terminal off-center are used as a means of identifying the S: the S is the terminal closest to the G arrow.
- Some JFET are manufactured with D and S interchangeable and the symbols for these devices will have the G arrow in the center.



Formation of depletion regions:

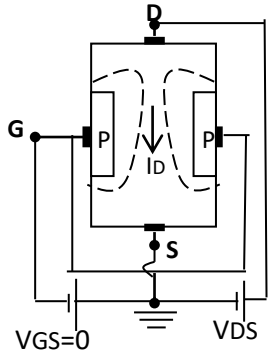
- In the N-channel JFET, the P-type G and N-type channel constitute a PN junction.
- In normal operation an external voltage V_{GS} is applied across G & S and a voltage V_{DS} applied across D & S.
- We first consider the case for when $V_{DS} = 0$.
- V_{GS} is applied so that the PN junctions on each side of the channel are reverse biased.
- Thus G is made –ve with respect to S.
- The reverse bias causes a pair of depletion regions to form in the channel.

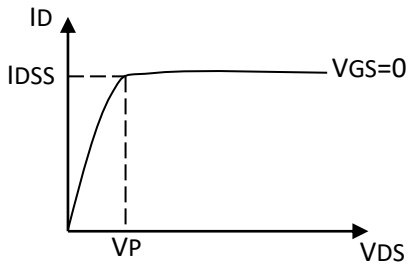


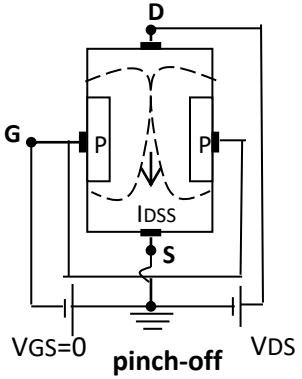


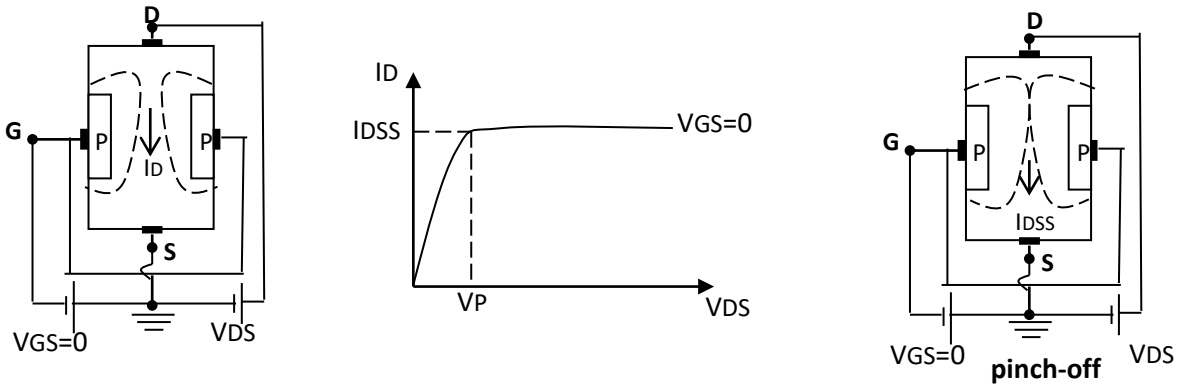
- Since the channel is more lightly doped than G, the depletion regions penetrate more into the N-type channel than into the P-type G.
- The width of the depletion region depends on the magnitude of the reverse bias voltage V_{GS}.
- The figure is for the case when V_{GS} is only a few tenths of a volt, so the depletion regions are relatively narrow.
- As V_{GS} is made more negative, the depletion region expand and the width of the channel decreases.
- The reduction in channel width increases the resistance of the channel and decreases the flow of current denoted as I_D.

- **The reverse bias across the G-S junction can also be achieved by applying a voltage V_{DS} across the D and S terminals.**
- As V_{DS} is increased (for V_{GS}=0), the current I_D increase in direct proportion to it.
- As V_{DS} is increased further, noticeable depletion regions begin to form in the channel.
- The depletion region is broader near the D end of the channel than they are near the S end.

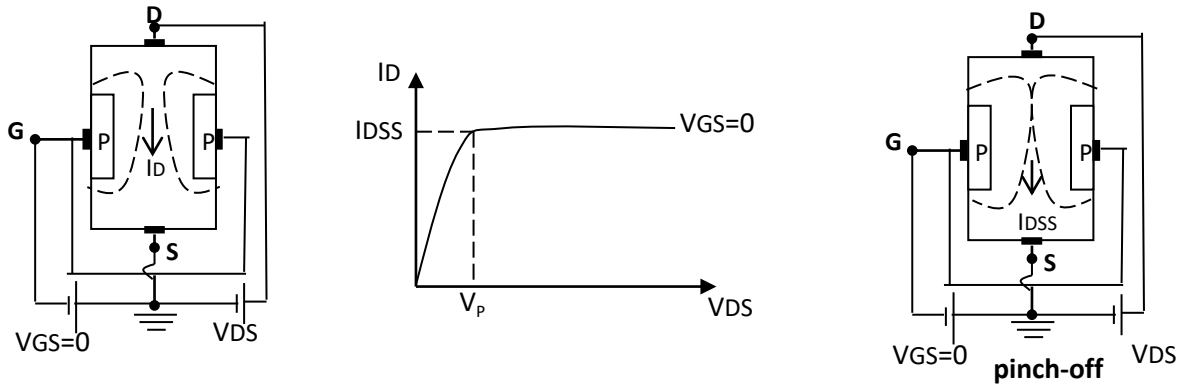








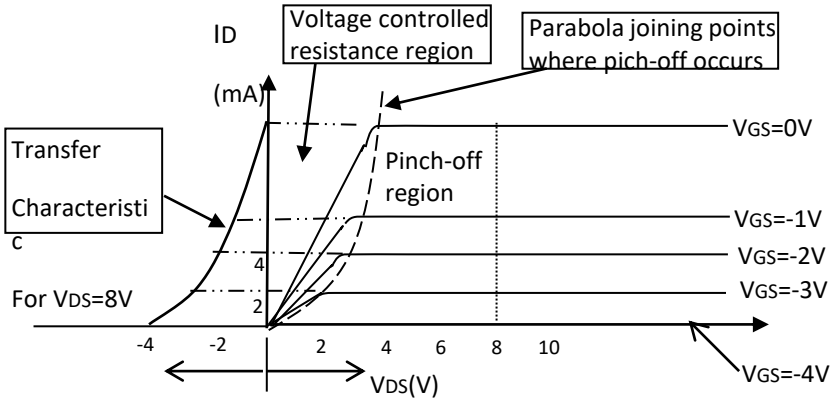
- This is because the current flowing through the channel creates a voltage drop along the length of the channel.
- When V_{DS} is increased further, the depletion region expand and the channel becomes very narrow near D, causing the total resistance of the channel to increase.
- As a consequence the current is no longer directly proportional to V_{DS} and instead the current begins to level off as shown in the middle figure.
- The figure on right shows what happens when V_{DS} is increased to a value large enough to cause the depletion regions to meet at a point near the channel Drain end.
- This condition is called **pinch-off**.

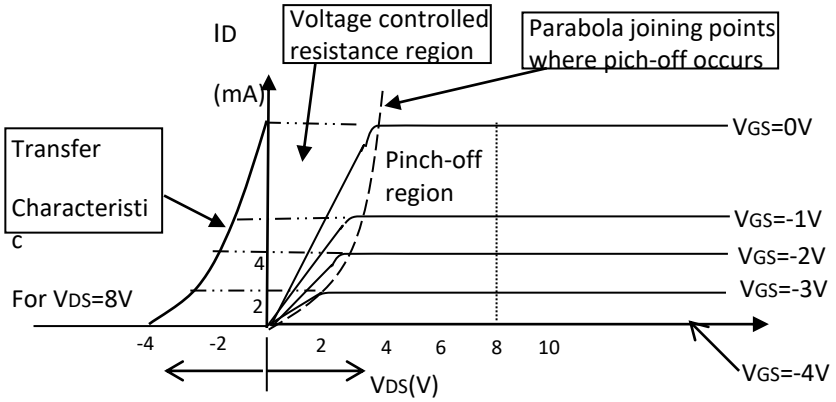


- At the point where pinch-off occurs the value of V_{DS} (the –ve of) is called pinch-off voltage V_P.
- V_P is an important JFET parameter, whose value depend on the doping and the geometry of the device.
- V_P is always –ve for an N channel JFET (and +ve for P channel JFET).
- The middle figure show the current reaches a maximum value at pinch-off and that it remains at that value as V_{DS} is increased beyond V_P.
- This current is called the saturation current and designated I_{DSS}, the drain to source current with the gate shorted.

- We can get other characteristics figures by setting different values for V_{GS} as shown in figure.
- The set of curves are known as the **drain characteristics**.
- The dashed line which is parabolic joins the points on each curve where pinch-off occurs.
- A value of V_{DS} on the parabola is called a saturation voltage $V_{DS}(sat)$.
- At any value of V_{GS}, the corresponding value $V_{DS(sat)}$ is the difference between V_{GS} and V_p:

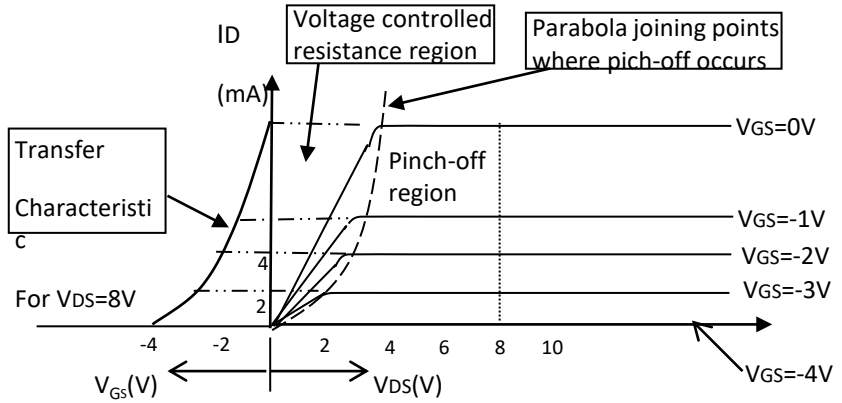
$$V_{DS(sat)} = V_{GS} - V_p$$





- The equation of the parabola is $I_D = I_{DSS}\,[V_{DS(sat)}/V_p]^2$
- The region to the right of the parabola is the pinch-off region (also known as the active or saturation region).
- This is the region in which the JFET is normally operated when used for small-signal amplification.
- The region to the left of the parabola is called the voltage-controlled resistance region, the ohmic region or the triode region.
- In this region the resistance is controlled by V_{GS}.
- The device acts like a voltage-controlled resistor in this region, and there are some practical applications that exploit this.

Transfer Characteristics:

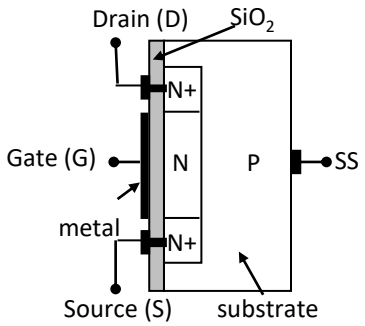


- Of a device is a plot of **output current** versus **input voltage**, for a **fixed value of output voltage**.
- When the input to a JFET is the gate-to-source voltage and the output current is drain current, the transfer characteristic can be derived from the drain characteristics.
- It is only necessary to construct a vertical line on the drain characteristics (a line of constant V_{DS}) and to note the value of I_D at each intersection of the line with a line of constant V_{GS}.
- The values of I_D can then be plotted against the values of V_{GS} to construct the transfer characteristic, as shown in the figure for V_{DS}=8V.
- The choice of this value of V_{DS} means that all points are in the pinch-off region.
- The equation for the transfer characteristic in the pinch-off region is, to a close approximation, $I_D = I_{DSS} (1 - V_{GS}/V_p)^2$

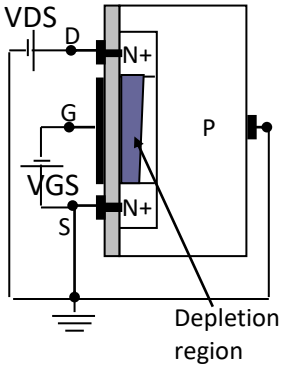
MOSFET: The Metal-Oxide-Semiconductor FET

- Similar to the JFET
- Both have drain, gate and source terminals
- Both are devices whose channel conductivity is controlled by a gate-to-source voltage.
- The main difference between a MOSFET and JFET is the Gate terminal in a MOSFET is insulated from its channel region.
- For this reason, a MOSFET is also called an insulated-gate FET or IGFET.
- **MOSFETs** come in **two types**: the **depletion type** and the **enhancement type**.
- These names are derived from the two different ways that the conductivity of the channel can be altered by variations in V_{GS}.

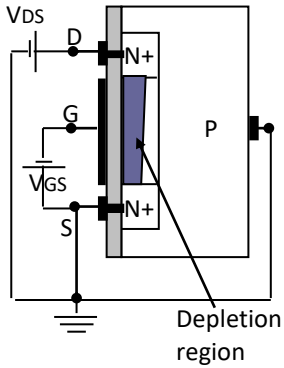
Depletion-Type MOSFETs



- N-channel, depletion type MOSFET.
- A block of high resistance, P type silicon forms a substrate, in which are
- embedded two heavily doped N type wells labeled N+.
- A thin layer of Silicon Dioxide (SiO_2), which is an insulating material, is deposited along the surface.
- Metal contacts penetrate the SiO_2 layer at the two N+ wells and become the drain and source terminals.
- Between the two N+ wells is a more lightly doped region of N material that forms the channel.
- Metal (Al) is deposited on the SiO_2 opposite the channel and becomes the gate terminal.
- Note that the gate is insulated from the channel and that there is no PN junction formed between gate and channel.

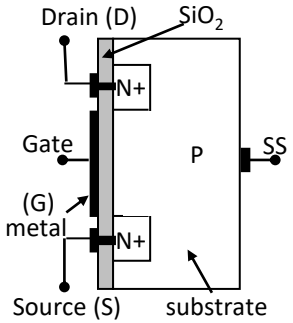


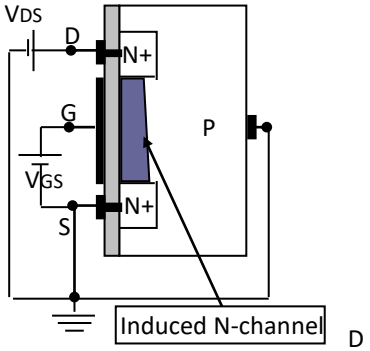
- In normal mode of operation of a depletion-type N-channel MOSFET a voltage V_{DS} is connected between drain and source to make the drain +ve with respect to the source.
- The substrate is usually connected to the source as shown in the figure.
- When the gate is made negative with respect to the source by V_{GS}, the electric field it produces in the channel drives electrons away from a portion of the channel near the SiO_2 layer.
- This portion is thus depleted of carriers and the channel width is narrowed.
- The narrower the channel the greater its resistance and the smaller the current flow from drain to source.



- The device behaves like a N-channel JFET, the main difference being that the channel width is controlled by the action of the electric field rather than by the size of the depletion region of a PN junction.
- Since there is no PN junction V_{GS} can be made +ve without any concern for the consequence of the forward biasing a junction.
- Making V_{GS} +ve attracts more electrons into the channel and increases or enhances its conductivity.
- Thus the gate voltage cane be made both +ve and –ve and the device can operate both in a depletion and enhancement mode.
- There is a PN junction between the N material and the P substrate but this junction is always reverse biased and very little substrate current flows. Thus the substrate has little bearing on the operation of the device.
- The resistance looking into the gate is very large, and of the order of thousands of megaohms.

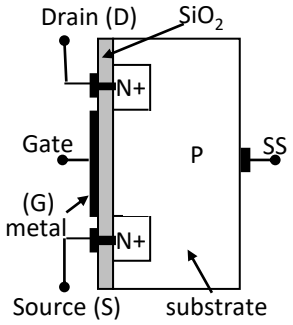
Enhancement –Type MOSFETs

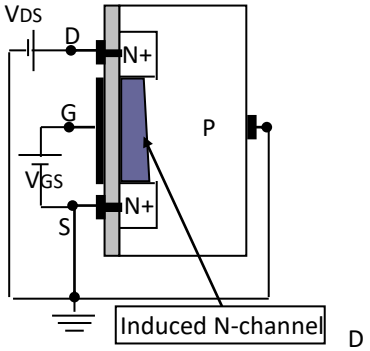




- In the enhancement MOSFET there is no N-type material between the drain and the source (as found in the depletion MOSFET).
- Instead the P-type substrate extends all the way to the SiO_2 layer.
- Figure shows the normal electrical connections between D, G and S.
- As in the depletion MOSFET the substrate is usually connected to the source.
- Note that V_{GS} is connected so that the gate is +ve with respect to the source.
- The +ve gate voltage attracts electrons from the substrate to the region along the insulating layer opposite the gate.
- If the gate is made sufficiently +ve enough electrons will be drawn into that region to convert it into N type material.

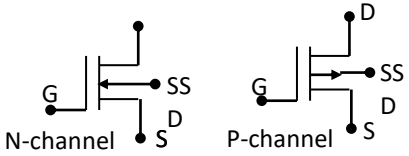
Enhancement –Type MOSFETs



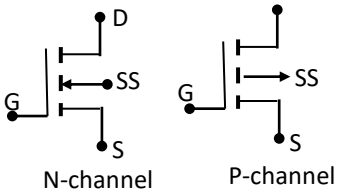


- Thus a N type channel will be formed between drain and source and the P material is said to have been inverted to form an N type channel.
- If the gate is made still more +ve, more electrons will be drawn into the region and the channel will widen making it more conductive.
- Thus making V_{GS} more +ve, enhances the conductivity of the channel and increase the flow of current from drain to source.
- Since electrons are induced into the channel to convert it into N type material the device is also known as an induced N-channel enhancement type MOSFET.

Circuit Symbols:



Depletion-Type



Enhancement-Type

Advantages of N-channel MOSFETs over P-channel

- N-channel MOSFETs have become much more popular than P-channel.
- The main advantage of N-channel MOSFET, over P-channel, is due to the charge carriers in N-channel devices being electrons which have a mobility of about 1300 $cm^2/V.S$ compared to the charge carriers in P-channel devices being holes which have a mobility of a bout 500 $cm^2/V.S$.
- Since the current in a s-c is directly proportional to the mobility, the current in a N-channel MOSFET is more than twice that of a P-channel with the same dimensions.
- The ON resistance of the N-channel MOSFET is 1/3 of that for P-channel.
- This means that in order to achieve the same value of current and ON resistance, the P-channel MOSFET requires 3 times the area of an equivalent N-channel MOSFET.
- Thus electronic circuits using N-channel MOSFETs are much smaller than circuits containing P-channel MOSFETs.