Silicon Valley Expert Witness Group
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Consultant Curriculum Vitae

John H. Givens, Ph.D.

Expertise

- Materials Science
- Microelectronics
- Semiconductor Engineering
- Semiconductor Devices
- Semiconductor Manufacturing
- Microelectronics Packaging

Professional Summary

Dr. John H. Givens is President of Innovative Materials Group, Inc. and CMP Solutions, Ltd. which he founded in 1999 and 2002, respectively. Dr. Givens has focused his career on the innovation and development of materials and processes necessary to enable IC fabrication. His industrial experience includes Vice President of Engineering for Thomas West, Inc., with a focus on CMP pad material development and process implementation, and CMP Section Manager for VLSI Technology with the responsibilities of CMP manufacturability and process strategy. In addition to providing technology necessary for the manufacturing of ASIC's at VLSI, Dr. Givens has developed advanced multilevel interconnects for the production of high-density DRAM's at Micron Technology, Boise, ID and advanced microprocessors at IBM in Burlington, VT. Dr. Givens has authored 11 peer reviewed publications and holds 53 patents concerning advanced semiconductor methodologies. He is a member of engineering technical societies TMS, ASM, AcerS, ECS, MRS, ASME and IEEE. Dr. Givens is an active member of AVS for which he is the instructor for both the CMP Short Course and Cu Interconnect Short Course. And, he is an editor for peer reviewed technical journals JVSTB and Thin Solid Films. Dr. Givens received his B.S. in Metallurgical Engineering, MS in Metallurgical Engineering and Ph.D. in Materials Science & Engineering from the University of Illinois at Urbana – Champaign.

Technology
Chemical Mechanical Polishing; Surface Modification; Colloidal Engineering; Nanomaterials; Nanofabrication; Materials Science & Engineering; Material Characterization Techniques; Thin Film Deposition; Plasma Chemistry; Application Development; Defect Reduction; Yield Enhancement**;** Semiconductor Device Fabrication; Process Integration; Manufacturing Scalability**;** Research & Development; Intellectual Property; Materials/Process Innovation; Technology Transfer

Management
Technical Sales and Marketing; Field Support; Project/Program; Client Relationships; Multi-site Operations; Global Business; Matrix/Module; Cross-Functional Teams; Personnel Development; Recruitment & Retention; Education & Training

Business
Investment Analysis; Competitive Analysis; Market Strategy & Penetration; Direct Sales; Business Start-ups; Planning & Execution; Joint Ventures; Business – IP Strength Assessment & Convergence; Capitalization; Product Life Cycle

Professional History

From:	2014	**Novati Technologies, Inc.**
To:	Present	Austin, TX
	Position:	*Director – Business Development – Wafer Solutions*
	Duties:	International Technical Sales and Representation for Semiconductor Industry; Engineering Field Support; Customer Support; Product Development and Implementation; Business Planning and Execution; Foundry Services; Equipment Access Programs

From:	2002	**CMP Solutions Ltd.**
To:	Present	San Antonio, TX
	Position:	*Founder & President*
	Duties:	Chemical Mechanical Planarization; Applications Engineering; Advanced Process Development; Materials Characterization; IC Fabrication Techniques; Contract Manufacturing

From:	1999	**Innovative Materials Group, Inc.**
To:	Present	San Antonio, TX
	Position:	*Founder & President*
	Duties:	Technical Marketing and Representation for Semiconductor Industry; Engineering Field Support; Customer Support; Product Development and Implementation; Business Planning and Execution; Supplier Industry Manufacturing, Engineering and Business Practices Consultant; CMP and Copper Interconnect Technology Short Course Instructor; Advanced Semiconductor Process Integration; Intellectual Property Assessment & Expert Witness

From:	07/1999	**Thomas West, Inc.**
To:	09/1999	San Antonio, TX
	Position:	*Vice President of Engineering & CTO*

	Duties:	Characterization/Development/Enablement of CMP Consumable – Process Relationships; Definition and Execution of CMP Consumable Strategy; Build-out of CMP Applications Laboratory and Engineering Facility

From:	1998	**VLSI Technology**
To:	1999	San Antonio, TX
	Position:	*Chemical Mechanical Planarization (CMP) Section Manager*
	Duties:	Development of CMP Manufacturing Team; CMP Manufacturing Engineering of CMOS Products; CMP Module Integration for CMOS Applications; BEOL Strategy and Integration

From:	1995	**Micron Technology**
To:	1998	Boise, ID
	Position:	*Senior Engineer and Senior Technical Member*
	Duties:	Advanced Metallization Process Development; Implementation of Damascene Technology; Overall Interconnect Strategy; Patent Strategy

From:	1990	**IBM**
To:	1994	Essex Junction, VT
	Position:	*Advisory Engineer*
	Duties:	Multilevel Metal Process Development/Integration; Selective Dielectric Plasma Etch Process Development; Local Interconnect Process Development/Integration; Implementation of Local Interconnect and MLM in Microelectronics Manufacturing

Litigation Support Experience

Date:	2017	**Covington & Burling (Los Angeles, CA)**
	Case:	Tessera vs. Broadcom
	Project:	Patent consultant
	Status:	Ongoing

Date:	2016	**Kirkland & Ellis (Washington, DC)**
	Case:	Samsung
	Project:	Patent consultant
	Status:	Complete

Date:	2014	**Kirkland & Ellis (San Francisco, CA)**
	Case:	Samsung vs. NVIDIA
	Project:	Patent consultant
	Status:	Complete

Date: 2013 **Kirkland & Ellis (Washington, D.C.)**
Case: Semcon Tech vs. Samsung
Project: Patent litigation, consulting
Status: Complete
Result: Parties settled out of court – settlement favorable to client

Date: 2013 **Kirkland & Ellis (Palo Alto, CA)**
Case: Sony
Project: Patent consultant
Status: Complete

Date: 2012 **Kirkland & Ellis (Washington, D.C.)**
Case: Samsung
Project: Patent consultant
Status: Complete

Date: 2011 **Kirkland & Ellis (Washington, D.C.)**
Case: Infineon vs. Atmel
Project: Patent litigation, consulting
Status: Complete
Result: Patents dropped from case

Date: 2009 **Kirkland & Ellis (Washington, D.C.)**
Case: Spansion vs. Samsung
Project: Patent litigation, testifying witness, ITC matter
Status: Complete
Result: ITC ruled in favor of client

Date: 2009 **Kirkland & Ellis (San Francisco, CA)**
Case: Samsung LED
Project: Patent consultant
Status: Complete

Date: 2008 **Kirkland & Ellis (Washington, D.C.)**
Case: Samsung vs. On Semiconductor
Project: Patent litigation, testifying witness
Status: Complete
Result: Parties settled out of court – settlement favorable to client

Date: 2008 **Kirkland & Ellis (Washington, D.C.)**
Case: Samsung
Project: Patent consultant
Status: Complete

Date:	2005	**Kirkland & Ellis (Washington, D.C.)**
	Case:	Samsung vs. Matsushita
	Project:	Patent litigation, testifying witness
	Status	Complete
	Result:	Parties settled out of court – settlement favorable to client
Date:	2003	**Kirkland & Ellis (New York, N.Y.)**
	Case:	Agere vs. Intersil
	Project:	Patent litigation, testifying witness
	Status:	Complete
	Result:	Parties settled out of court – settlement favorable to client
Date:	2000	**Kirkland & Ellis (Chicago, IL)**
	Case:	Hyundai vs. Infineon
	Project:	Patent litigation, consultant
	Status:	Complete
	Result:	Parties settled out of court – settlement favorable to client

Patents

Patent Number	Issue Date	Title
7510961		Utilization of energy absorbing layer to improve metal flow and fill in a novel interconnect structure
6984874		Semiconductor device with metal fill by treatment of mobility layers including forming a refractory metal nitride using TMEDT
6812139		Method for metal fill by treatment of mobility layers
6790764		Processing methods for providing metal-comprising materials within high aspect ratio openings
6787472		Utilization of disappearing silicon hard mask for fabrication of semiconductor structures
6787447		Semiconductor processing methods of forming integrated circuitry
6784550		Thermal processing of metal alloys for an improved CMP process in integrated circuit fabrication
6781235		Three-level unitary interconnect structure
6774035		Thermal processing of metal alloys for an improved CMP process in integrated circuit fabrication
6689693		Methods for utilization of disappearing silicon hard mask for fabrication of semiconductor structures
6548883		Reduced RC between adjacent substrate wiring lines
6537903		Processing methods for providing metal-comprising materials

	within high aspect ratio openings
6534408	Utilization of disappearing silicon hard mask for fabrication of semiconductor structures
6482735	Method for improved metal fill by treatment of mobility layers
6461963	Utilization of disappearing silicon hard mask for fabrication of semiconductor structures
6404053	Utilization of energy absorbing layer to improve metal flow and fill in a novel interconnect structure
6396119	Reduced RC delay between adjacent substrate wiring lines
6320261	High aspect ratio metallization structures for shallow junction devices, and methods of forming the same
6319813	Semiconductor processing methods of forming integrated circuitry and integrated circuitry constructions
6316360	High aspect ratio metallization structures for shallow junction devices, and methods of forming the same
6316356	Thermal processing of metal alloys for an improved CMP process in integrated circuit fabrication
6309946	Reduced RC delay between adjacent substrate wiring lines
6297156	Method for enhanced filling of high aspect ratio dual damascene structures
6274253	Processing methods for providing metal-comprising materials within high aspect ratio openings
6271593	Method for fabricating conductive components in microelectronic devices and substrate structures therefor
6267852	Method of forming a sputtering apparatus
6200895	Method of forming an electrical connection
6133133	Method for making an electrical contact to a node location and process for forming a conductive line or other circuit component
6114232	Method for making an electrical contact to a node location and process for forming a conductive line or other circuit component
6091148	Electrical connection for a semiconductor structure
6087711	Integrated circuit metallization with superconductor BEOL wiring
6080655	Method for fabricating conductive components in microelectronic devices and substrate structures thereof
6080653	Method for making an electrical contact to a node location and process for forming a conductive line or other circuit component
6060386	Method and apparatus for forming features in holes, trenches and other voids in the manufacturing of microelectronic

	devices
6060385	Method of making an interconnect structure
6057231	Method for improved metal fill by treatment of mobility layers
6054768	Metal fill by treatment of mobility layers
6051121	Deposition chamber with a biased substrate configuration
5985103	Method for improved bottom and side wall coverage of high aspect ratio features
5980657	Alloy for enhanced filling of high aspect ratio dual damascene structures
5956612	Trench/hole fill processes for semiconductor fabrication
5908813	Method making integrated circuit metallization with superconductor BEOL wiring
5894169	Low-leakage borderless contacts to doped regions
5888896	Method for making an electrical contact to a node location and process for forming a conductive line or other circuit component
5835987	Reduced RC delay between adjacent substrate wiring lines
5807467	In situ preclean in a PVD chamber with a biased substrate configuration
5776828	Reduced RC delay between adjacent substrate wiring lines
5726100	Method of forming contact vias and interconnect channels in a dielectric layer stack with a single mask
5658438	Sputter deposition method for improved bottom and side wall coverage of high aspect ratio features
5605862	Process for making low-leakage contacts
5545581	Plug strap process utilizing selective nitride and oxide etches
5268330	Process for improving sheet resistance of an integrated circuit device gate
5055169	Method of making mixed metal oxide coated substrates

Education

Year	College/University	Degree
1990	University of Illinois at Urbana-Champaign	Ph.D., Materials Science
1989	University of Illinois at Urbana-Champaign	MS, Metallurgical Engineering
1985	University of Illinois at Urbana-Champaign	BS, Metallurgical Engineering

Publications

11 Peer Reviewed Publications

Conferences/Short Courses

- 2002 – 2006 Program Committee AVS sponsored International Conference on Microelectronics and Interfaces
- 1999 – 2001 Chairman of AVS sponsored International Conference on Advanced Materials and Processes for Microelectronics
- 1992 – 1998 Chairman of Advanced Materials in Microelectronics Symposium of ICMCTF (AVS Conference)
- 1997 – 2011 AVS Short Course Instructor for "Chemical Mechanical Planarization" and "Copper Technology"
- 1997 – 1999 ICMCTF Proceedings Editor
- 1995 – 2011 Associate Editor for **JVST**
- 1999 – 2011 Guest Editor for **Thin Solid Films**

Professional Associations and Achievements

- Member, AVS
- Member, ASM
- Member, TMS
- Member, ACerS
- Member, MRS
- Member, IEEE
- Member, ECS
- Member, ASME

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