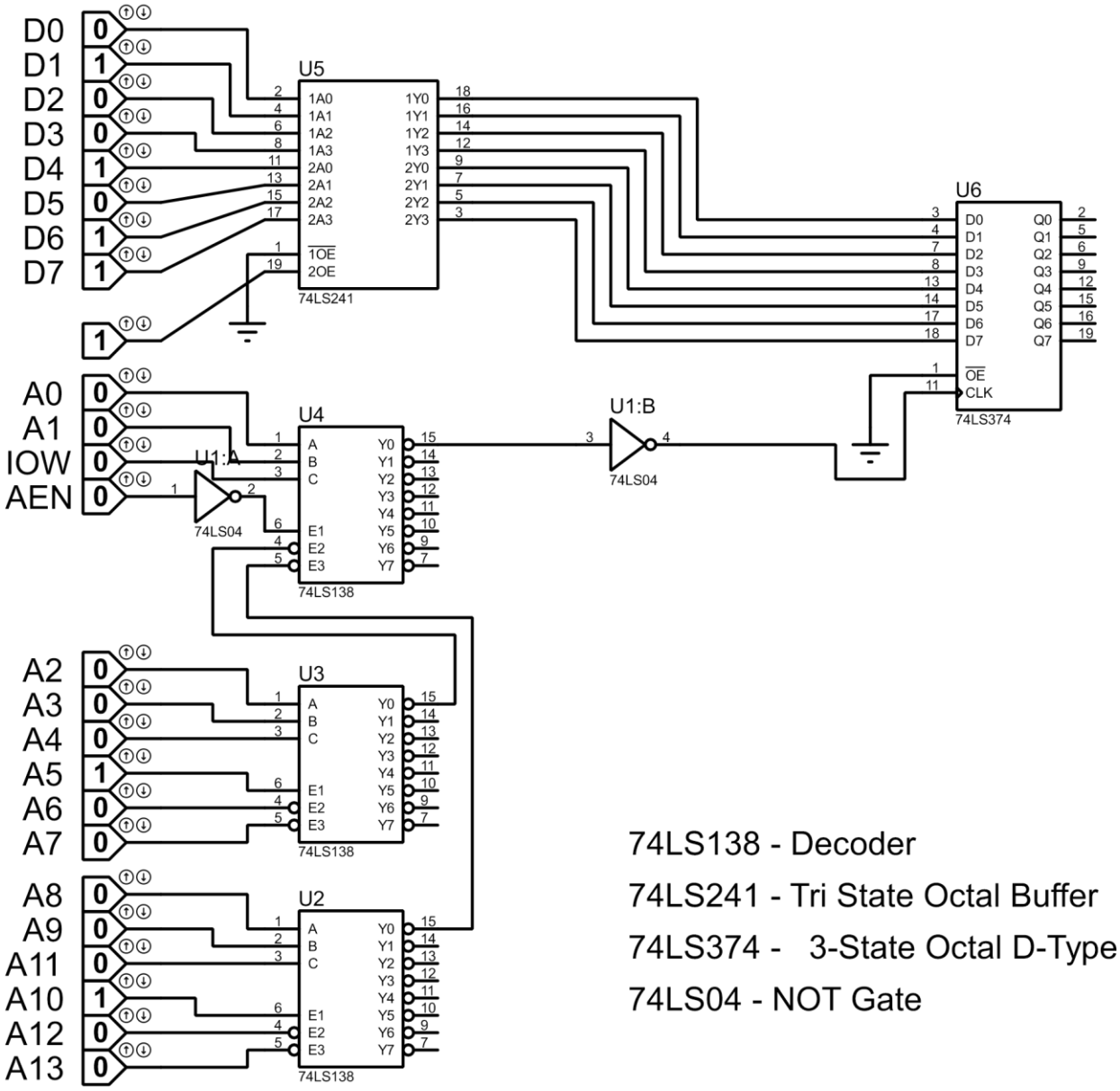
Design of an 8 bit ISA interface of 0 bit input port an 8 bit output port



74LS138 - Decoder

74LS241 - Tri State Octal Buffer

74LS374 - 3-State Octal D-Type Transparent Latches

74LS04 - NOT Gate

a) Assumptions

Assume that buffers getting inputs and giving outputs as the same speed.

c) Briefly explain the importance of using nIOW, nIOR, AENs line in an ISA bus based interface design.

Signal nIOR is an output line indicating an I/O read cycle. IOR goes low when the processor initiates a read from the port address space. This tells the external I/O device being addressed to place its data on the bus.

Similarly, IOW is an output signal indicating an I/O write cycle. IOW goes low when the processor initiates a write to the port address space.This instructs an external I/O device to read data from the system bus.

AEN (Address Enable) is a output signal which allows the IO device to distinguish between processor bus cycles and DMA bus cycles. A high on AEN indicates that a DMA cycle is occurring and that the address, data and control lines are under the control of the DMA controller. Peripheral IO devices that do not have DMA capability should ensure that they only decode address that are generated by the processor (AEN='0') and not a DMA controller. It is low when normal address bus cycle is happening.