Assignment #12

Modeling Delays : timescale and $time

- **Observe delay effect with different timescales :** Write a simple delay-based module and run it with different timescale values.
- **Use different timescale in module and testbench** : Observe the mismatch.
- **Try different units: ns, us, ms :** Write a module and use: -6 for microseconds , -3 for milliseconds, 0 for seconds
- **Print the timescale** of a any module in simulation (try atleast 4 already simulated modules)
- **Nested modules with different timescales** : Create two modules with different timescale values and call $printtimescale from testbench.
- Write a Verilog module that simulates a simple counter circuit. Measure the time elapsed between two specific events during simulation using $time, $stime, and $realtime. Display the results using $display