Assignment-07: Sequential Circuits

1. Design a **Mod-10 synchronous counter**
   - The counter should count from 0 to 9 and then reset back to 0.
   - Use a **4-bit output** to display the count.
   - Include a **synchronous reset** input that resets the counter to 0 when high.
   - The counter should increment on each **rising edge of the clock**
2. Design a **4-bit Ring Counter** using Verilog HDL.
   - The ring counter should shift a single 1 through the register.
   - The counter should reset to the state 0001 on **synchronous reset**.
   - On each **clock edge**, the 1 should shift to the left (circularly)
3. Design a **8-bit Johnson Counter**
   - A Johnson counter feeds the inverted output of the last flip-flop into the input of the first.
   - On **reset**, the counter should initialize to all zeros.
   - On each **clock edge**, the pattern should progress according to Johnson counter behavior.
4. Design a 4-bit synchronous up/down counter using Verilog HDL.
   - Include an input control signal up_down:
     - 1 → count up
     - 0 → count down
   - Use synchronous reset.
5. Design a **4-bit Gray code counter** using Verilog.
   - On each clock pulse, output the next value in the Gray code sequence.
   - Reset should bring the counter back to 0.