Assignment-01 : Data flow modelling

Write Verilog Codes using dataflow model for the following (**Continuous Assignments**)

Basic Logic Gates

- AND Gate
- OR Gate
- XOR Gate
- XNOR Gate
- NAND Gate
- NOR Gate
- NOT Gate

Arithmetic Circuits

- Half Adder
- Full Adder
- Half Subtractor
- Full Subtractor
- 4-bit Adder
- 4-bit Subtractor

Multiplexers & Demultiplexers

- 2-to-1 Multiplexer
- 4-to-1 Multiplexer
- 1-to-2 Demultiplexer
- 1-to-4 Demultiplexer

Decoders & Encoders

- 2-to-4 Decoder
- 3-to-8 Decoder
- 4-to-2 Binary Encoder (Page 35 , Quick Start)
- 4-to-2 Priority Encoder

Parity Circuits

- 4-bit Even Parity Generator
- 4-bit Odd Parity Generator

Comparators

- 2-bit Magnitude Comparator
- 4-bit Magnitude Comparator

Shift and Rotate Circuits

- 4-bit Left Shift
- 4-bit Right Shift

Majority & Other Logic Circuits

- Majority Circuit
- 4-bit XOR-based Comparator
- 4-bit AND-based Comparator

ALU and Miscellaneous

- 4-bit ALU (Add, Sub, AND, OR)