

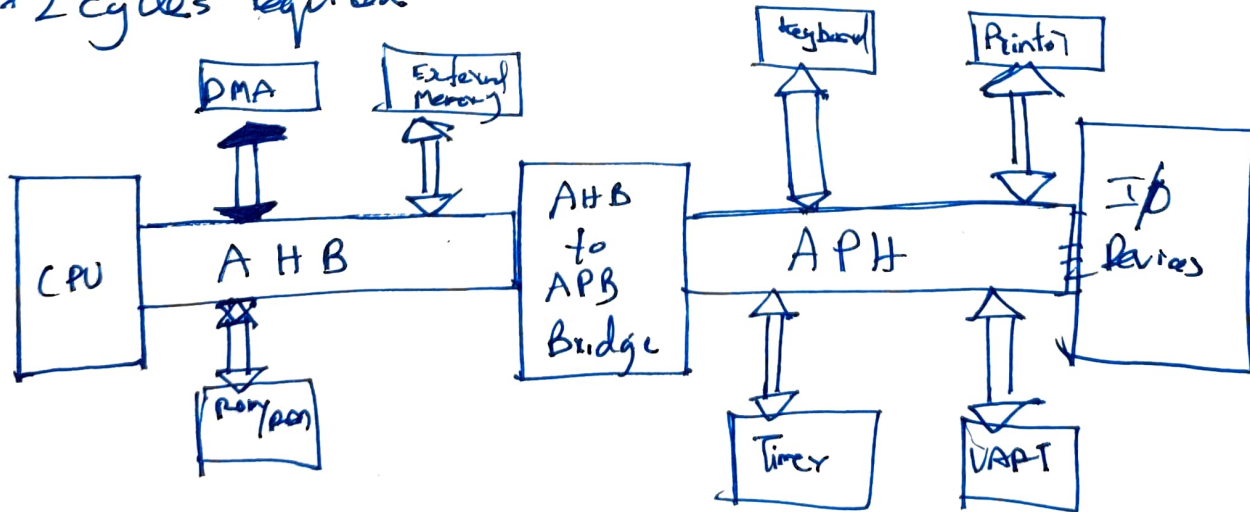
# AMBA: [Advance Microcontroller Bus Architecture]

## • APB: [Advance Peripheral Bus]

- Simple, Low power
- Light-weight
- Commonly used for low-bandwidth peripherals like
  - UART, Timers, GPIO etc

• APB interface is not pipelined, synchronous.

• 2 cycles required for one transfer.



## • Signals associated with APB Interface:

• PCLK - CLK source

• PRESETN - Active Low reset

• PADDR - Address bus (Max - 32 bits) [From M  $\rightarrow$  S]

• PPROT - Protection type

• PSELY - Correspond Slave select [M  $\rightarrow$  S]

• PENABLE - Enables a transfer [M  $\rightarrow$  S]

• PWRITE - Direction of the data [1  $\rightarrow$  Write, 0  $\rightarrow$  Read] [M  $\rightarrow$  S]

• PWDATA - Write Data Bus [8, 16 or 32 bits] [M  $\rightarrow$  S]

• PSTPB - Stroke signal  $\Rightarrow$  Indicates whether the bridge can transfer data to particular byte  
Each bit for byte of data  
[32-bit  $\Rightarrow$  4 Stroke signal bits]  
for or not.

• PREADY - Output signal (Status - Ready for transfer) [S  $\rightarrow$  M]

• PRDATA - output data (Read data bus) [S  $\rightarrow$  M]

• PSLVERR - Output signal - Error signal [S  $\rightarrow$  M]

• PWAKEUP - Indicates any activity associated with APB interface  
 $\hookrightarrow$  Input signal.

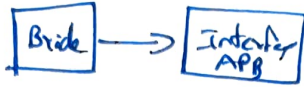
• PAUSER -

• PWUSER -

• PBUSER -

{ User Attributable signal }

## • Transfer in APB Interface:



### • Write Transfer:

#### • Idle phase ( $PSEL = 0$ )

- Setup phase ( $PSEL = 1$ )  $\Rightarrow$ 
  - $PADDR$
  - $PWRITE$
  - $PWDATA$

$\left\{ \text{Must be valid} \right\}$

$\rightarrow$  IF  $PSEL$  is X or Z  $\Rightarrow$   $PSLVERR = 1$

#### • Access phase ( $PENABLE = 1$ ) ( $CPREADY = 1$ )

$\downarrow$   
Read for transfer  
of data from  
bridge to interface.

$\downarrow$   
These values must remain the same during the  
transition from setup to Access phase.

### • Write Transfer with WAIT State:

$\rightarrow$  Same as the earlier phase.

$\rightarrow$  Occurs when  $PENABLE = 1$  &  $CPREADY = 0$  in the access phase,  
it waits till  $CPREADY = 1$ , then the data is transferred.

### • Read Transfer with No WAIT:

- Same idle phase,

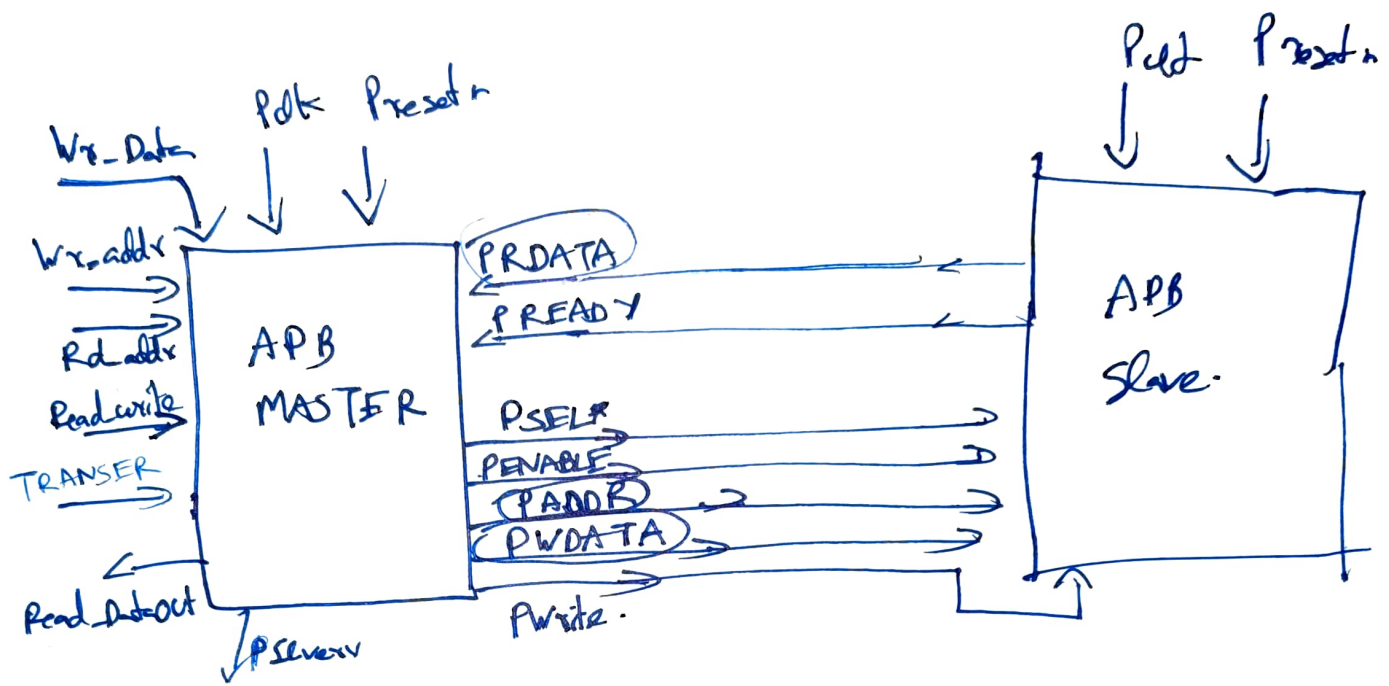
$\rightarrow$  Setup phase  $\rightarrow PSELECT = 1$

$\rightarrow PWRITE = 0$  [Read transfer] [From APB to Bridge]

• Access phase [ $PENABLE = 1$   
 $CPREADY = 1$ , if not wait]

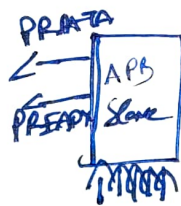
$\rightarrow PWDATA$  will be the output

- 1) Check Read/Write
- 2) Then the address
- 3) From it, get the Slave number.

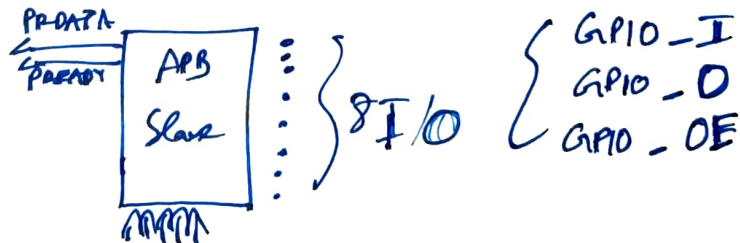


Slaves:

• Memory Unit



• GPIO Pins



• UART

