Prasanna Venkatesh S

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ACADEMIC QUALIFICATION

Bachelor of Technology in Electronics and Communication Engineering **Aug 2021 - June 2025**
Vellore Institute of Technology, Chennai • **CGPA- 9.26 / 10**

AISSCE **April 2019 – June 2021**
Chettinad Vidyashram, Chennai • **Percentage- 87 %**

EXPERIENCE

Maven Silicon - RTL Design Trainee — June – July 2024

- Developed comprehensive expertise in digital electronics, with a focus on combinational and sequential circuits, finite state machines (FSM), and memory design.
- Researched on RISC-V Instruction Set Architecture and contributed to the RTL Design and Development of 3-staged pipeline architecture of the RV32I processor which was later verified using UVM.

EMD Electronics Instrument Ltd. – Project Intern — October - December 2023

- Collaborated on an industrial project to develop a control system for an exhaust fan using the ATSAMD21G18A microcontroller and MPLAB PICkit 4 debugger module.
- Designed a Pulse Width Modulation (PWM) system with 100% accuracy to control fan speed at three different precision levels.

TECHNICAL SKILLS

- **Programming Languages** – Python, Java, C & Embedded C, MATLAB
- **Hardware Description** – Verilog HDL, System Verilog
- **Hardware Simulation:** Intel Quartus Prime, Cadence Virtuoso, LT Spice
- **IDE** - Keil uVision, ARM Keil Studio, Microchip studio, Atmel Start
- **Communication Protocols –** UART, SPI, I_2C, APB

PROJECTS (https://github.com/Prasanna116)

In Memory Computing Architecture using 8T SRAM Memory Cells for ML Applications

VIT, Chennai • November 2024 – March 2025

- A novel 8T SRAM cell architecture is being developed to enable memory arrays to execute logic operations directly within the memory and **64-bit SRAM Array architecture** was designed using **Cadence Virtuoso** and tested using ADE.
- Following the completion of the architectural design, the focus was shift into designing novel computational sensing methods - **Skewed inverter and Multi-Logic Sense Amplifier approach**, then the design was rigorously tested using PVT (Process Voltage Temperature), parametric and Monte-Carlo simulations.

FPGA Implementation and analysis of High-Performance (4,8,16 bit) MAC Unit

VIT, Chennai • August 2024 – December 2024

- Built **RTL designs** of Parallel Prefix adders**(Kogge Stone and Brent Kung adders**) and advance Multiplier algorithms (**Vedic, Dadda and Wallace multipliers**) using Verilog HDL in ModelSim.
- Verified the RTL designs using extensive testbench, synthesized, and evaluated a suite of Multiply-Accumulate (MAC) units by incorporating advanced multiplier architectures with optimized adders, using Intel Quartus Prime on Intel Cyclone V FPGA. Conducted comprehensive PPA (**Performance, Power, Area**) trade-off analysis via to identify the most efficient architecture across 4-bit, 8-bit, and 16-bit datapaths.

RISC-V RV32I Processor Design

Maven Silicon • June 2024 -August 2024

- Designed a robust **RISC-V processor** with careful considerations of architectural design and performance.
- Implemented an efficient **3-staged pipeline architecture** of RV32I using Verilog HDL and synthesized the design using Intel Quartus Prime. Developed the top-level schematic and successfully verified 6 types of RISC V instruction set using **UVM**.

CERTIFICATIONS

- **VLSI Physical Design** NPTEL• 2025
- **Advance Physical Design using OpenLane and SKY130** VLSI System Design (VSD IAT) • 2025
- **Autodesk Eagle: PCB and Hardware design for Beginners** Udemy• 2024
- **VLSI CAD: Part 1** University of Illinois Urbana-Champaign and Coursera • 2023