Introduction to Verilog Programming on FPGA

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Component	Value	Quantity
Breadboard		1
Resistor	≥ 220Ω	1
FPGA	Zedboard	1
Seven Segment Display	Common Anode	1
Jumper Wires		20

TABLE 0

Pin	Segment
JA1	a
JA2	b
JA3	c
JA4	d
JB1	e
JB2	f
JB3	g
Vcc	COM

TABLE 1: Pin Connections

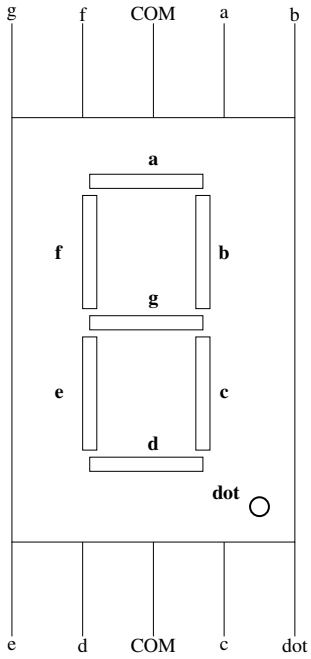

Fig. 1

***Abstract*—This manual provides an introduction to Verilog programming using the Zedboard FPGA. This is done by implementing a decade counter using verilog. The process is likely to be similar for other FPGA boards as well.**

Problem 1. Connect the Zedboard to the seven segment display in Fig. 1 according to Table 1

Problem 2. In your xdc file, make the following changes for the pin connections.

```
set_property PACKAGE_PIN Y9 [
    get_ports {clk}];   # "GCLK"

# ----------------
# JA Pmod - Bank 13
# ----------------
set_property PACKAGE_PIN Y11   [
    get_ports {a}];   # "JA1"
set_property PACKAGE_PIN AA8   [
    get_ports {JA10}];   # "JA10"
set_property PACKAGE_PIN AA11  [
    get_ports {b}];   # "JA2"
set_property PACKAGE_PIN Y10   [
    get_ports {c}];   # "JA3"
set_property PACKAGE_PIN AA9   [
    get_ports {d}];   # "JA4"
set_property PACKAGE_PIN AB11  [
    get_ports {JA7}];   # "JA7"
```

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```
set_property PACKAGE_PIN AB10 [
   get_ports {JA8}];  # "JA8"
set_property PACKAGE_PIN AB9  [
   get_ports {JA9}];  # "JA9"


# ----------------
# JB Pmod - Bank 13
# ----------------
set_property PACKAGE_PIN W12 [
   get_ports {e}];  # "JB1"
set_property PACKAGE_PIN V8 [
   get_ports {JB10}];  # "JB10"
set_property PACKAGE_PIN W11 [
   get_ports {f}];  # "JB2"
set_property PACKAGE_PIN V10 [
   get_ports {g}];  # "JB3"
set_property PACKAGE_PIN W8 [
   get_ports {JB4}];  # "JB4"
set_property PACKAGE_PIN V12 [
   get_ports {JB7}];  # "JB7"
set_property PACKAGE_PIN W10 [
   get_ports {JB8}];  # "JB8"
set_property PACKAGE_PIN V9 [
   get_ports {JB9}];  # "JB9"
```

Problem 3. Run the following program and verify if the number 1 is displayed.

```
`timescale 1ns / 1ps
//////////////////////
// Company:
// Engineer:
//
// Create Date: 31.10.2017
   14:17:14
// Design Name:
// Module Name: sevenseg
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////
```

```
module sevenseg(input wire clk,
   output reg a, output reg b,
   output reg c, output reg d,
   output reg e, output reg f,
   output reg g

    );
    initial
    begin
    a=1;
    b=0;
    c=0;
    d=1;
    e=1;
    f=1;
    g=1;
    end
endmodule
```

Problem 4. Extend the previous program for all numbers between 0-9. Print E on the display if the input is not in this range.

Problem 5. Write a function for implementing a decade counter.

```
`timescale 1ns / 1ps
//////////////////
// Company:
// Engineer:
//
// Create Date: 28.10.2017
   13:08:19
// Design Name:
// Module Name: spidelay
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////
```

```
module display_decoder(
    input  wire clk,

    output reg a,//1-bit variable
       register // a, b, c, d, e, f
       , g are the final outputs.
    output reg b,
    output reg c,
    output reg d,
    output reg e,
    output reg f,
    output reg g
);
reg A;
reg B;
reg C;
reg D;
reg W;
reg X;
reg Y;
reg Z;

  reg [26:0] delay;//for delay of
     1 second

  initial begin
    W=0;
    X=0;
    Y=0;
    Z=0;
    end
  always @(posedge clk) begin

  a=(!D&!C&!B&A)|(!D&C&!B&!A);
  b=(!D&C&!B&A)|(!D&C&B&!A);
  c=(!D&!C&B&!A);
  d=(!D&!C&!B&A)|(!D&C&!B&!A)|(!D&
     C&B&A);
  e=(!D&!C&!B&A)|(!D&!C&B&A)|(!D&C
     &!B&!A)|(!D&C&!B&A)|(!D&C&B&A)
     |(D&!C&!B&A);
  f=(!D&!C&!B&A)|(!D&!C&B&!A)|(!D
     &!C&B&A)|(!D&C&B&A);
  g=(!D&!C&!B&!A)|(!D&!C&!B&A)|(!D
     &C&B&A);

  D=(W&X&Y&!Z)|(!W&!X&!Y&Z);
  C=(Y&!X)|(Y&!W)|(!Y&X&W);
  B=(!W&X)|(!Z&!X&W);
  A=!W;



     delay = delay+1;

       if( delay == 27'
          b101111101011110000100000000
          )begin

                delay = 27'b0;
                                W=A;
                                X=B;
                                Y=C;
                                Z=D;


       end

 end
endmodule
```

Problem 6. In problem 5, verify that the binary number

$$101111101011110000100000000 = 10^8 \qquad (6.1)$$

This is the frequency of the Zedboard clock, which is 100 MHz.