Minor Project

Shift Register Design in Verilog

- **Objective**: Design a 4-bit or 8-bit shift register in Verilog. This project demonstrates data storage and shifting operations, which are fundamental to digital systems like data transfer and manipulation.
- **Features**:
    - Implement shift-left and shift-right operations.
    - Create both parallel-in/serial-out (PISO) and serial-in/parallel-out (SIPO) shift register designs.
    - Simulate the behavior of the shift register using Verilog.
- **Tools**: Verilog for design, ModelSim for simulation.