Major Project

4-bit RISC Processor Design

- **Objective**: Design a basic 4-bit Reduced Instruction Set Computer (RISC) processor in Verilog. Implement essential components such as the ALU, control unit, and simple memory management to simulate a small, functioning CPU.
- **Features**:
    - Implement a 4-bit ALU for arithmetic and logic operations.
    - Design a control unit that decodes instructions.
    - Implement a simple instruction set with load, store, and arithmetic operations.
    - Simulate the processor's functionality to execute programs.
- **Tools**: Verilog for design, ModelSim for simulation.