Minor Project

Multiplexer and Demultiplexer Design

- **Objective**: Design a 2:1 multiplexer (MUX) and a 1:2 demultiplexer (DEMUX) using VHDL. Simulate the functionality of both designs to understand how data selection and routing work.
- **Features**:
    - Design a 2:1 multiplexer (MUX) and implement its functionality.
    - Design a 1:2 demultiplexer (DEMUX) and demonstrate data distribution.
    - Simulate both designs using ModelSim.
- **Tools**: VHDL for design, ModelSim for simulation.