Minor Project

2-bit ALU Design in Verilog

- **Objective**: Design a 2-bit Arithmetic Logic Unit (ALU) in Verilog to perform basic arithmetic and logical operations, such as addition, subtraction, AND, OR, and XOR. This project helps in understanding the fundamental operations of an ALU and digital design using hardware description languages (HDLs).
- **Features**:
    - Implement basic arithmetic operations: addition, subtraction.
    - Implement logical operations: AND, OR, XOR.
    - Control unit to select the operation based on input signals.
    - Simulation of ALU functionality using ModelSim.
- **Tools**: Verilog for designing, ModelSim for simulation.