

GPIO

General Purpose Input Output

GPIO - 0 to 31 pins with input or output (3)

Each general purpose I/O

=> 1 32 bit Register - configuration registers (commonly used)
[GPIO - OTYPER, OSPEEDR, PUPDR, MODAR]

=> 1 32 bit Register - data Register (commonly used)
[GPIO - IDR, ODR]

=> 1 32 bit Register - set/reset register (commonly used)
[GPIO - BSRR]

=> 1 32 bit Register - locking register
[GPIO - LCKR]

=> 1 32 bit Register - Alternative function selection Register
[GPIO - AFRH, AFRL]

GPIO Main features

1) up to 16 I/O under control

2) output states:

Push-pull or open drain + pull-up/down

3) output data from output data Register (GPIOx_ODR)
or peripheral alternative function output

4) speed selection for each I/O

5) Input states:

floating, pull up / down, analog,

6) Input data to Input data Register (GPIO - ODR)
or peripheral (alternative function input)

7) Bit set and reset register (GPIOX - BSRR) for
bitwise write access to GPIOx - ODR

8) Locking Mechanism (GPIOX - LCKR) provided to
freeze the I/O configuration.

9) Analog function

10) Fast toggle capable of changing every two clock
cycles.

GPIO functional description:

Subject to the specific hardware characteristics of each I/O port listed in the datasheet, each port bit of the general purpose I/O (GPIO) ports can be individually configured by software in several modes.

* Input - floating, pull up, pull down

* Analog

* Output:

Open drain with pull-up or pull-down capability.

Push-pull with pull-up or pull-down capability

The purpose of the GPIOX - BSRR register is to allow atomic read / modify access to any of the GPIO registers.

GPIO generally used for

Reading digital signal

Possing interrupts

Generating triggers for external components

GPIO nothing but collection of fixed Number of I/O pins

GPIO PIN:

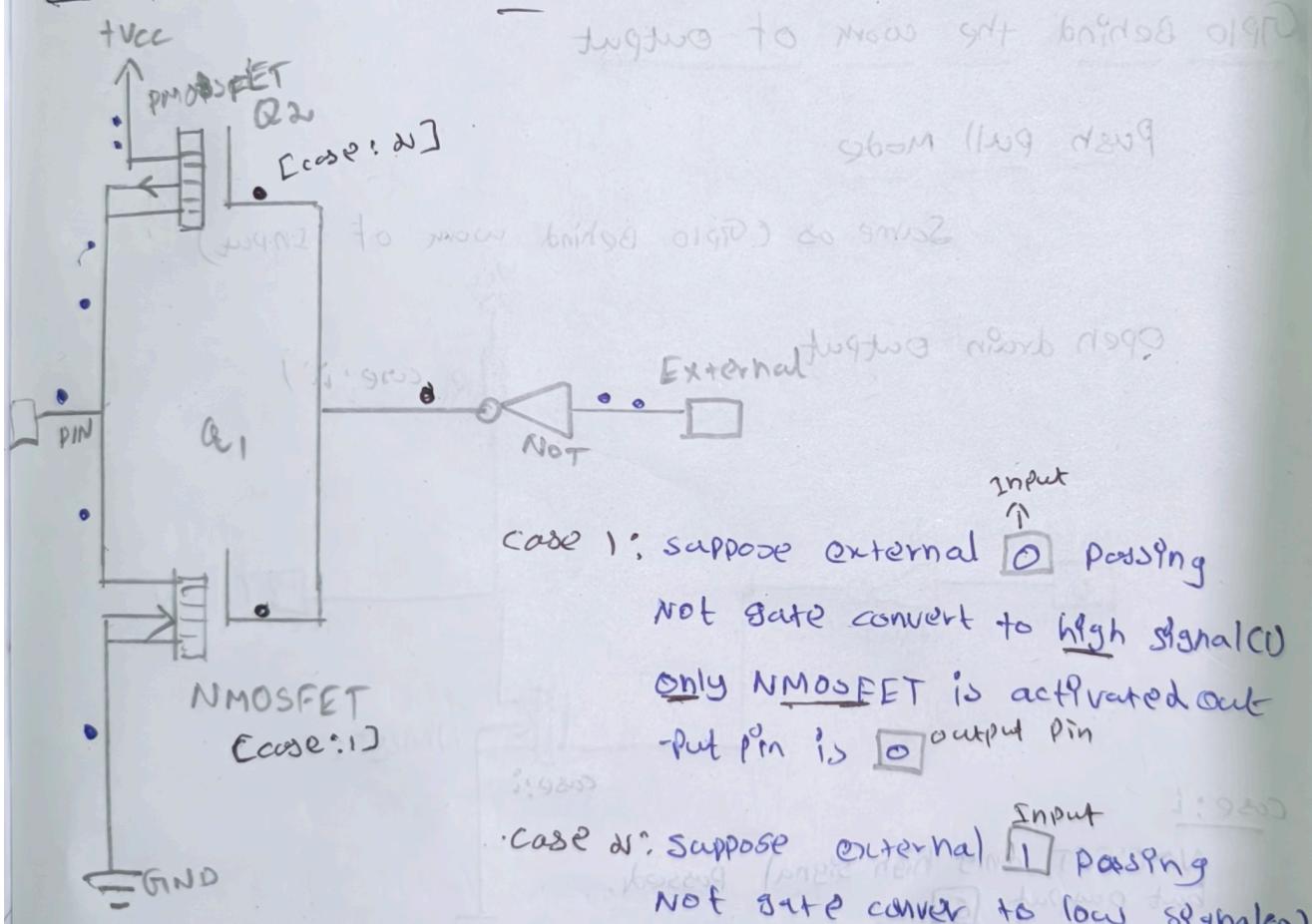
Generic pin whose value consists of one of two voltage setting (high or low)

Behavior can be programmed through software.

GPIO port:

Platform-defined grouping of GPIO pins (standard 16 pins)

GPIO Behind work of input



Case 1: suppose external passing

Not gate convert to high signal()

only NMOSFET is activated out
-Put Pin is output pin

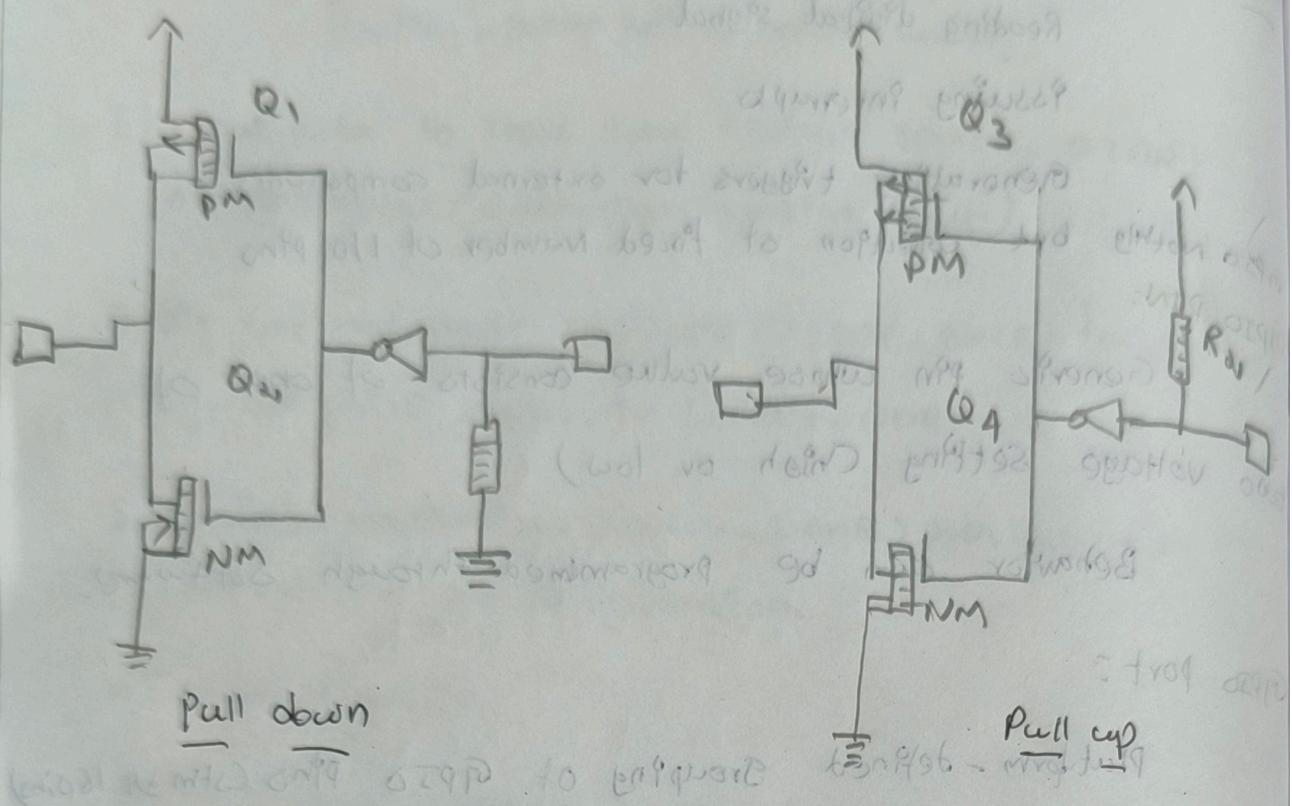
Case 2: suppose external passing

Not gate convert to low signal()

only PMOSFET is activated out
-Put Pin is output pin

∴ This mode keeping a pin floating may lead to leakage current. So avoid the we are using pull up and down.

Input Mode pull up and pull down

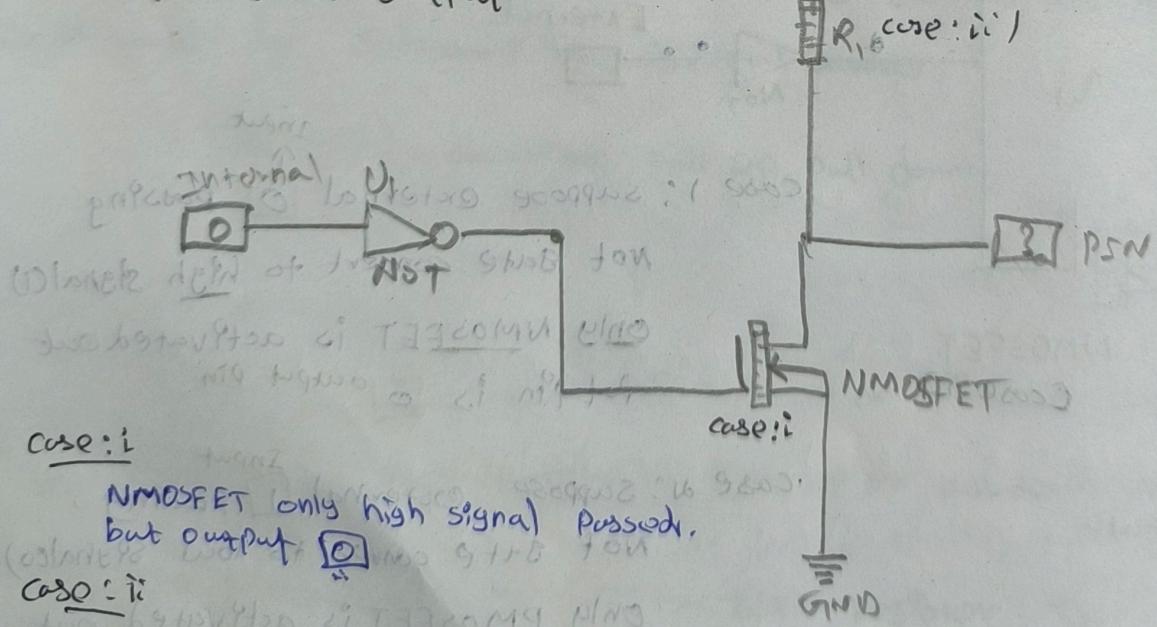


GPIO Behind the work of output

Push pull mode

Same as (GPIO Behind work of input)

Open drain output



case: i

NMOSFET only high signal passed.
(output is low)

case: ii

high signal only passed.

case ii is only low signal pass
and output $\overline{1}$

Graph of first case NMOSFET i_{DS} vs time t
when $t = 0$ $i_{DS} = 0$ when $t = T$ $i_{DS} = I_{DS}$