Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications

Abstract

The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Tools:

- Xilinx 14.5

Language:

Verilog HDL

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