Experiment No: 10

Aim: Make use of NAND and NOR gates to Verify state tables of J – K flip-flop

Learning Objectives: To understand Sequential circuit working

Tools/Software Required: Simulator

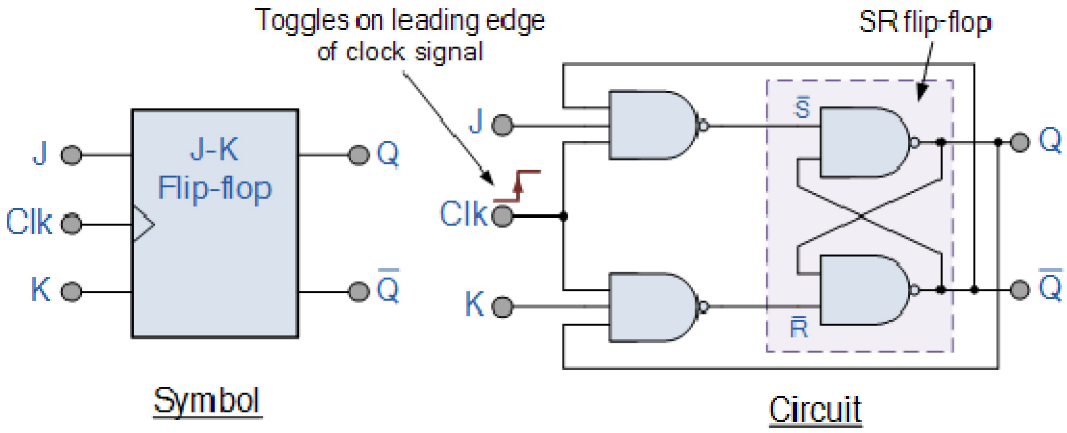
Theory:

Then to overcome these two fundamental design problems with the SR flip-flop design, the JK flip Flop was developed.

This simple JK flip Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The two inputs labelled “J” and “K” are not shortened abbreviated letters of other words, such as “S” for Set and “R” for Reset, but are themselves autonomous letters chosen by its inventor Jack Kilby to distinguish the flip-flop design from other types.

The sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same “Set” and “Reset” inputs. The difference this time is that the “JK flip flop” has no invalid or forbidden input states of the SR Latch even when S and R are both at logic “1”.

The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. The symbol for a JK flip flop is similar to that of an SR Bistable Latch as seen in the previous tutorial except for the addition of a clock input.

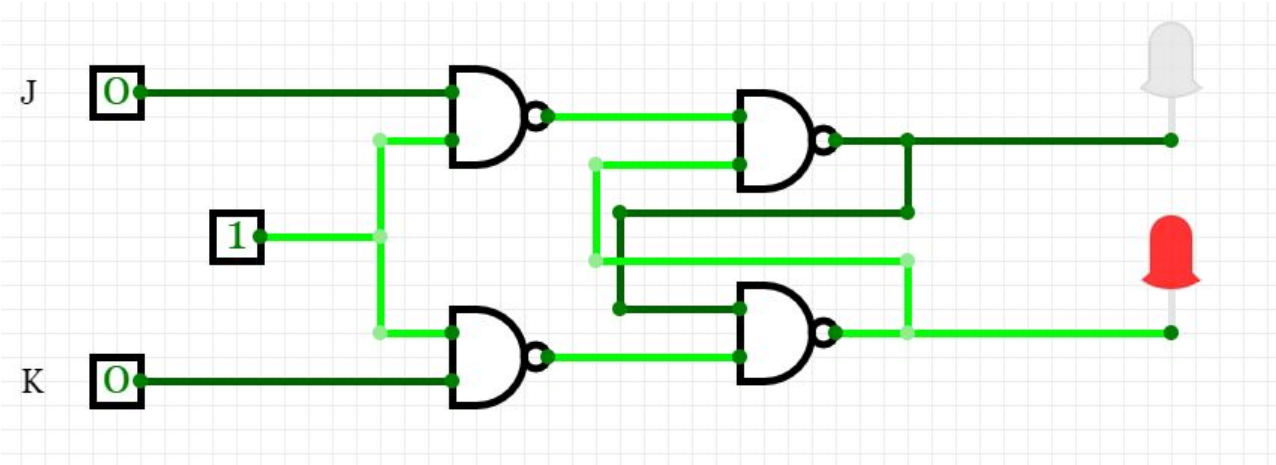


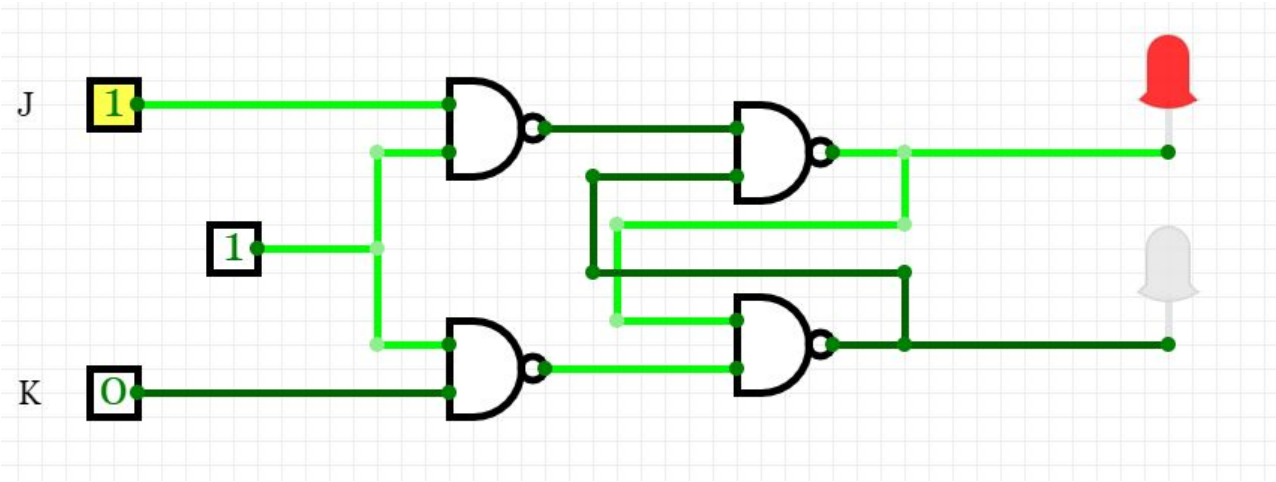
Design J-K Flip Flop using NOR GATE and obtain truth table and functional table for the same .

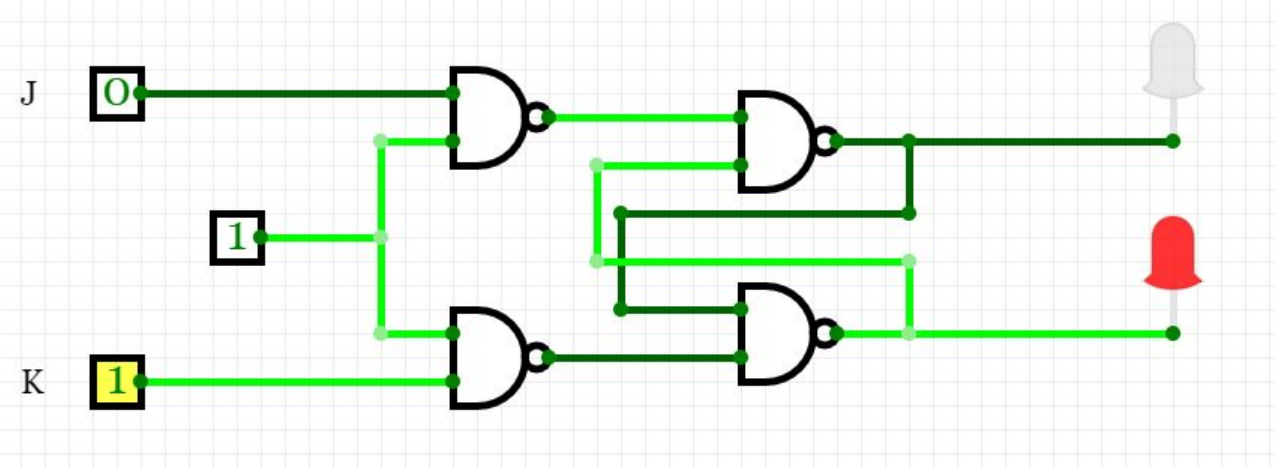
Truth table:

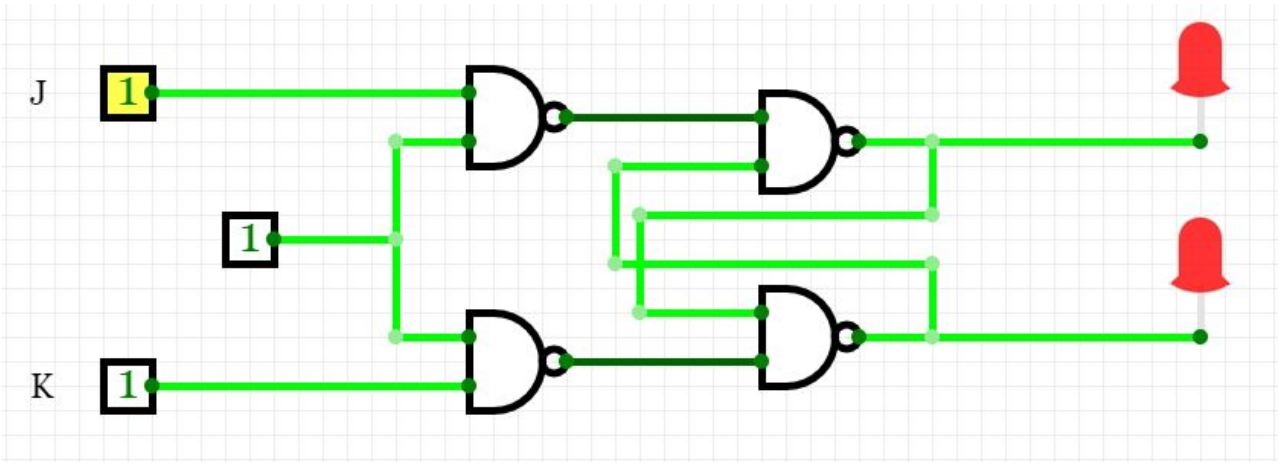
Input		Output		Remark
J	K	Q	Q’	
0	0	q	q’	No change
0	1	0	1	RESET
1	0	1	0	SET
1	1	q’	q	TOGGLE

Implementation:









Conclusion:

Understood what is JK latch and how it is implemented using basic gates. Implemented on simulator and got expected result. Learnt application of latch.