IPA Project Mid Report

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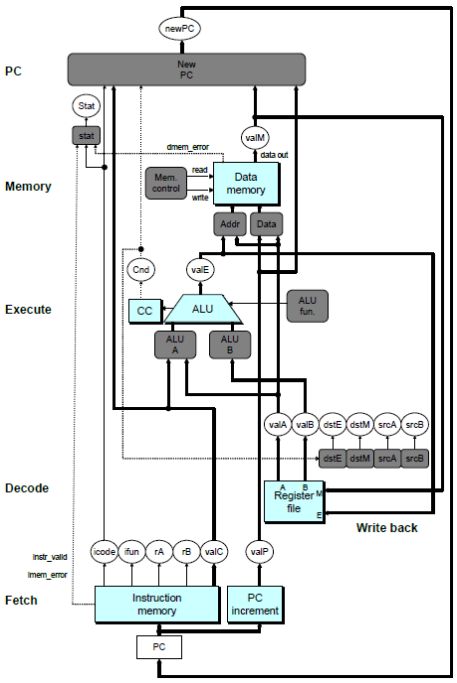
Entire Processor Block :



The figure shown in the side shows the entire block which is used for the design of the entire sequential processor. In this there are different block which are coded and then all of these block will be integrated to a single module which will finally act as the processor which accepts the instruction from the instruction memory and then does the operations.

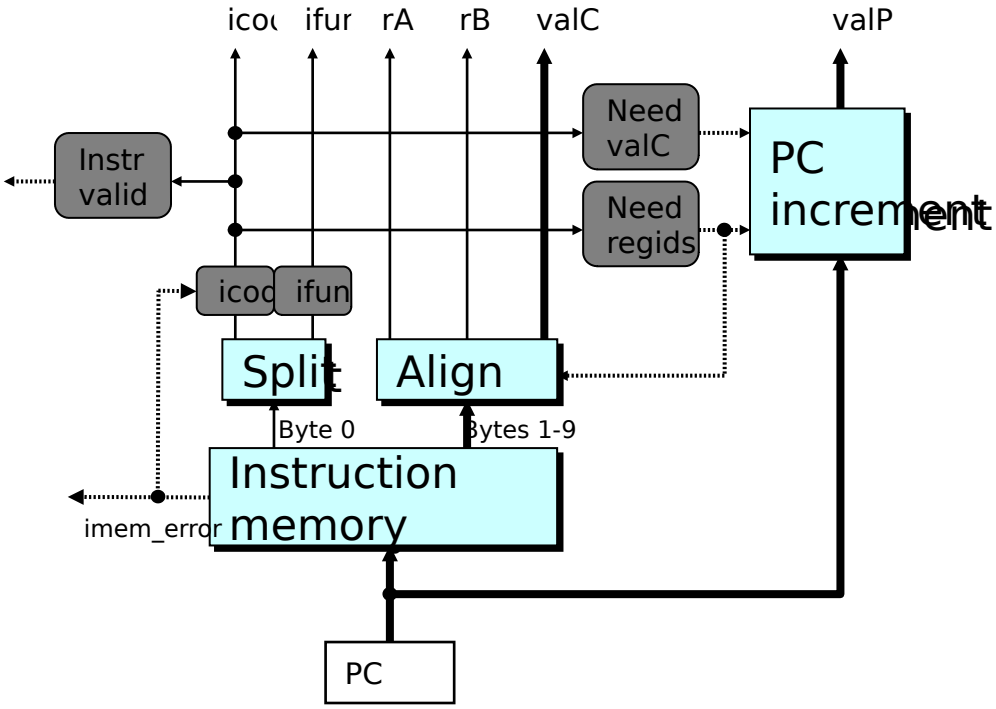
Below is a description of the different modules implemented till now :

1. Instruct_split module

In this the first byte of the instruction is accepted from the instruction memory and then it is split into 2 4 bits the icode and ifun.

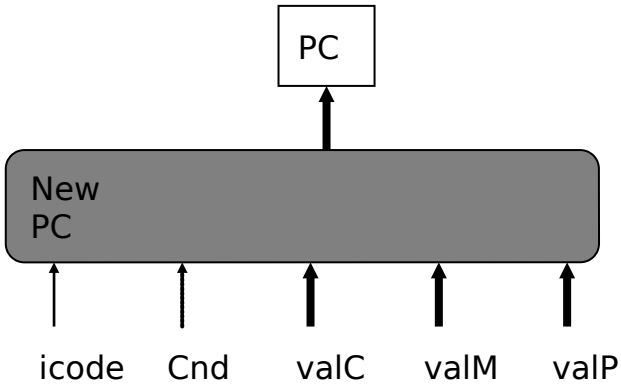
2. Instruct_fetch module

This is used to assign the different values such as instruction validation , memory error and we have used the conditional statements to assign the values of different register values which are not to be used in the case of halt condition and we set the instruction validation in the case it matches with no instruction.



3. update_pc module

In this module we take the value of valC and registers need and then we update pc_val which is the updated value of the program counter.



4. register_file module

This is the implementation of the decode logic which takes the inputs as shown in the figure below and this uses the conditional statements and to assigns valA valB if value is to be taken and when write enable is activated then the values are written into the register file.

5. register_update

This uses a clock as the input and then it takes the input as reset and write enable and updates the value that particular register as according to write enable or reset.