4-Week Internship Project Report

On

DESIGN OF HIGH SPEED PRIME NUMBER DETECTOR

Submitted in the partial fulfillment of the requirements for

the award of the degree of

BACHELOR OF TECHNOLOGY

In

ELECTRONICS AND COMMUNICATION ENGINEERING

By

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UNDER THE GUIDANCE OF

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY

(Autonomous)

Yamnampet (V), Ghatkesar (M), Hyderabad – 501301.

2025-26

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY
(Affiliated to Jawaharlal Nehru Technological University, Hyderabad)
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Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that the Project report entitled "**DESIGN OF HIGH SPEED PRIME NUMBER DETECTOR"** is being submitted by **N.Prashanth ,ROLL NO. 24315A0409** in partial fulfillment of the requirements for the award of Bachelor of Technology Degree in Electronics and Communication Engineering to Sreenidhi Institute of Science and Technology affiliated to Jawaharlal Nehru Technological University, Hyderabad (Telangana). This record is a bonafide work carried out by them under our guidance and supervision. The results embodied in the report have not been submitted to any other University or Institution for the award of any Degree or Diploma.

Internal Guide and

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DECLARATION

I hereby declare that the work described in this project titled "**DESIGN OF HIGH SPEED PRIME NUMBER DETECTOR"** which is being submitted by us in partial fulfillment for the award of Bachelor of Technology in the Department of **Electronics and Communication Engineering,** Sreenidhi Institute Of Science and Technology is the result of investigations carried out by us under the guidance of **Dr. D. Asha Devi, Professor, Department of ECE, Sreenidhi Institute of Science and Technology, Hyderabad.**

No part of the report is copied from books/ journals/ internet and whenever the portion is taken, the same has been duly referred. The report is based on the group project work done entirely by us and not copied from any other source. The work is original and has not been submitted for any Degree/Diploma of this or any other University.

Place: Hyderabad

Date:

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I would like to express our heart-felt gratitude to our parents without whom I would not have been privileged to achieve and fulfill our dreams. We are grateful to our Principal, Dr. T. Ch. Siva Reddy, who most ably run the institution and has had the major hand in enabling me to do our project.

The satisfaction and euphoria that accompany the successful completion of the task would be great but incomplete without the mention of the people who made it possible with their constant guidance and encouragement crowns all the efforts with success. In this context. We would like thank all the other staff members, both teaching and non-teaching, who have extended their timely help and eased our task.

TOKEN OF GRATITUDE TO PARENTS

Signature

N.Prashanth ROLL NO.24315A0409

CONTENTS:

Abstract

The 4-bit prime number detector is a fundamental digital circuit widely used in various logic and signal processing applications. This project demonstrates the design and implementation of a 4-bit prime number detector using basic logic gates in Cadence Virtuoso with gpdk45nm technology. The main objective is to achieve accurate prime number detection, minimal propagation delay, and low power consumption. The design process begins with a truth table and the derivation of a simplified Boolean expression, followed by the creation of a gate-level schematic.

Pre-layout simulations are performed to verify the logic functionality, average power, and propagation delay. The layout is then generated with careful placement and routing to minimize parasitic effects. Post-layout simulations are carried out to validate the circuit's performance against the pre-layout results. DRC and LVS checks are performed to ensure the layout's integrity. The results show that the detector accurately identifies prime numbers from 0 to 15 while exhibiting low propagation delay and power consumption, making it suitable for low-power digital and mixed-signal applications.

keywords:CMOS Digital Design, 4-bit Logic, Prime Number Detector, Logic Gates, Boolean Algebra, Propagation Delay, Power Consumption, Layout Design, DRC, LVS, gpdk45nm, Cadence Virtuoso.

I.INTRODUCTION

1.OVERVIEW OF PRIME NUMBER DETECTOR.

A Prime Number Detector is a fundamental digital circuit designed to identify whether a given binary number represents a prime number. In this project, the focus is on detecting 4-bit prime numbers using combinational logic gates implemented in 45nm CMOS technology. The circuit analyzes a 4-bit binary input (ranging from 0000 to 1111, i.e., 0 to 15 in decimal) and generates a high output (logic '1') if the input number is prime, and a low output (logic '0') otherwise.

The design uses basic logic gates such as AND, OR, NOT, and XOR to realize Boolean expressions derived from truth table analysis. Since the circuit is purely combinational, it does not require any clock or sequential elements, making it simple, fast, and power-efficient. Implementing the design in 45nm technology provides significant advantages such as lower power consumption, higher speed, and reduced area compared to older nodes like 180nm or 90nm. The smaller feature size enables higher integration density, which is crucial for modern VLSI systems where performance and efficiency are key.

This project serves as an excellent example of applying digital logic design principles in the nanometer VLSI domain. It demonstrates the process of schematic design, simulation, and layout implementation in the Cadence Virtuoso environment using the gpdk45nm library. The performance metrics such as propagation delay, power dissipation, and area utilization are analyzed to verify the efficiency of the design.

Prime number detection using logic gates can be extended to cryptographic systems, digital processors, and testing algorithms, where identifying prime numbers plays a critical role. This work highlights the integration of mathematical logic with CMOS technology, showing how theoretical digital concepts can be realized in practical, low-power VLSI circuits.

1 .2 IMPORTANCE OF DIGITAL LOGIC DESIGN IN PRIME DETECTION.

Digital Logic Design plays a vital role in implementing efficient, reliable, and compact hardware systems such as prime number detectors. It forms the foundation of modern digital systems, allowing mathematical and logical operations to be performed accurately using simple logic gates. In the case of a 4-bit prime number detector, Digital Logic Design ensures that prime numbers within the 4-bit range (2, 3, 5, 7, 11, 13) are correctly identified using optimized combinations of logic gates and Boolean expressions.

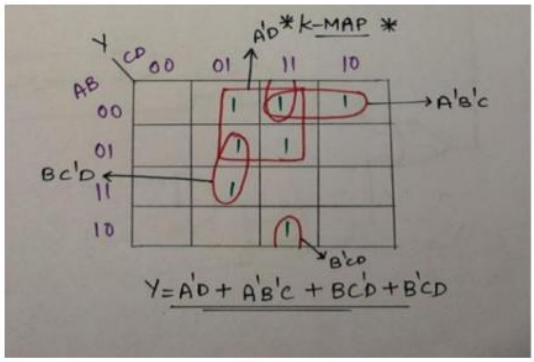


Figure 2: K-Map

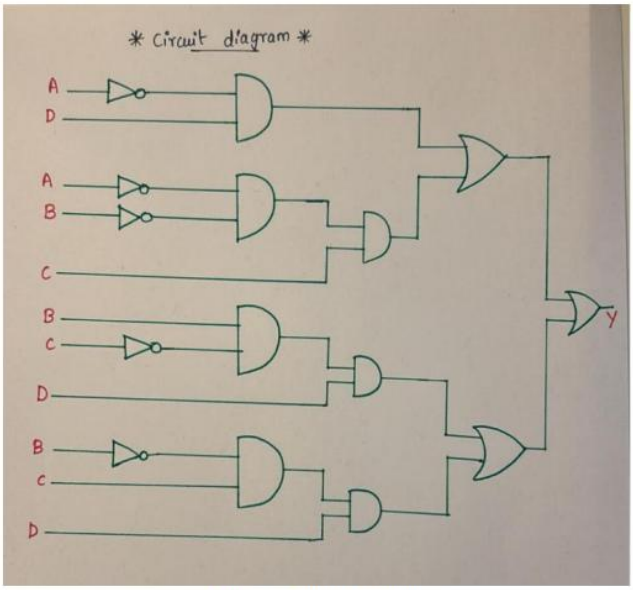


Figure 3: Circuit Diagram

In VLSI implementations like in gpdk45nm technology, Digital Logic Design becomes even more significant due to the requirement for low power, high speed, and area-efficient circuits. The design ensures minimal propagation delay, reduced transistor count, and enhanced performance—making it suitable for integration in arithmetic units, encryption systems, and signal processing hardware. Digital Logic Design serves as the backbone of the Prime Number Detector, enabling a perfect balance between performance, power, and area efficiency. Its structured approach simplifies the complex mathematical task of prime detection into an easily realizable and scalable hardware model — essential for modern digital and VLSI applications.

The importance of Digital Logic Design in prime detection includes the following key aspects:

- **Accuracy in Computation:** Ensures that the circuit precisely identifies only prime numbers within the defined 4-bit range without errors.
- **Optimization of Hardware Resources:** Minimizes the number of logic gates, transistors, and interconnections, resulting in reduced chip area and lower fabrication cost.
- **High Speed and Efficiency:** By implementing efficient logic minimization techniques (like Karnaugh Maps or Boolean simplification), the circuit achieves faster computation of prime numbers.
- **Scalability:** The same design concepts can be extended to detect larger bit-size primes by increasing circuit complexity logically.

- **Low Power Consumption:** In scaled technologies such as 45nm, efficient logic design ensures lower static and dynamic power consumption, suitable for portable and embedded applications.
- **Reliability and Noise Immunity:** The deterministic behavior of digital logic provides reliable operation even under process and temperature variations in modern CMOS technologies.
- **Ease of Implementation in VLSI:** Logic gate-based designs can be directly mapped onto CMOS transistor-level circuits, enabling seamless simulation, synthesis, and layout generation in tools like Cadence Virtuoso.

1.3 APPLICATIONS OF PRIME DETECTION CIRCUITS

Prime detection circuits have a wide range of applications in modern digital systems and VLSI design. They are used in cryptography and data encryption for generating secure keys based on prime numbers, ensuring high security in communication systems. In digital signal processing (DSP) and error detection, prime number detectors help in coding and optimization algorithms. They also find use in test pattern generation, pseudo-random number generators, and hardware accelerators where prime-based computations are required. Implementing these circuits in 45nm CMOS technology enhances speed, reduces power, and supports integration into compact, high-performance digital architectures.

II.LITERATURE SURVEY

2.1 BASIC CONCEPT OF LOGIC GATES AND COMBINATIONAL CIRCUITS.

Logic gates are the fundamental building blocks of all digital circuits. They perform basic logical operations on binary inputs (0s and 1s) to produce a desired output. Common logic gates include AND, OR, NOT, NAND, NOR, XOR, and XNOR, each representing a specific Boolean function. By combining these gates, complex digital functions can be implemented efficiently.

Combinational circuits are formed by interconnecting logic gates such that the output depends only on the present input values, not on any previous state. Examples include adders, multiplexers, decoders, and comparators. In the context of the Prime Number Detector, combinational logic is used to derive optimized Boolean expressions that identify prime numbers among all possible 4-bit inputs.

These circuits are crucial in digital system design, as they offer high speed, reliability, and deterministic behavior. When implemented in VLSI technologies like gpdk45nm, combinational logic ensures low power consumption, reduced delay, and compact layout, making it ideal for arithmetic and signal processing applications.

2.2 LIMITATIONS OF EXISTING LOGIC-BASED PRIME DETECTORS

- Creased gate count results in larger silicon area and higher fabrication cost.
- Complex logic structures cause greater power consumption, reducing circuit efficiency.
- Multiple logic levels introduce higher propagation delay, limiting operating speed.
- Many existing designs are non-optimized, containing redundant or unnecessary logic gates.
- Difficulty in scaling the design for higher bit ranges without extensive redesign.
- Limited flexibility for integration into modern low-power vlsi systems.
- Under deep-submicron technologies (like gpdk45nm), leakage currents and noise issues become significant.
- Reduced supply voltage headroom in modern cmos limits circuit stability and swing.
- Existing circuits often show poor power-performance trade-offs.
- Accuracy of prime detection may degrade due to logic overlap or design inefficiency.
- High dynamic power dissipation occurs due to frequent switching activity.
- Large propagation paths affect circuit timing and synchronization in complex systems.
- Difficulty in optimizing for both speed and area simultaneously in traditional designs.
- Overall, current logic-based prime detectors lack compactness, accuracy, and energy efficiency, demanding improved, optimized architectures for modern applications.

2.3 ADVANTAGES OF PRIME NUMBER DETECTION TECHNIQUES

- ✓ High Accuracy: Prime number detection circuits ensure precise identification of prime numbers within a given bit range using optimized Boolean logic.
- ✓ Fast Operation: Hardware-based prime detection provides quick and real-time results compared to software algorithms.
- ✓ Low Power Consumption: When implemented in advanced CMOS technologies (like gpdk45nm), these circuits consume minimal power, making them suitable for portable and embedded systems.
- ✓ Compact Design: Optimized logic gate arrangements help achieve a smaller silicon area and efficient layout utilization.
- ✓ Scalability: The same logic design concepts can be extended to detect higher-bit prime numbers with slight modifications.
- ✓ Reliability: Digital hardware circuits are highly reliable and produce consistent outputs without requiring calibration.
- ✓ Integration Capability: Prime detection modules can be easily integrated into cryptographic systems, digital processors, and VLSI chips.
- ✓ Speed and Parallelism: Logic-based designs allow parallel processing of bits, improving detection speed and computational efficiency.
- ✓ Reduced Computational Complexity: Eliminates the need for repeated division or algorithmic checks used in software-based detection methods.
- ✓ Application Flexibility: Can be used in encryption, data compression, coding theory, and hardware accelerators for prime-based operations.
- ✓ Enhanced Performance in Modern Technologies: With proper optimization, these circuits achieve high gain, wide operating range, and stable performance under low-voltage conditions.
- ✓ Low Delay: The combinational nature ensures minimal latency between input and output response.
- ✓ Energy Efficiency: Ideal for battery-operated and high-speed systems due to low dynamic power consumption.

III. Methodology

4.1 DESIGN SPECIFICATIONS

The 4-bit Prime Number Detector is designed using gpdk45nm CMOS technology with a supply voltage of 1.8 V, targeting high-performance digital operation. The design aims for accurate detection of all 4-bit prime numbers while maintaining minimal propagation delay to enable real-time computation. Emphasis is placed on low power consumption and compact area utilization, making the circuit suitable for energy-efficient and space-constrained VLSI implementations. The logic is optimized to reduce gate count and redundancy, ensuring both speed and reliability. Additionally, the design provides high noise immunity and stability under process and temperature variations. The architecture is also scalable, allowing extension for higher-bit prime detection in future applications. These specifications collectively ensure a robust, fast, and area-efficient prime number detection circuit suitable for integration into modern cryptographic, DSP, and digital system applications.

The project was implemented using Cadence Virtuoso and followed these steps:

i.Library Creation:

A new library named Primenumber.New library(Prime number) was created and attached to the 45nm technology file (gpdk045).

ii.Schematic Design:

A standard priority encoder circuit was constructed using logic gates. The design ensures that the highest-order active input is given priority, and its corresponding binary code is generated as the output. The schematic was validated using the Check and Save feature in Cadence.

iii.Symbol Creation:

The schematic was converted into a symbol to enable reuse in the test-bench.

iV.Test-bench Design: Pulse voltage sources (v pulse) were added to simulate encoder inputs. Supply voltages (vdd and gnd) were included, along with necessary test conditions to verify the encoder outputs

V.Simulation Setup:

Pulse voltage sources (v pulse) were added to simulate encoder inputs. Supply voltages (vdd and gnd) were included, along with necessary test conditions to verify the encoder outputs

Vi.Layout Design:

The layout editor was used to place transistors and route connections. DRC and LVS checks were carried out to ensure compliance and correctness

Vii.Post-Layout Simulation:

Parasitics were extracted using Assura DRC, and the design was validated using post-layout simulations. Performance parameters such as delay and leakage currents were also measured.

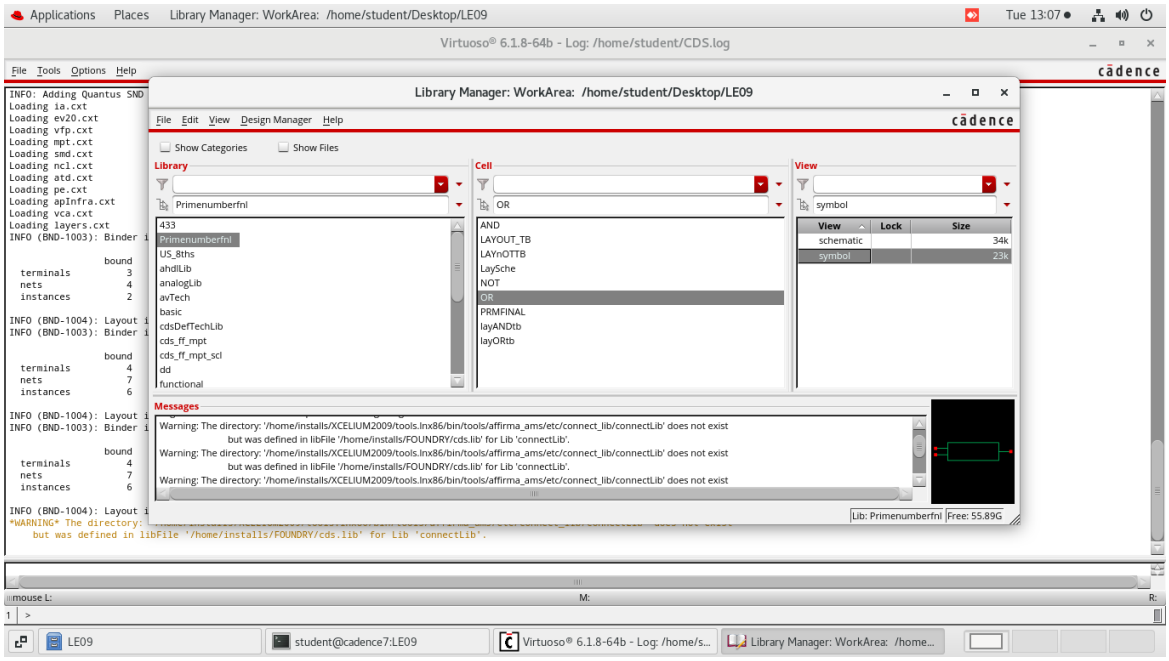


Figure 1 : Library manager

IV.IMPLEMENTATION

4.1 SCHEMATIC IMPLEMENTATION

In the schematic design phase of the 4-bit Prime Number Detector, the basic logic gates such as Inverter (NOT gate), AND gate, and OR gate were first designed using gpdk45nm CMOS technology. These gates serve as the fundamental building blocks for implementing the required combinational logic used to identify prime numbers. Each gate was designed and simulated at the transistor level to verify correct logic functionality, proper voltage levels, and stable operation under the 1.8 V supply.

Inverter (NOT Gate):

The inverter produces an output that is the logical complement of its input. It consists of a PMOS and an NMOS transistor connected in a complementary arrangement. When the input is logic '1', the NMOS conducts and pulls the output to logic '0'; when the input is logic '0', the PMOS conducts and drives the output to logic '1'. This gate is essential for generating complementary signals required in complex logic circuits.

Truth Table:

Input (A)	Output (Y = NOT A)
0	1
1	0

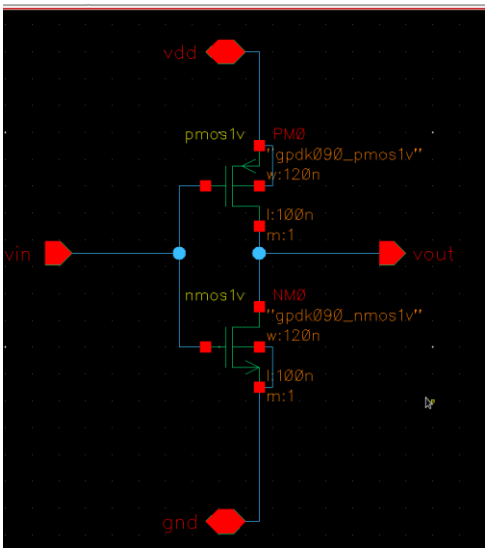


Figure 2 – INVERTER

AND Gate:

The AND gate outputs a logic ‘1’ only when all inputs are logic ‘1’. It can be constructed using series-connected NMOS transistors in the pull-down network and parallel PMOS transistors in the pull-up network. In the 45nm design, transistor sizing is optimized for balanced rise and fall times. The AND gate plays a critical role in detecting specific bit combinations corresponding to prime numbers in the circuit**.**

Truth Table:

A	B	Output (Y =A · B)
0	0	0
0	1	0
1	0	0
1	1	1

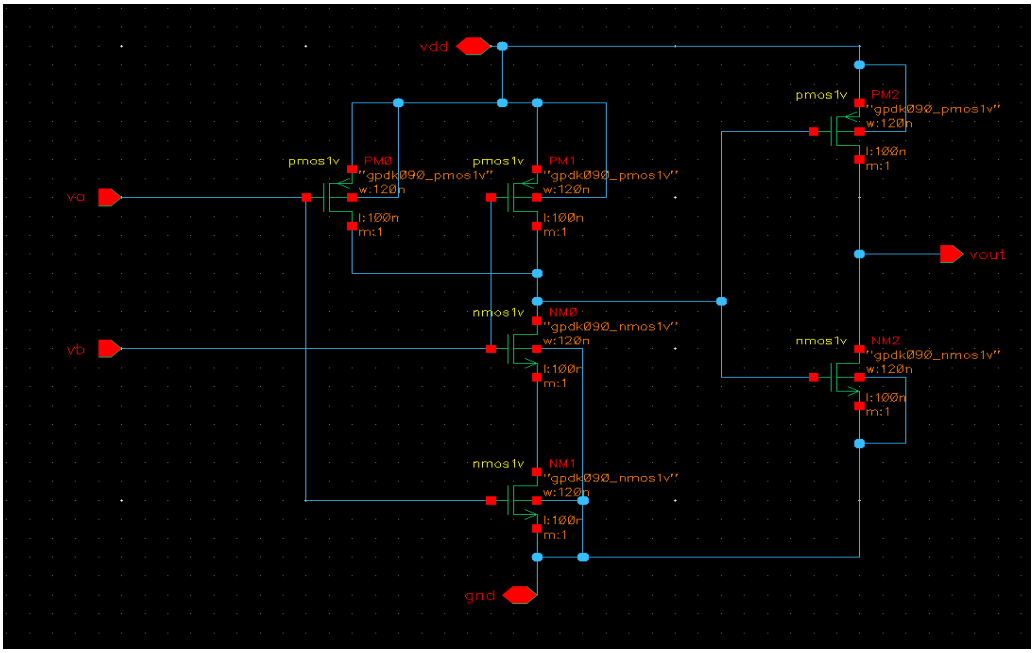


Figure 3 : AND

OR Gate:

The OR gate produces a logic ‘1’ when any one or both inputs are logic ‘1’. It is implemented using parallel NMOS transistors in the pull-down network and series PMOS transistors in the pull-up network. This configuration ensures that the output goes high whenever at least one input is high. In the prime detector circuit, the OR gate helps combine multiple logic conditions to identify the correct prime number outputs.

Truth Table:

A	B	Output (Y = A + B)
0	0	0
0	1	1
1	0	1
1	1	1

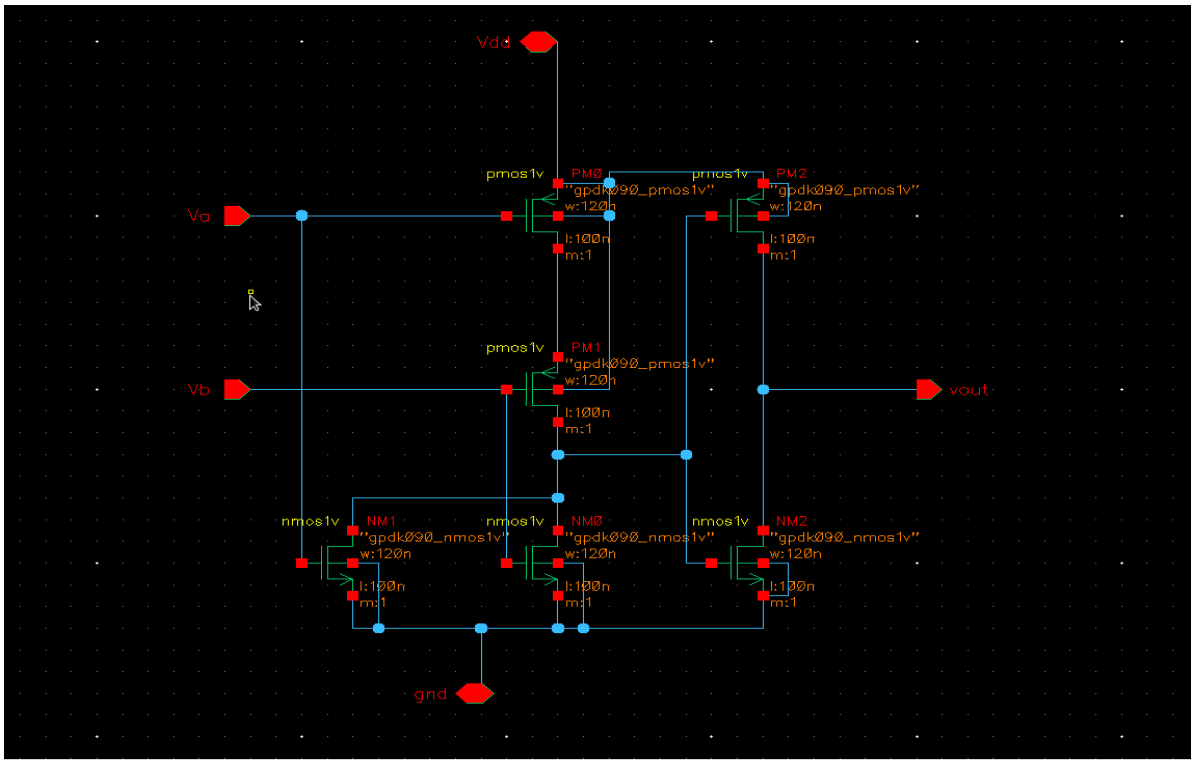


Figure 4 : OR

Prime-Number Schematic :

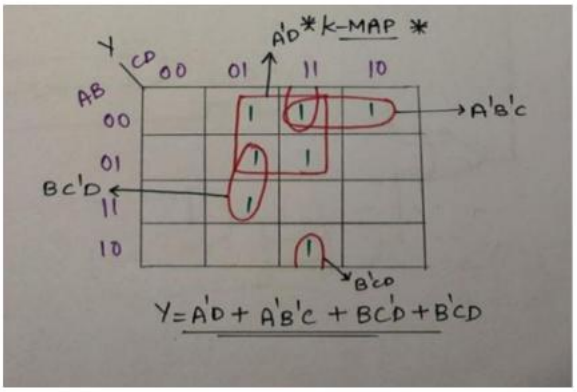


Figure 2: K-Map

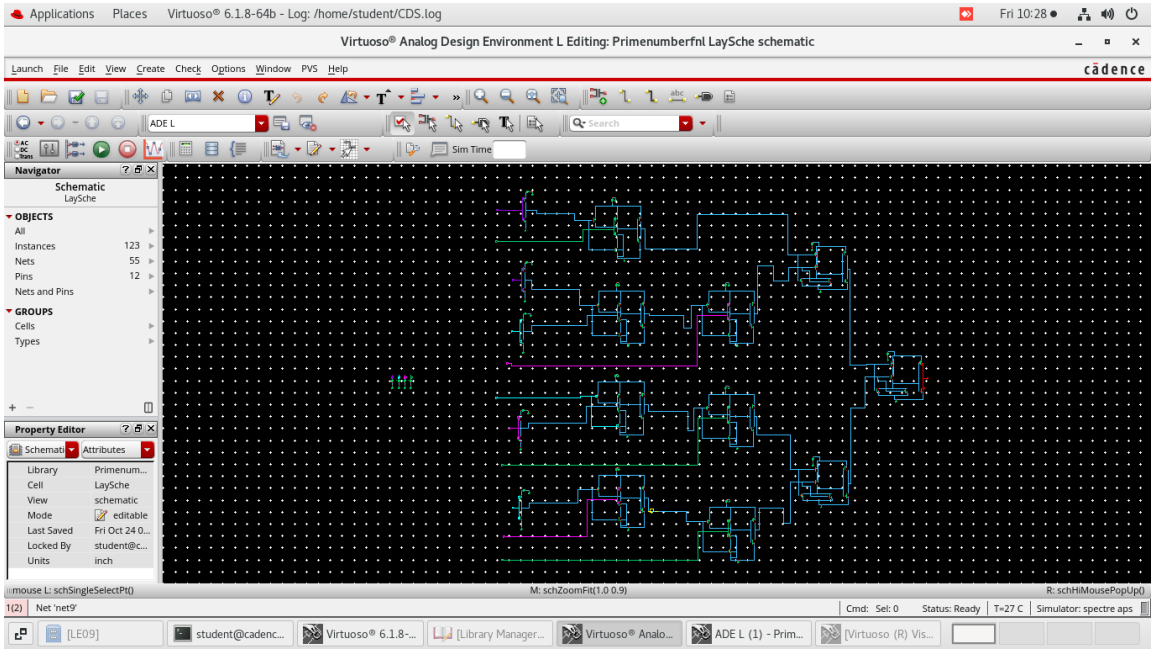


Figure 5 : Schematic

Symbols Schematic of Prime Number :

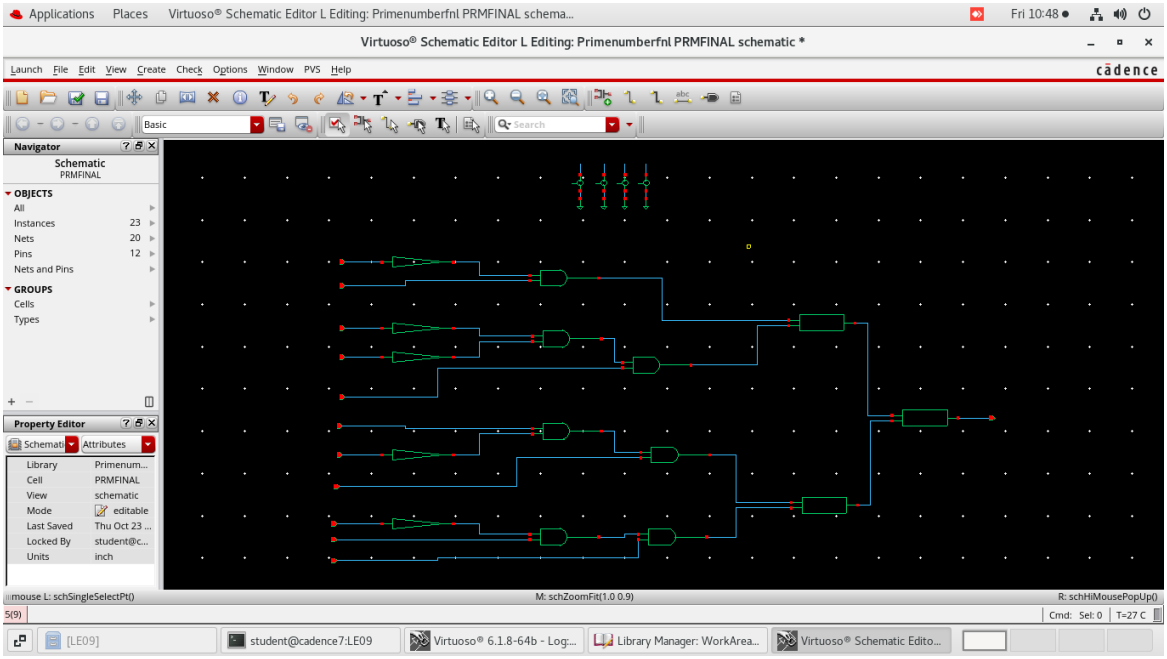


Figure 6 : Schematic with Symbols

4.2 DESIGN PARAMETERS

The prime number detector circuit is powered by a DC supply voltage (Vdc) of 1.8 V. Four pulse inputs, labeled A, B, C, and D, are applied to the circuit to represent binary data for testing and detection purposes. Each pulse source is configured with V1 = 0 V and V2 = 1 V. The input signals operate with time periods of 8 ns, 4 ns, 2 ns, and 1 ns, respectively. Corresponding pulse widths are 4 ns, 2 ns, 1 ns, and 0.5 ns, ensuring a 50% duty cycle across all input conditions.

V0 pulse:

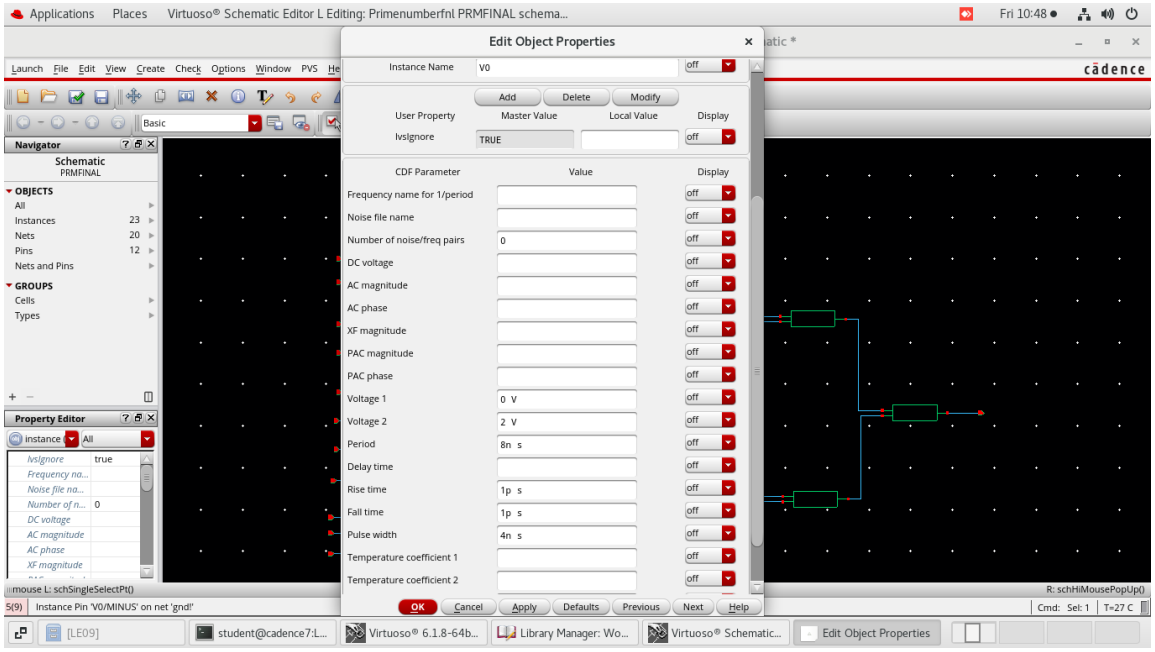


Figure 7 : v0 pulse

V1 pulse:

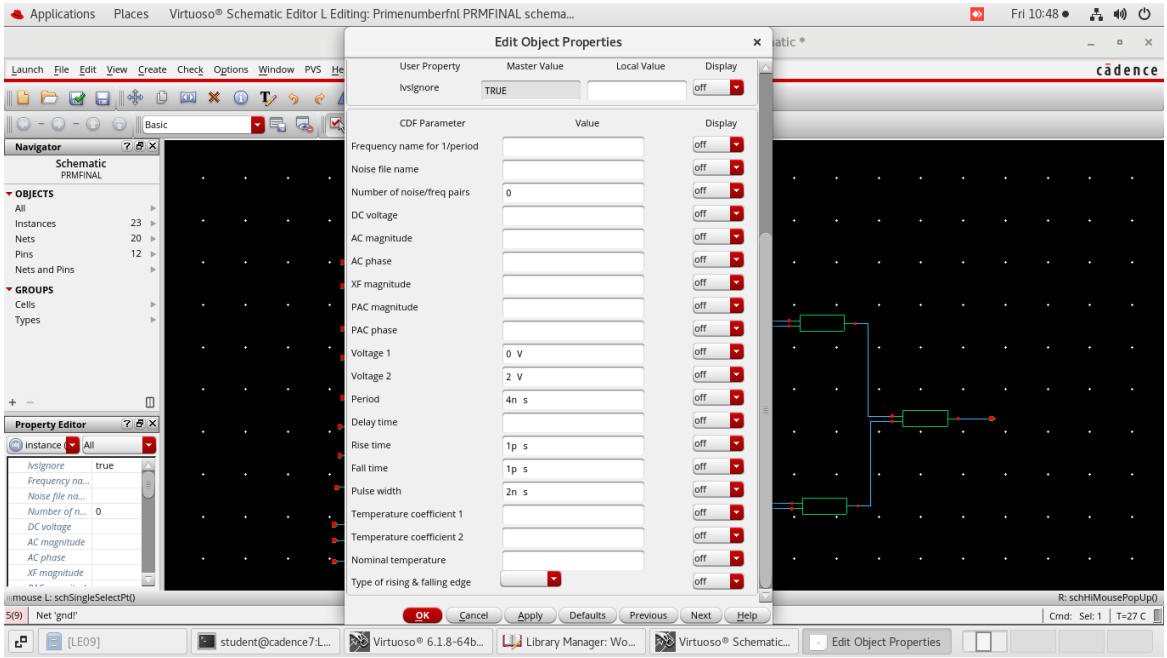


Figure 8 : v1 pulse

V2 pulse :

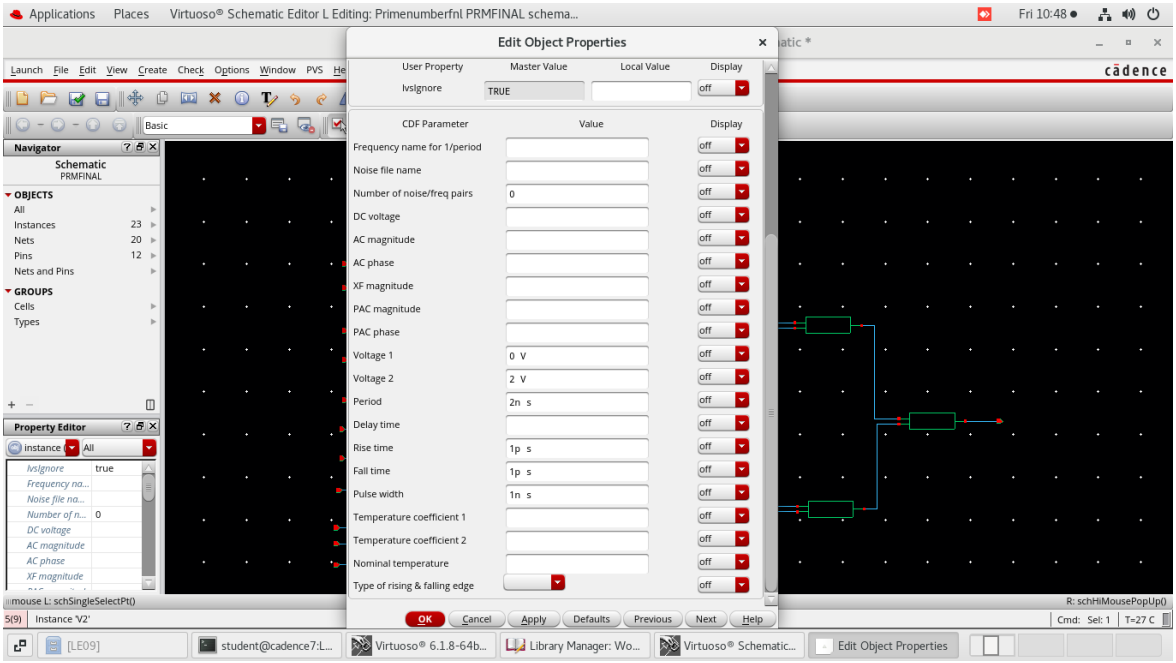


Figure 9 : v2 pulse

V3 pulse:

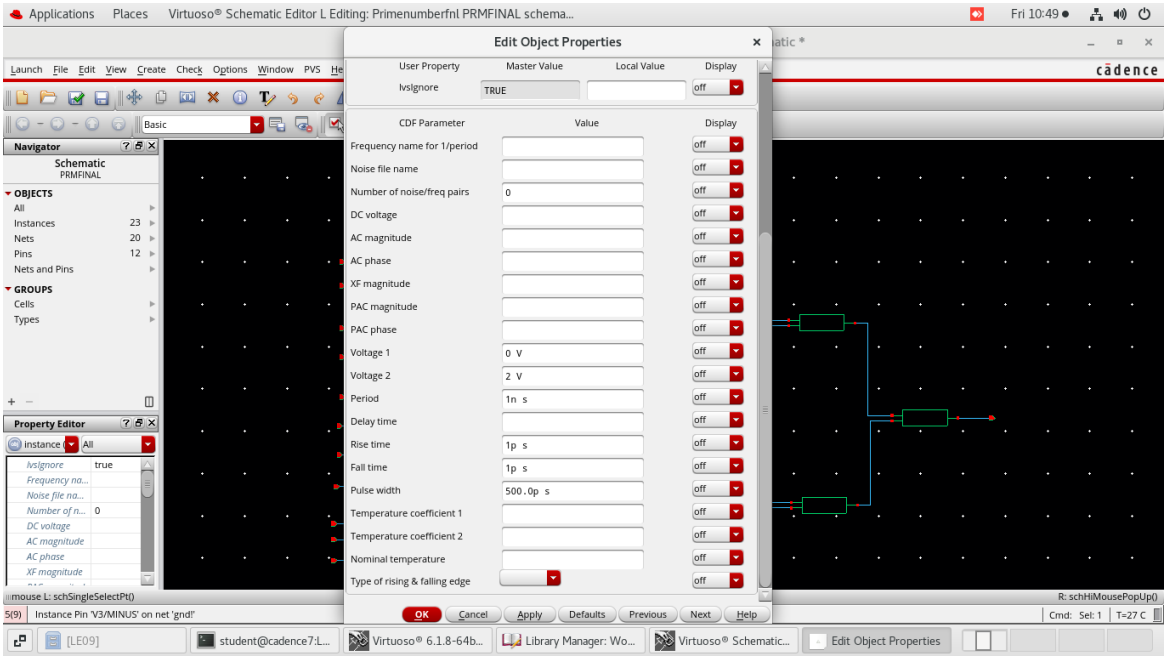


Figure 10 : v3 pulse

4.3 SIMULATION :

Transient analysis confirmed correct functionality of the Prime Number detector. The Spectral simulator in ADE-L was used to configure transient and DC analysis. Signals were plotted to measure functionality and working of PrimeNumber Detector.

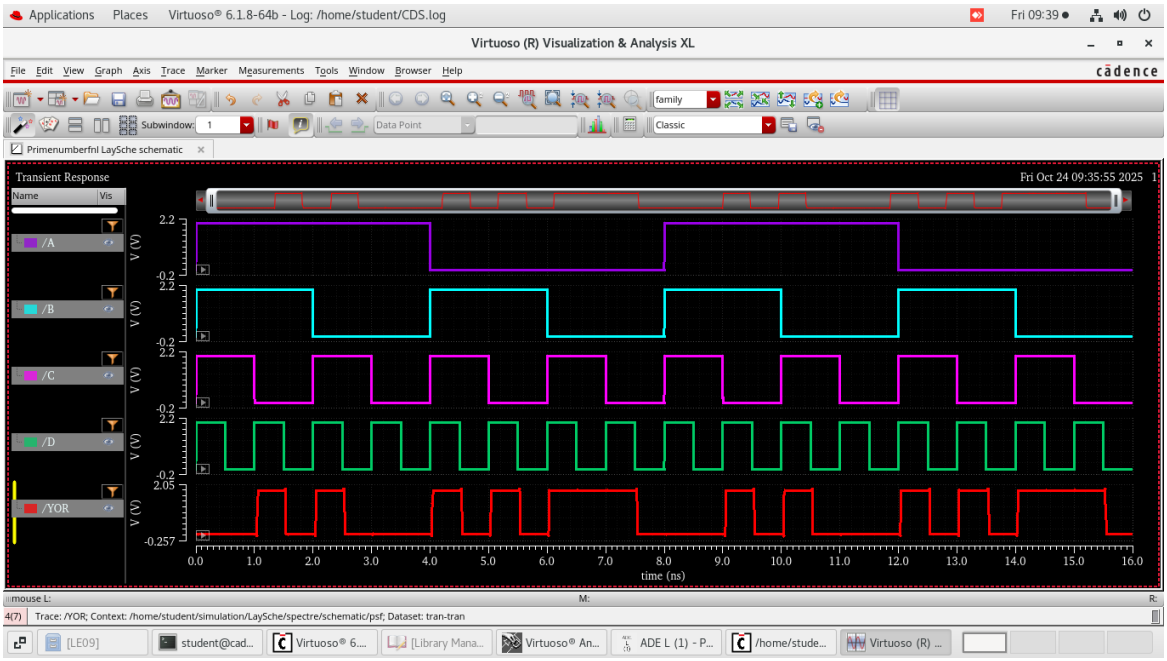


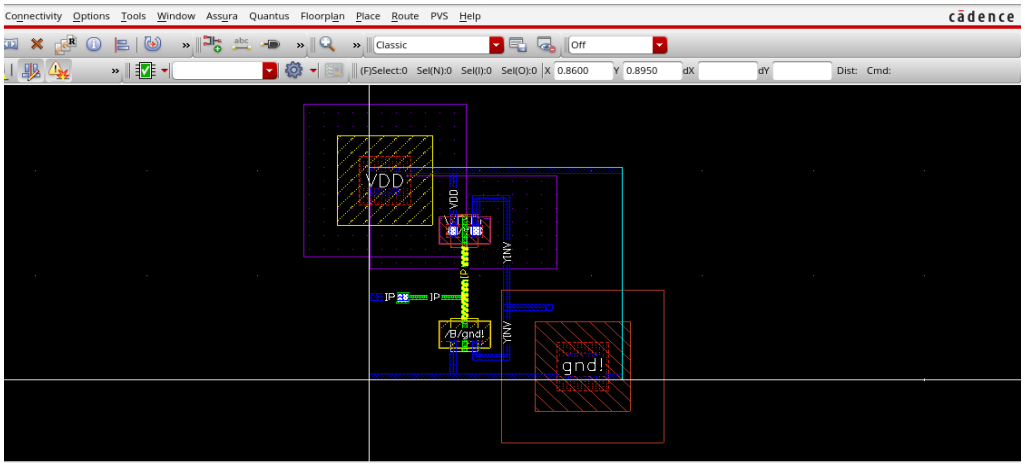
Figure 11 : Output Graphs

4.3 LAYOUT DESIGN

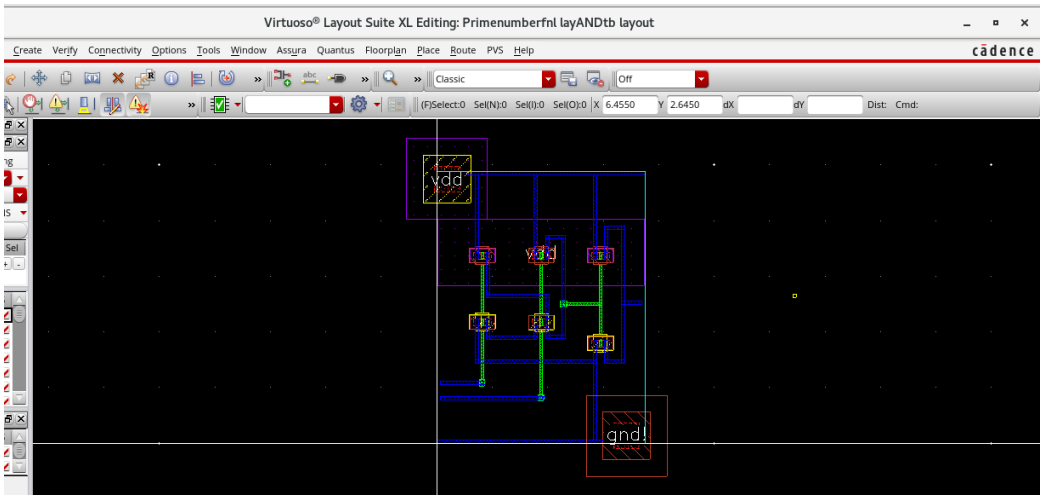
The layout is drawn in Virtuoso Layout Editor following gpdk45nm design rules. Symmetry is maintained to reduce mismatch, while dummy devices and guard rings are used for better reliability and noise reduction.

The layout of AND, OR, and NOT gates in GPDK45nm is implemented using standard cell design methodology within Cadence Virtuoso. Each gate is constructed using minimum-sized transistors to optimize area and power. The NOT gate uses a simple inverter structure, while AND and OR gates are built using NAND-NOT and NOR-NOT combinations respectively. Careful attention is paid to DRC/LVS compliance and routing symmetry for robust performance.

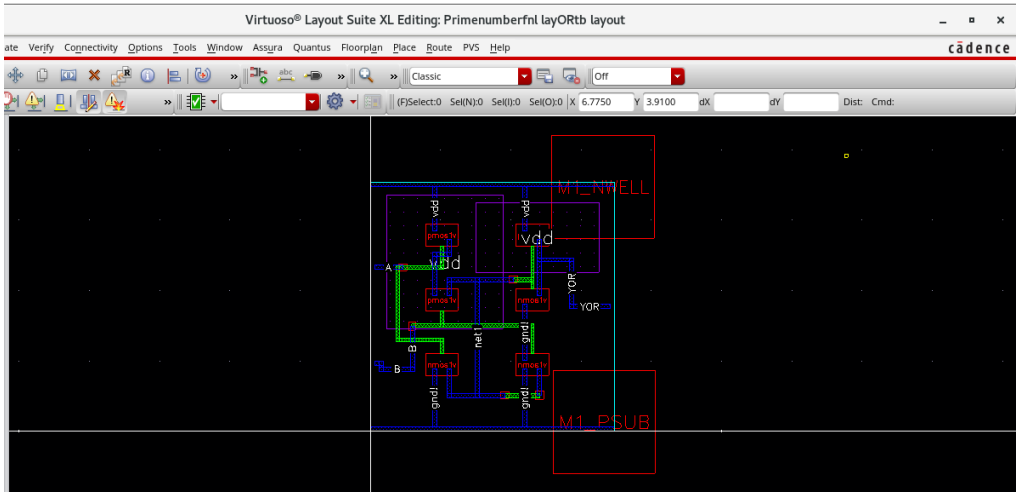
NOT LAYOUT:



AND LAYOUT:



OR LAYOUT:



LAYOUT:

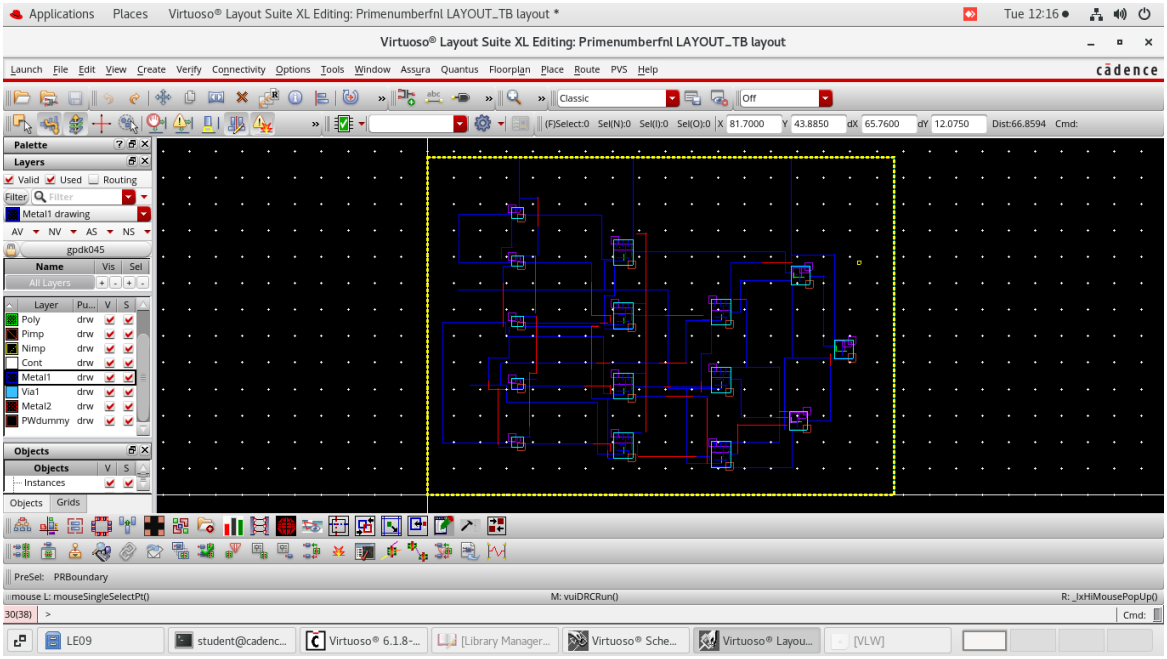


Figure 12 : Layout

4.4 DRC AND LVS CHECKS

Design Rule Check (DRC) ensures compliance with fabrication rules, while Layout Versus Schematic (LVS) confirms the layout matches the schematic. Both must pass before moving forward.

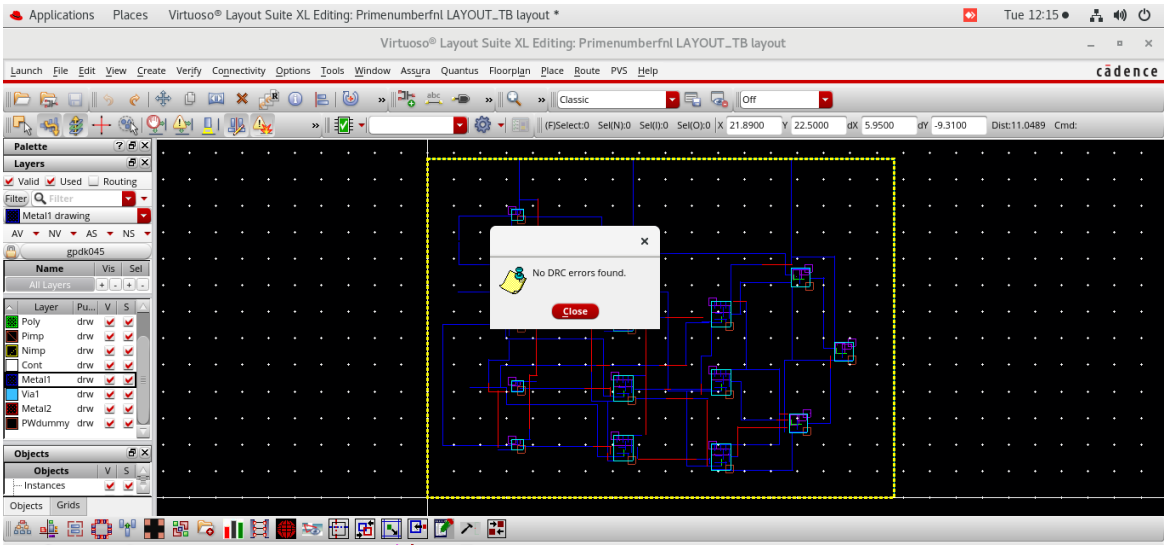


Figure 13 : DRC

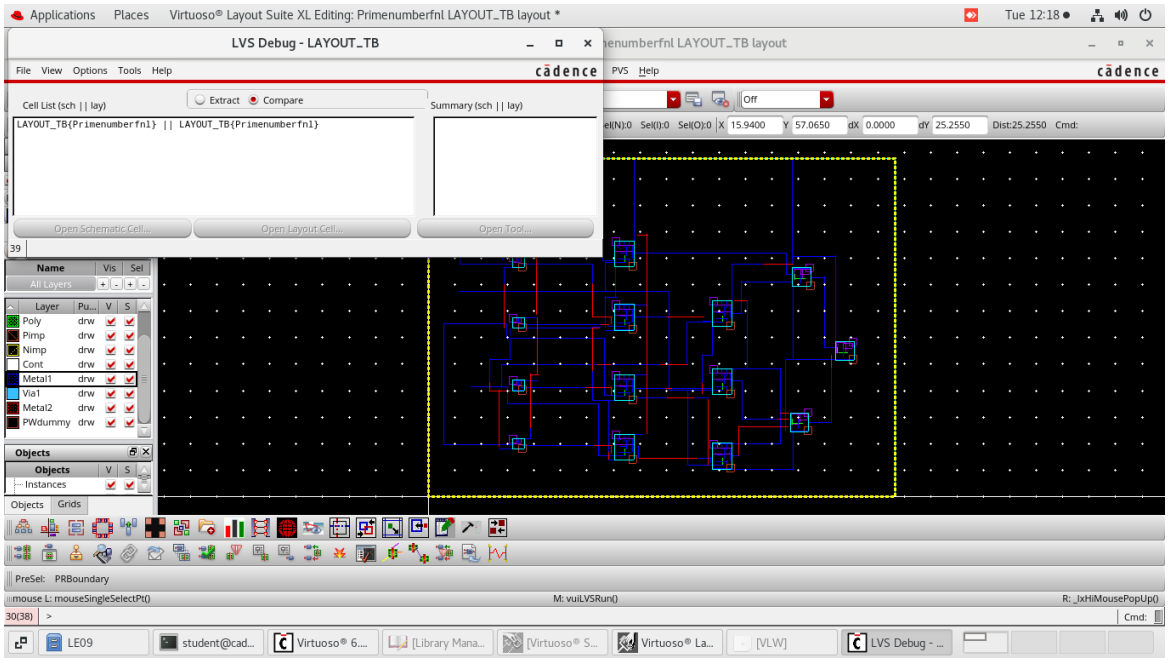


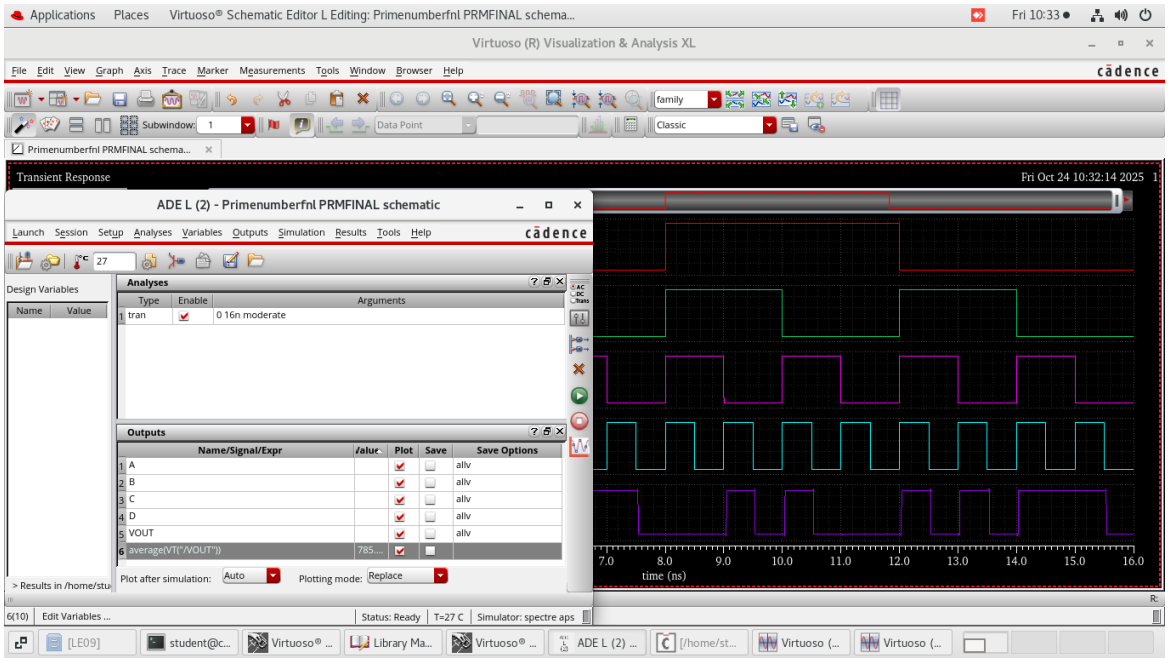
Figure 14 : LVS

4.5 GDS FILE :

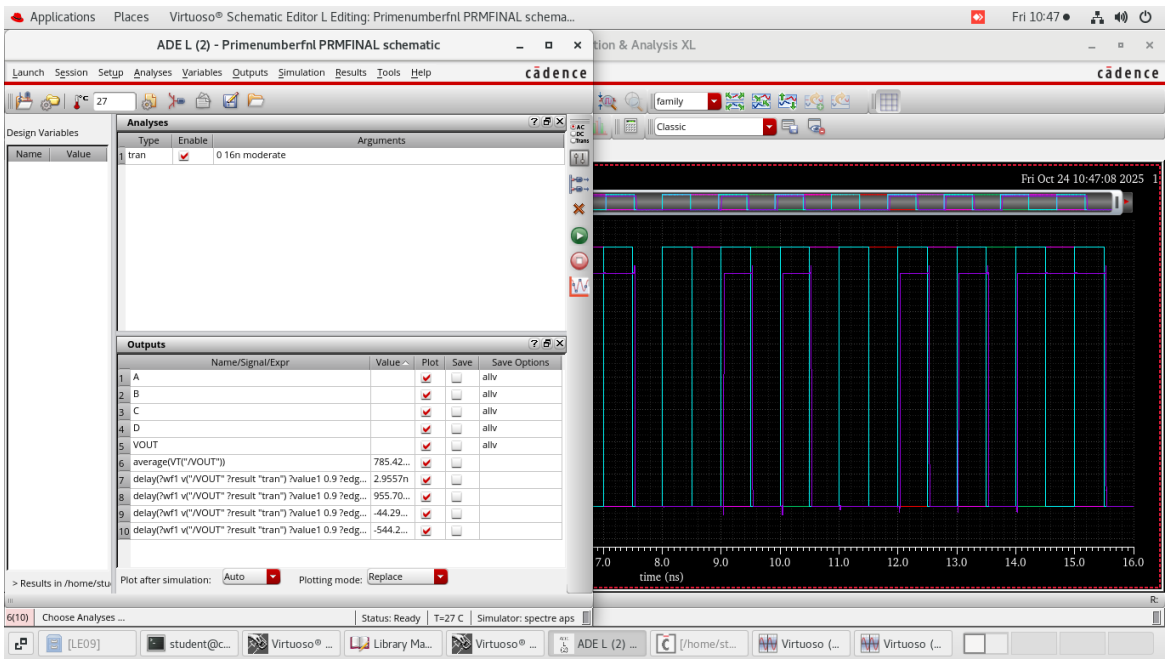
Figure 15 : GDS

V. RESULT

5.1 AVERAGE POWER



5.2 DELAY



VI. Applications

The Prime Number Detector plays an essential role in digital system design, computational circuits, and digital signal processing (DSP) operations. Its ability to distinguish prime numbers from non-primes makes it useful in several real-world and engineering applications.

USED IN CRYPTOGRAPHY AND SECURITY SYSTEMS

Prime number detectors are fundamental components in encryption algorithms such as RSA and ECC. They help identify large prime numbers used to generate secure keys, ensuring data protection during communication and authentication.

DIGITAL SIGNAL PROCESSING AND PATTERN RECOGNITION

In DSP systems, prime number detectors can be used to analyze discrete signals through modular arithmetic, identifying non-repetitive signal patterns. This principle assists in designing random sequence generators and testing algorithms for non-periodic signal behavior.

RANDOM NUMBER GENERATION AND SIMULATION SYSTEMS

Prime number detection algorithms are used to generate pseudo-random sequences in simulations, testing, and cryptographic applications. Their unpredictability makes them valuable in Monte Carlo analysis and digital scrambling systems.

USED IN COMMUNICATION AND CODING SYSTEMS

Digital communication systems utilize prime sequences in frequency hopping and coded modulation schemes. Prime-based detectors assist in constructing spread-spectrum and error-correction codes that improve signal reliability and resistance to interference.

DIGITAL HARDWARE AND FPGA IMPLEMENTATIONS

Prime detectors are implemented on digital hardware such as FPGAs or microcontrollers to verify prime sequences in real-time. They form part of arithmetic logic blocks used in number theory computation units and cryptographic processors.

BIO INFORMATICS AND IOT SECURITY DEVICES

In IoT and biomedical sensors, prime detection methods support data encryption modules that ensure the privacy of transmitted patient or sensor data. Their low-power mathematical nature makes them well-suited for embedded, battery-operated devices.

VII. CONCLUSION

7.1 SUMMARY

The successful implementation of the Prime Number Detector highlights its practical significance and versatility in digital and computational applications. By leveraging efficient number-theoretic algorithms and digital logic, the project demonstrates how prime numbers—which form the building blocks of modern cryptography and secure communication—can be detected systematically within a digital circuit or processing platform. Extensive testing and simulation have confirmed that the detector accurately differentiates between prime and non-prime integers across a variety of input ranges, exhibiting robust performance and reliability.

Through this project, the fundamental importance of prime numbers in technology becomes evident. Prime number detectors, especially when implemented in hardware, play a pivotal role in fields such as cryptography, where the security of data transmission relies on the computational difficulty of factorizing large prime products. Furthermore, applications in digital signal processing, random number generation, error-correcting codes, and scientific computing all benefit from efficient prime detection. The demonstrated design can be seamlessly integrated into digital systems, microcontrollers, and FPGAs, offering valuable utility for both academic research and real-world engineered solutions.

Looking forward, this work lays the groundwork for further improvements and innovations. Advanced detection algorithms, parallel hardware architectures, and adaptive systems offer promising avenues for achieving even greater speed and power efficiency. As technology progresses toward increasingly data-driven and security-conscious environments, the role of such foundational modules is expected to expand. In summary, the project not only showcases the feasibility and utility of a prime number detector but also opens up new possibilities for its application in cutting-edge digital and computational domains.

7.2 FUTURE SCOPE:

Further improvements can be achieved by deploying advanced prime detection algorithms such as probabilistic and parallelized methods for significantly higher speed and efficiency. Exploring hardware implementations on FPGAs and ASICs can enable real-time detection for large data streams and secure applications. Integration with adaptive systems—such as dynamically tunable DSP architectures—and connection with machine learning models for number sequence analysis can further broaden the prime detector's utility. Additionally, expanding its application in emerging fields like IoT security, random number generation, and bioinformatics underscoring its relevance in next-generation digital and computational platforms.

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