EEE1024: Fundamentals of Electrical and Electronics Engineering

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ARM specific features – which differ from RISC

- Variable cycle execution for certain instructions –

  (multiple-register load/store for higher code density)
- Inline barrel shifter leading to more complex instructions -

  (improves performance and code density)
- Thumb 16-bit instruction set:

  When 32-bit power is not needed, it can work with 16-bit thumb, resulting in 30% code density improvement

  (32-bit instructions that can be freely intermixed with 16-bit instructions in a program.)
- Conditional execution –

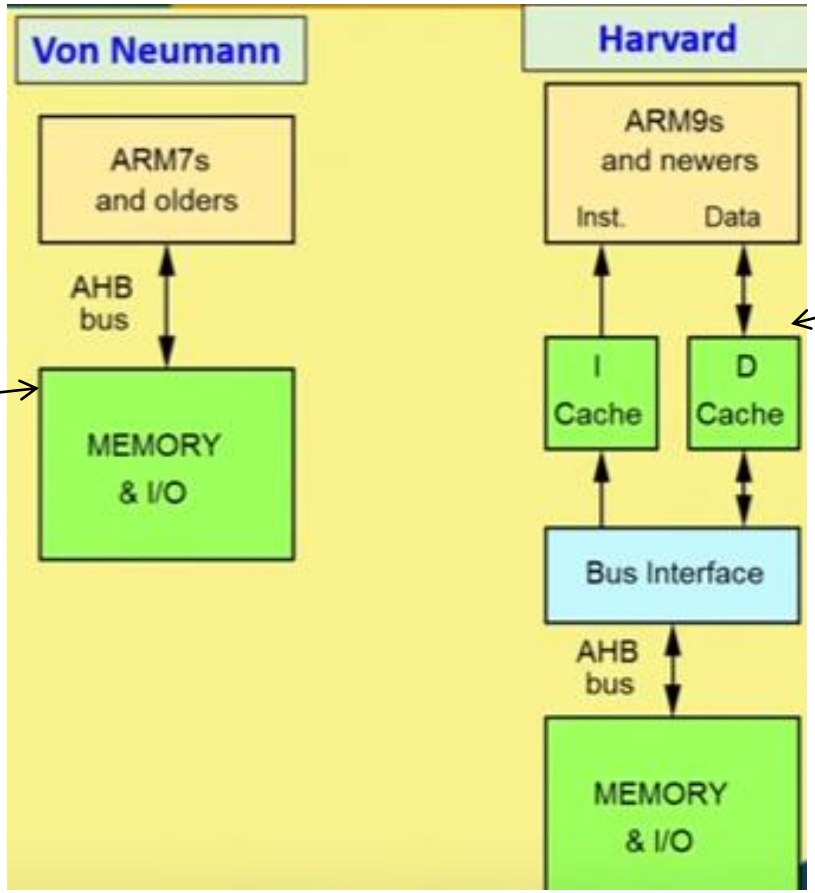
  reduces branches and improves performance

  (Add 2 numbers provided '0' flag is Set. This is common in other architectures' branch or jump instructions but ARM allows its use with most mnemonics.)

  Mnemonics:
  ADD for add and CMP for compare
- Enhanced instructions –

  additional functions like MULTIPLY and ADD especially for DSP applications (-from voice to audio to sensor hubs to machine learning (ML))

Architectures



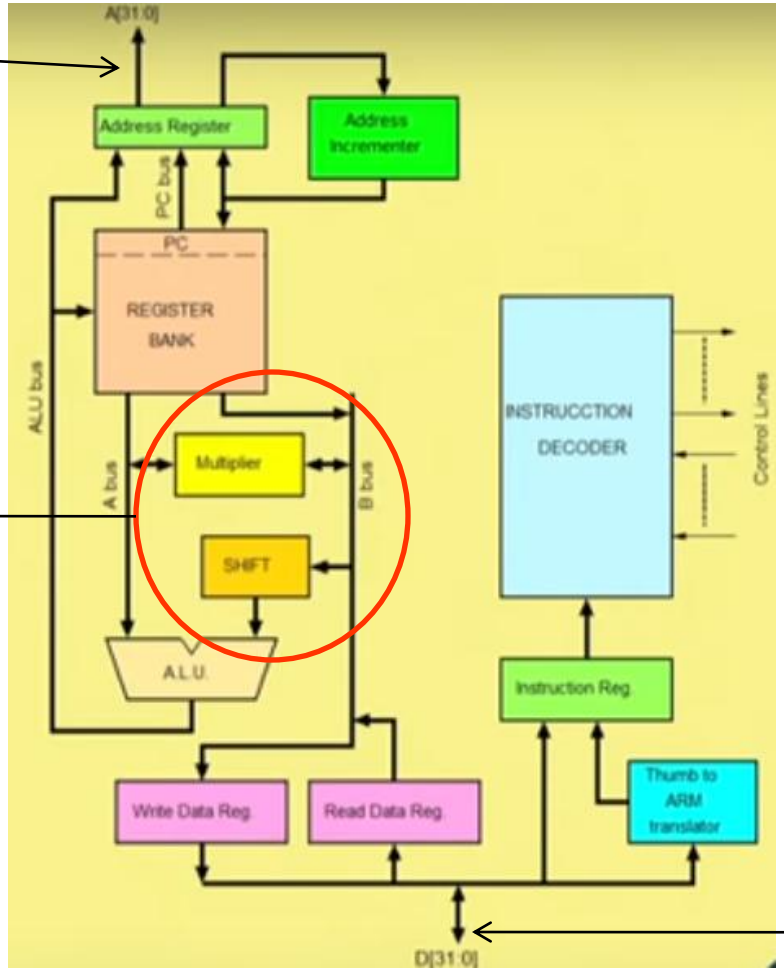
Single

Instruction and Data

Some part of memory is reserved for I/O

ARM7 Architecture

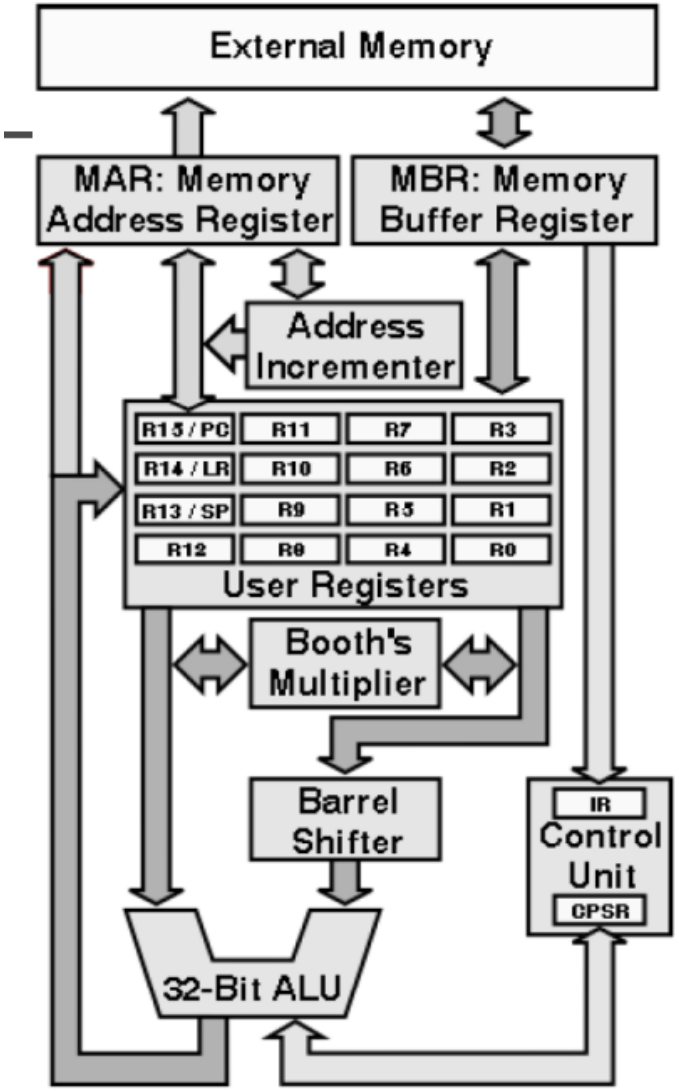
Address Bus



Unique feature of ***ARM***

Data Bus

ARM Architecture!



Different modes of ARM Processor

ARM Processor Modes

Interrupt handler routine

Memory protection

Expansion

Mode	Code	Description	Family
User	usr	Normal program execution, no privileges	All
FIQ	fiq	Entered when a High priority (Fast) interrupt is raised	All
IRQ	irq	Entered when a Low priority (Normal) interrupt is raised	All
Supervisor	svc	Privileged or protected mode for the operating system	All
Abort	abt	Used to handle memory access violations	ARMv3+
Undefined	und	Used to define undefined instructions - Facilitates emulation of co-processors in hardware	ARMv3+
System	sys	Runs privileged operating system tasks	ARMv4+

REGISTERS -I

- ARM has 37 registers all of which are 32 bit long
- These registers are –

a) 1 dedicated program counter (PC)

b) 1 dedicated current program status register (CPSR) ← Conditional flags

c) 5 dedicated saved program status register (SPSR)

d) 30 general purpose registers (GPR)

No support for Stack (FIFO)

REGISTERS - II

- Processor mode governs which of the several register sets is accessible

- Only 16 registers are visible to a specific mode of operation.

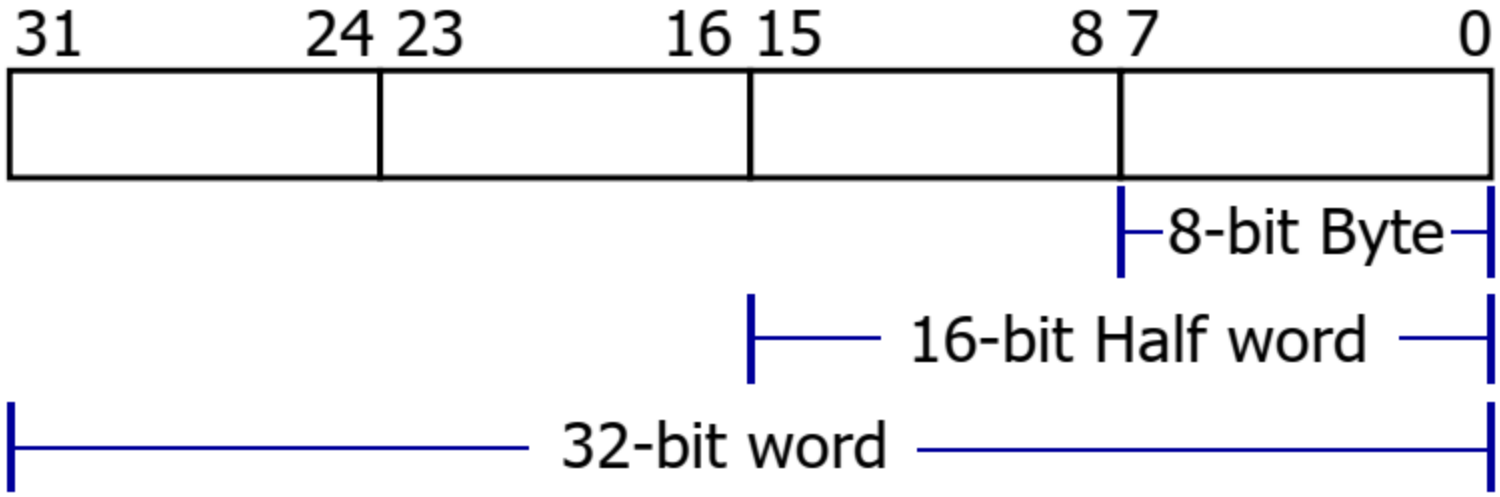
Each mode can access-

- A particular set of registers (r0-r12)
- r13 – Stack Pointer (SP)
- r14 – Link register (LR)
- r15 – Program counter (PC)
- Current program status register (CPSR)

General Purpose Registers (GPRs)

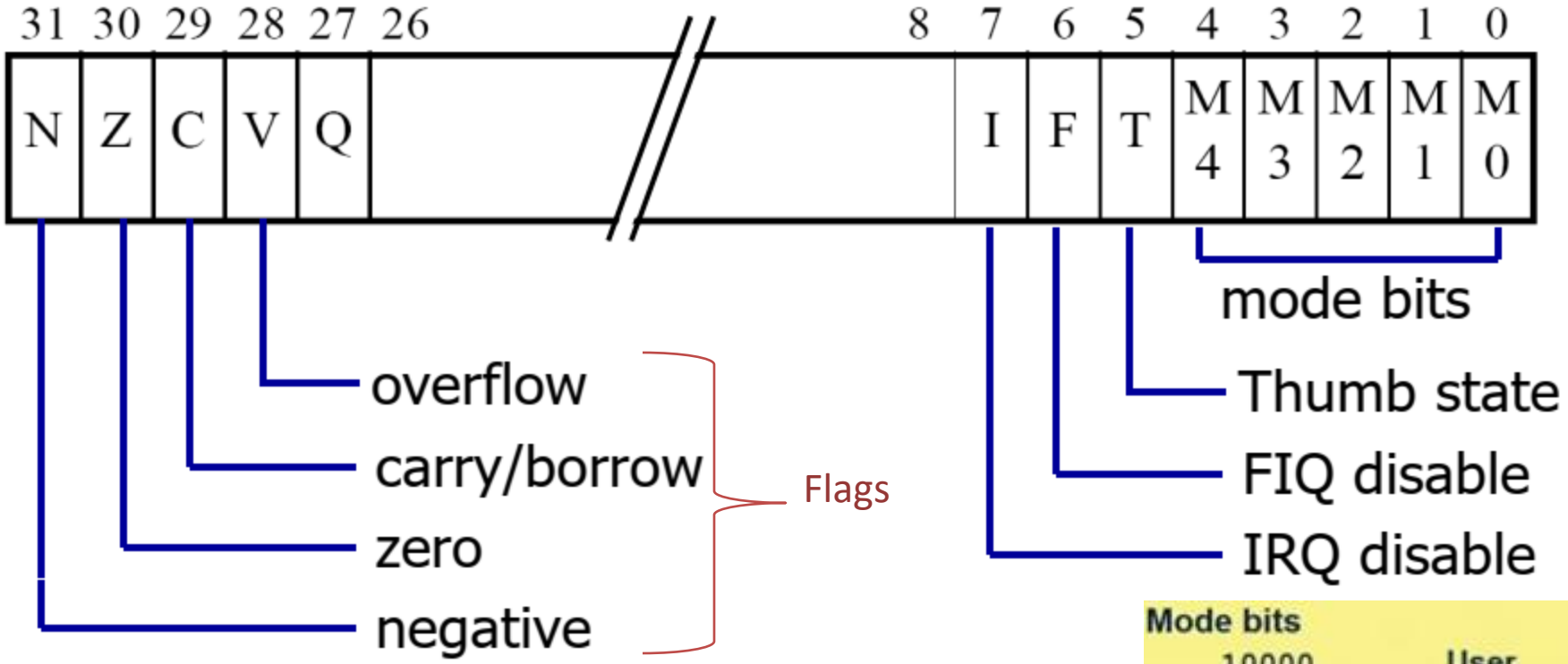
- 6 data types are supported (signed/unsigned)
- Operations that are supported – 8 bit byte, 16 bit half word, 32 bit word

- All ARM operations : 32-bit



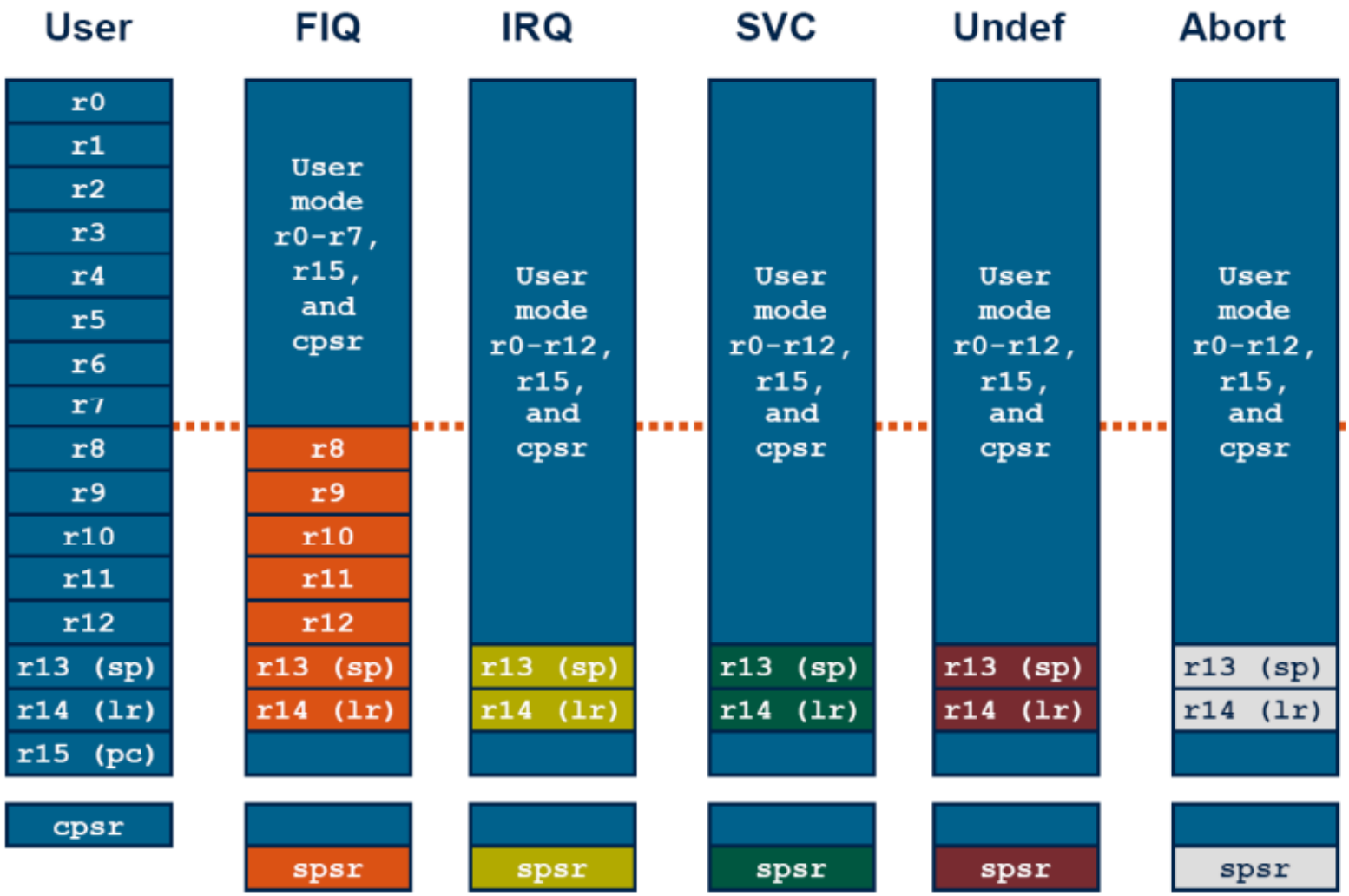
Arithmetic operations – 32 bit, Logical operations – shorter data types

Current Program Status Registers (CPSR)



Mode bits	
10000	User
10001	FIQ
10010	IRQ
10011	Supervisor
10111	Abort
11011	Undefined
11111	System

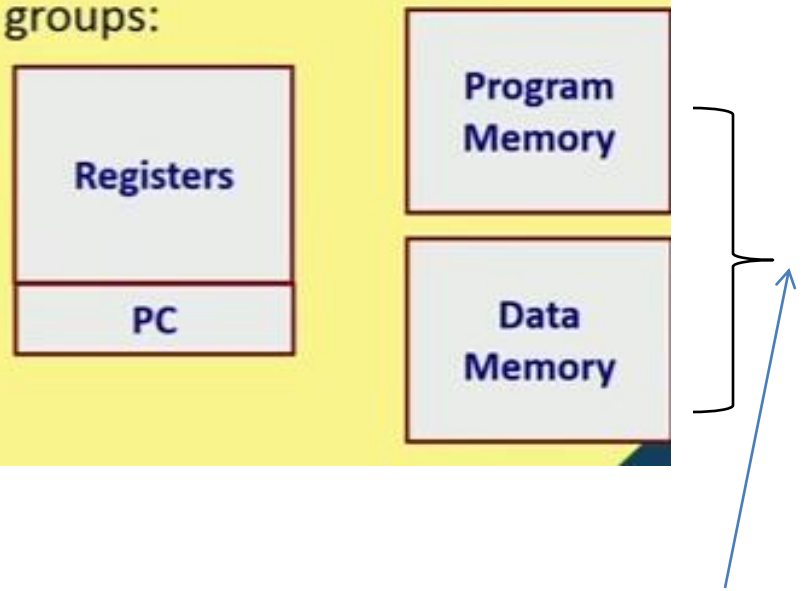
REGISTER ORGANIZATION



INSTRUCTION SET of ARM Processor

The ARM INSTRUCTION SET

- ARM instruction can be categorized into three groups:
  - a) Data processing instructions
    - Operate on values in registers
  - b) Data transfer instructions
    - Move values between registers and memory
  - c) Control flow instructions
    - Change the value of the program counter (PC)



Harvard architecture

Acknowledgements

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3. https://developer.arm.com/documentation/dui0471/i/key-features-of-arm-architecture-versions/thumb-2-technology
4. https://www.arm.com/why-arm/technologies/dsp
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