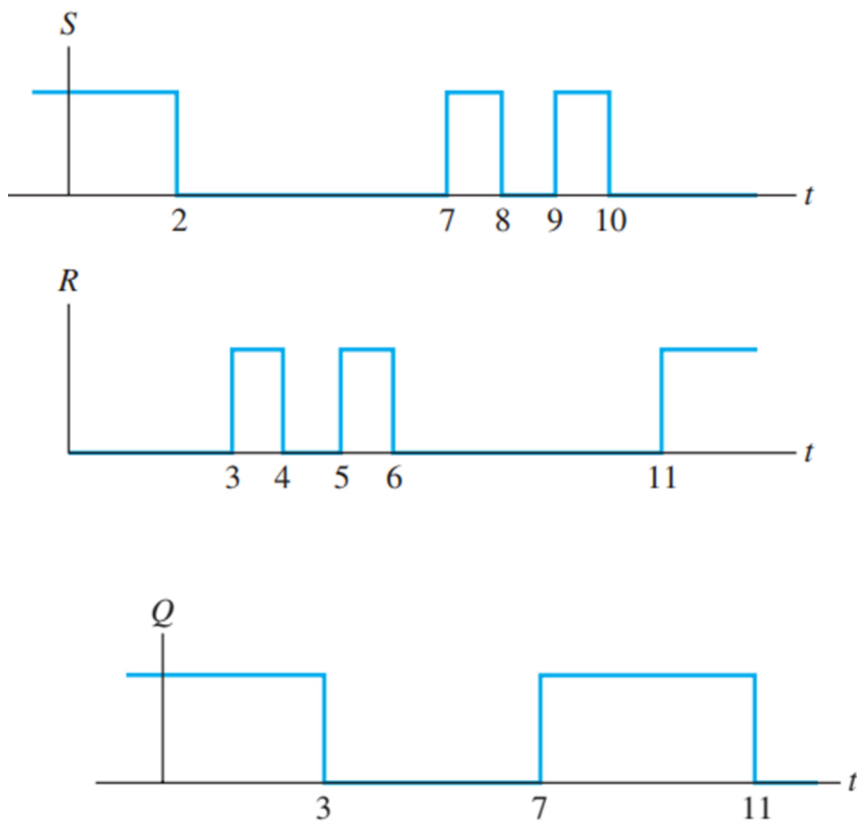


Example 1 Flipflop

Wednesday, 2 September, 2020 10:00 AM



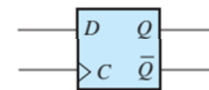
R	S	Q_n
0	0	Q_{n-1}
0	1	1
1	0	0
1	1	Not allowed

(a) Truth table

Example 2

Wednesday, 2 September, 2020 10:11 AM

- The input signals to a positive-edge-triggered D flip-flop are shown in Figure. Sketch the output Q to scale versus time. (Assume that Q is low prior to $t = 2$.)



(a) Circuit symbol

C	D	Q_n
0	\times	Q_{n-1}
1	\times	Q_{n-1}
\uparrow	0	0
\uparrow	1	1

(b) Truth table
indicates a transition
from low to high

