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Continuous Assessment Test II

Computer Architecture and organization

CSI1004

Slot : D1 And D2 **Max : 30 marks** **Duration : 45 Mins**

Answer All the questions

1. Designed a cache memory with the size of 4GB, main memory (16GB), start the execution of task requires 3GB of data, dynamically new requirement of 2GB of data needed, how can this situation is handled in cache memory.

   2GB of required reference string are 1 2 3 0 4 5 7 0 1 2 2 3 4 5 6 7 8 7 0 0 1 1.
   Page size is = 1GB
2. Assume that the new design of processor involves 16 bit addition of two numbers, how can you design the algorithm to match cases (signed and unsigned) with an example.
3. Solve the 100011110/10111 by using the restoring and non restoring method with the support of algorithms.
4. Assume that different levels of cache are allowed, how this will affect the performance of the system or improve the performance of the system.
5. Discuss the algorithm for multiplication of -8 x -14, how the sign magnitude is handled?
6. Following requirements are given, cache memory – 64KB and the main memory – 128KB, Frame-4, discuss the advantage and disadvantage over different mapping procedure with the above given requirements.
7. Register A holds 8(1110 0 111) bit number, register B holds the 4(1111) bit number, how can you develop the algorithm in your design?
8. Design hardware (single unit) to perform the addition, subtraction, multiplication, division.
9. Main memory with the size of 16KB and virtual memory is 64KB and execution of single program needs 1GB of reference string. How can you resolve this issue?
10. What is the modification to be done on booth multiplication algorithm when 3 numbers are given for multiplication (1000 x 1001 x 0111).
11. Justify-“replacement algorithm not used in cache memory “any other mechanism can be adopted?
12. Design a hardware and algorithm for multiplying 32 bit x 32 bit.

13. Compare and contrast the application of restoring and non restoring division method for an example 15/2.
14. Differentiate the multiplication algorithm and booth multiplication algorithm with an example of 30 x 16.
15. Device an algorithm for performing 15 % 3.
16. Cache memory with the size of 4KB(4 lines) and the virtual memory with the size of 8KB(Lines) following reference string is needed for the execution

    1 2 1 2 3 4 5 6 8 9 10 12 11 8 9 6 7 2 3 1 2 11 12 1 2 3 4 9 6 7 8 1.

    How the execution is carried out?
17. Design hardware for storing a 6 bit number in the dynamic RAM.
18. Design a DRAM for 128 x 16.