EEE1024: Fundamentals of Electrical and Electronics Engineering

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Module 3

1. Number Systems - Conversions
2. Logic Gates
3. Boolean Algebra
4. Computer Organization (Memory)
5. HA, FA, Mux, Demux
6. Sequential - Flip flops, Counters

SPECIAL Circuits – Half Adder & Full Adder

ADDERS

Digital Circuits –
Addition of 2 ***binary*** digits

Half Adder

Performs addition of 2 bits

Full Adder

Performs addition of 3 bits

Binary Addition

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

```
                        1
0   1   0   0   0   0   0   1
0   1   0   0   1   0   1   1
-----------------------------
1   0   0   0   1   1   0   0
```

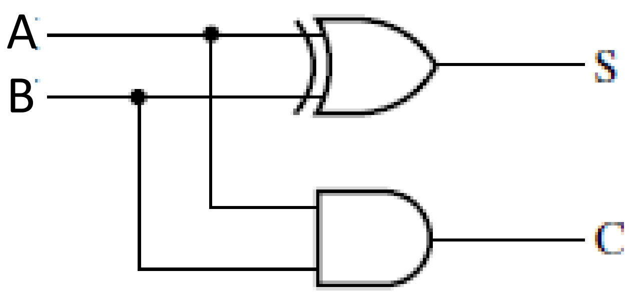
HALF ADDER

Binary Addition

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table of XOR gate

A	B	C= $A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

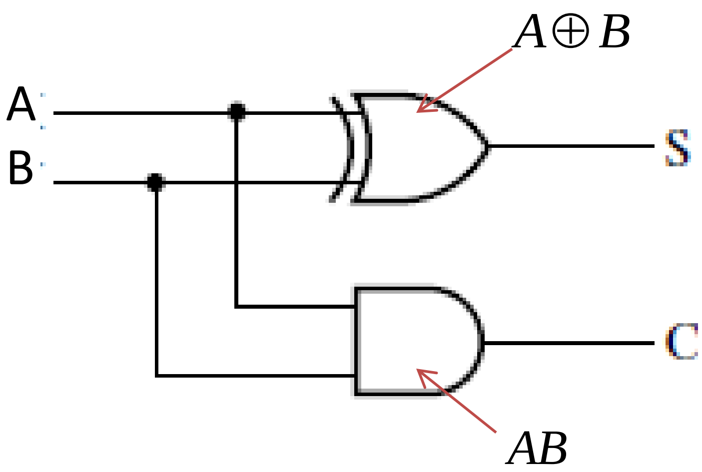


Truth table of AND gate

A	B	$C = AB$
0	0	0
0	1	0
1	0	0
1	1	1

HALF ADDER(2 bits)

Logic Circuit: Realization of Half Adder



Truth table

Inputs		Outputs	
A	*B*	*Sum ($A \oplus B$)*	*Carry (AB)*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Binary addition: If there is any ***Carry*** in the input?
- Half adder cannot do the addition then !!!
- Which is why it is called HALF adder as only half of the binary addition is done

FULL ADDER (3 bits)

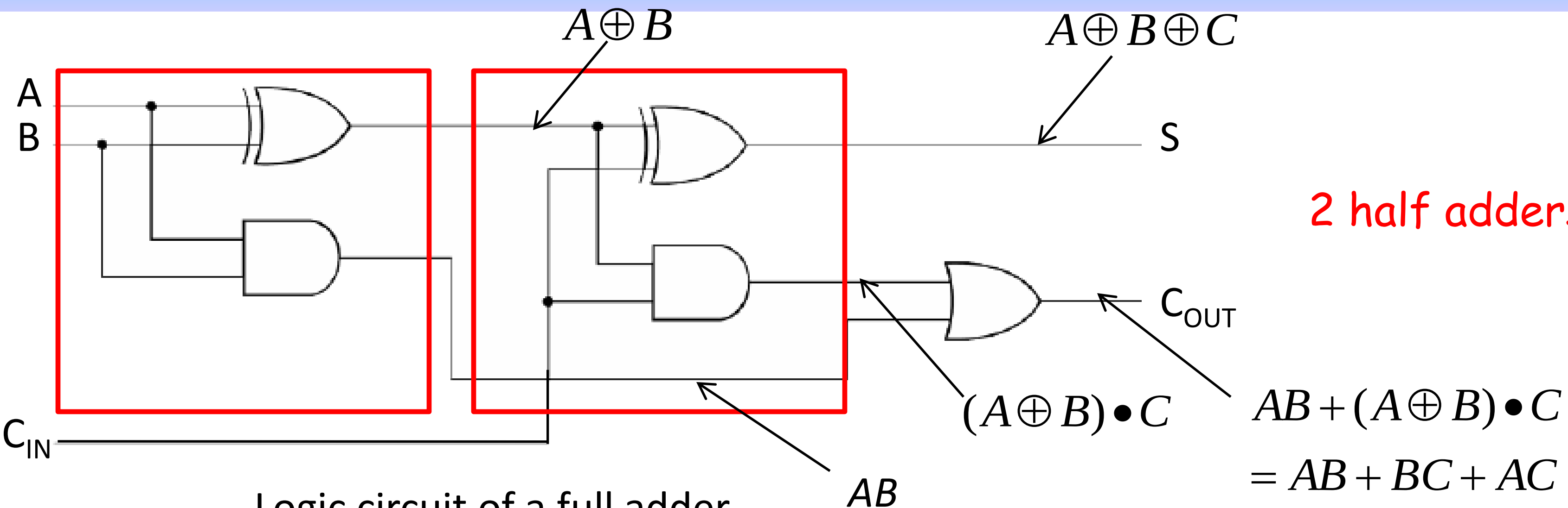
- The additional 3rd bit – Carry from previous operation - C_{IN}
- Two outputs – Sum –S (final) and Carry - C_{OUT}

Inputs			Outputs	
A	B	C_{IN}	S	C_{OUT}
0	0	0	**0**	**0**
0	0	1	**1**	**0**
0	1	0	**1**	**0**
0	1	1	**0**	**1**
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Realize a logic circuit?

- 1 XOR, 3 AND, 1 OR
- 2 Half-adders and an OR gate

FULL ADDER (3 bits)



Logic circuit of a full adder

2 half adders used

- First half adder produces a partial sum
- This sum is connected as input to 2nd half adder alongwith C_{IN} which produces final sum S
- Carry outputs of the 2 hald adders connected to an OR gate which produces final carry C_{OUT}

Multiplexer and De-multiplexer

Multiplexer (MUX) *- "Many-to-one" digital switch*

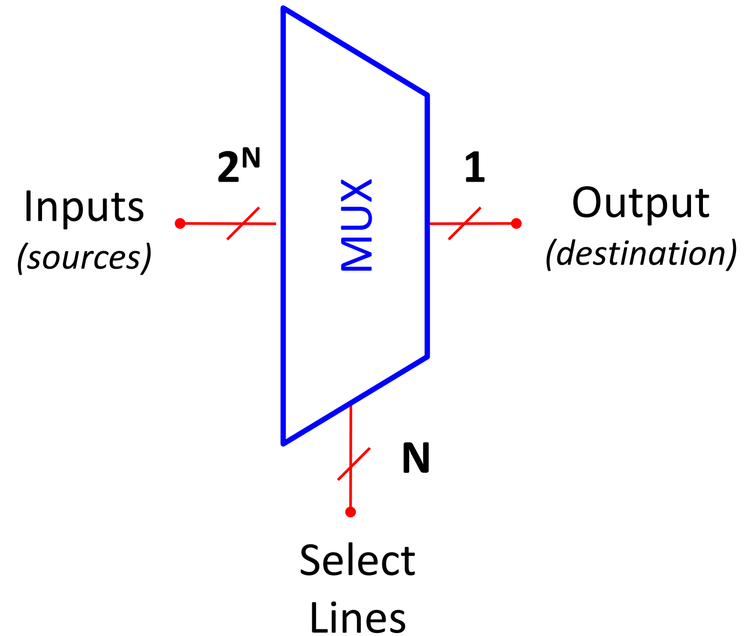
○ A combinational logic circuit has **multiple inputs** (sources) and a **single output** (destination).

○ **Only one input is allowed at a particular time** to be connected to the output.

○ **SELECT Lines** control which line (signal) is connected to the output

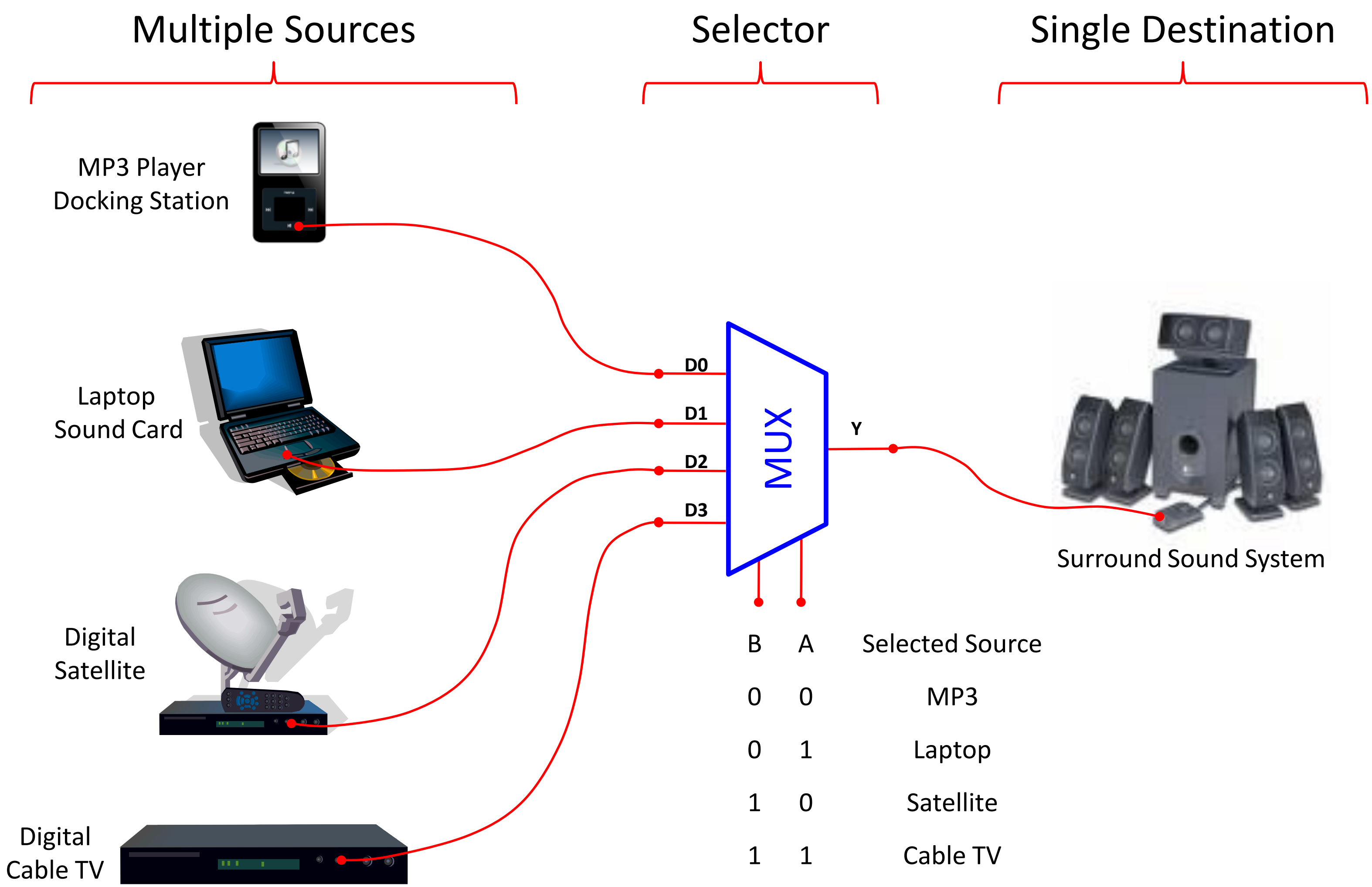
MUX Types

→ 2-to-1 (1 select line)
→ 4-to-1 (2 select lines)
→ 8-to-1 (3 select lines)
→ 16-to-1 (4 select lines)



Block diagram

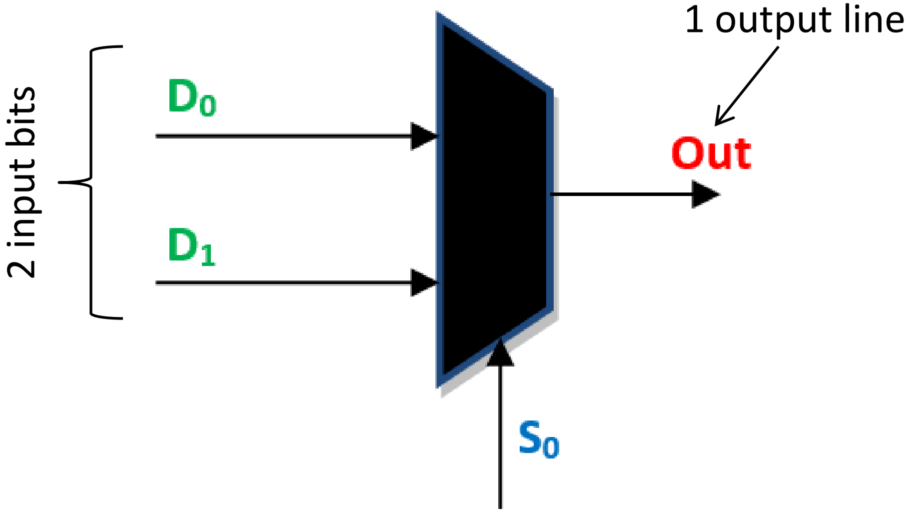
A typical application of MUX



B	A	Selected Source
0	0	MP3
0	1	Laptop
1	0	Satellite
1	1	Cable TV

2:1 Multiplexer (MUX)

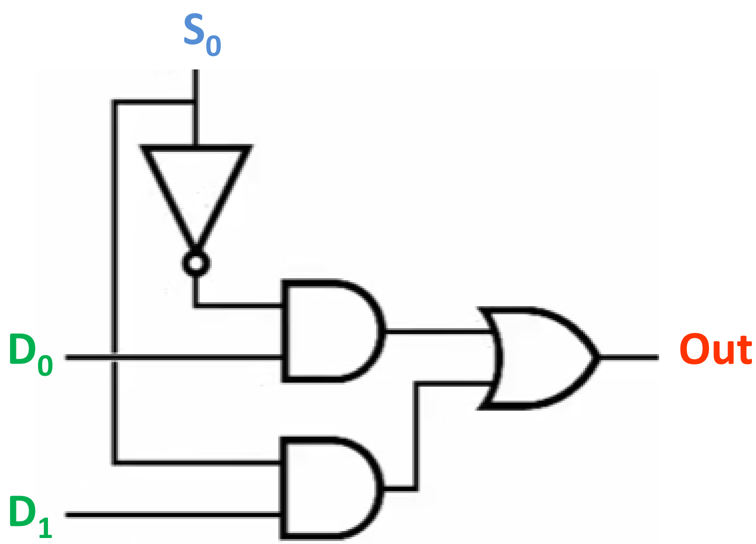
Block diagram



Truth table

S0	D0	D1	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

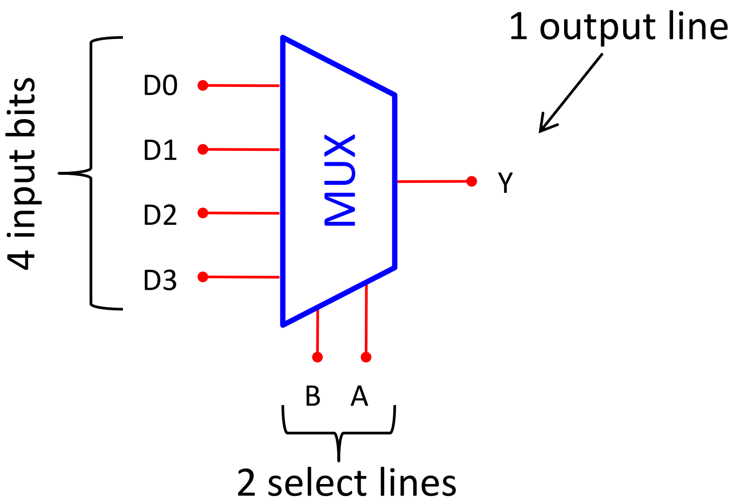
Logical circuit



- When S0 is 0, output reflects values of D0
- When S0 is 1, output reflects values of D1

4:1 Multiplexer (MUX)

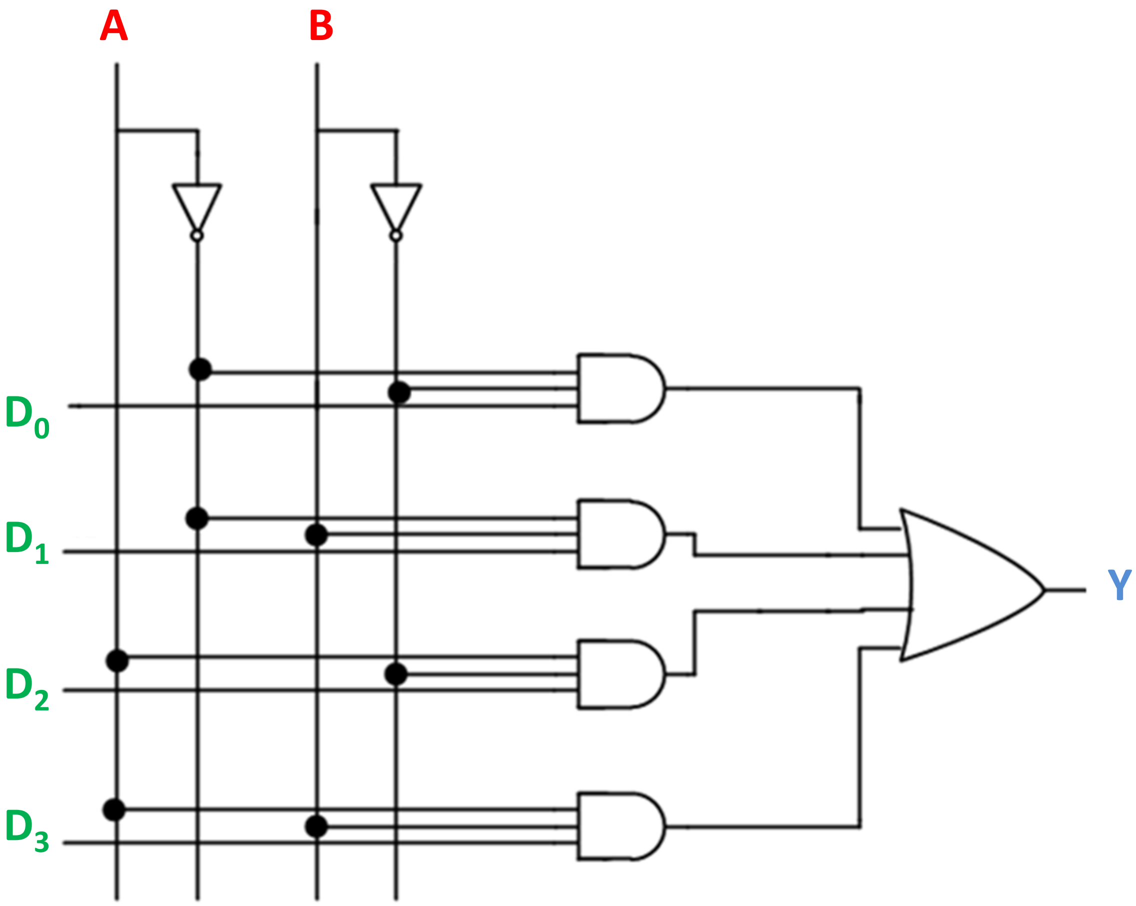
Block diagram



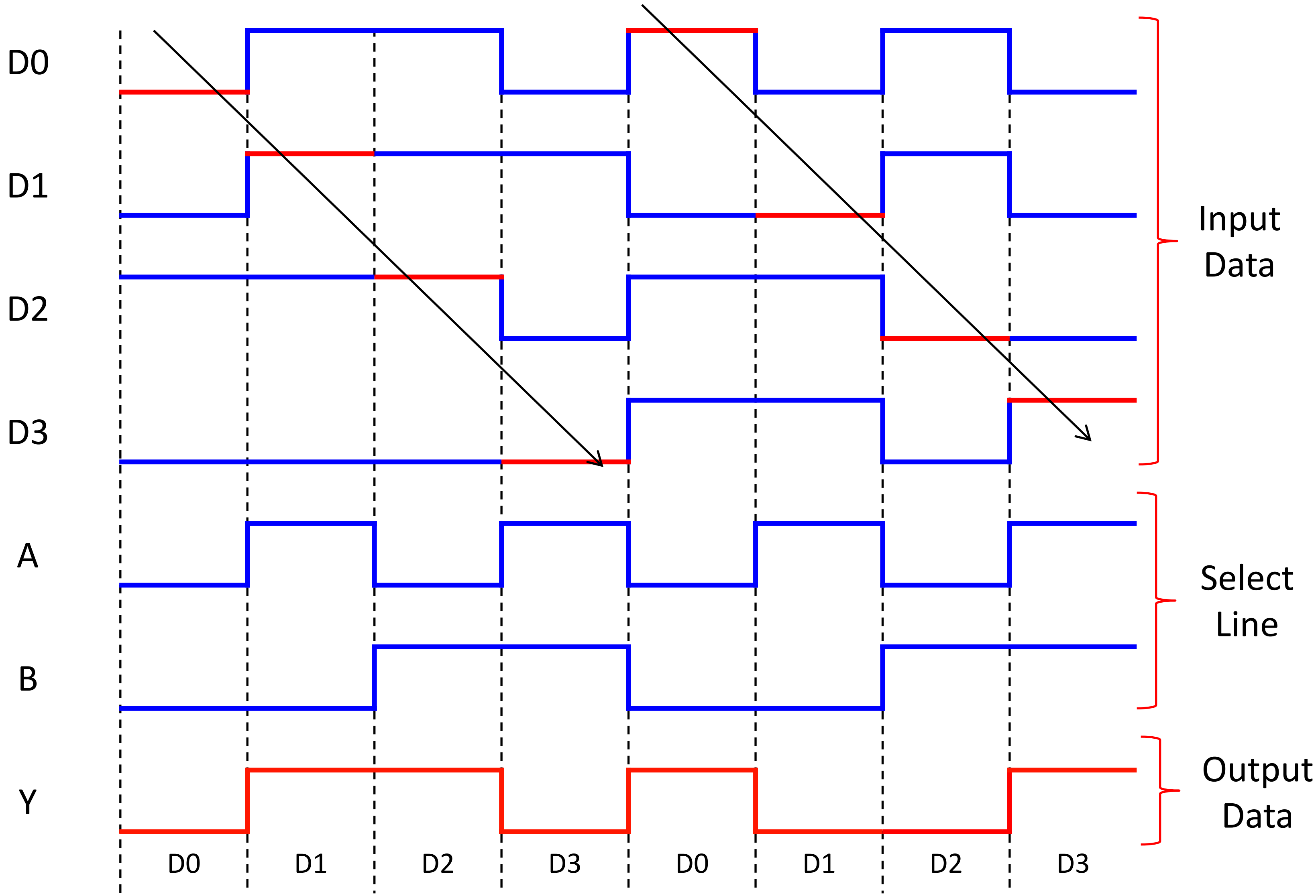
Truth table

B	A	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Logical circuit



4:1 Multiplexer waveforms



De-multiplexer

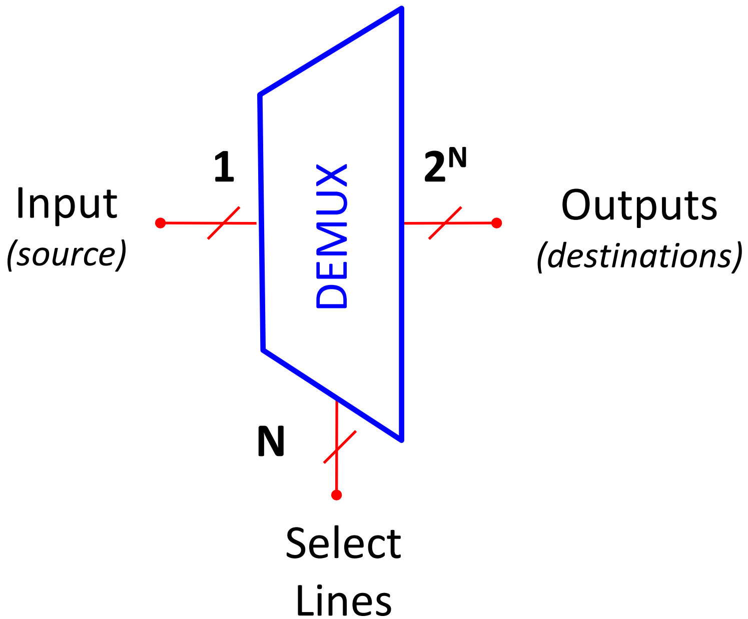
De-multiplexer (DEMUX) *- "One-to-many" digital switch*

- A combinational logic circuit which has a **single input** (source) and a **multiple outputs** (destinations)

- **SELECT Lines** control which line (signal) is connected to the output

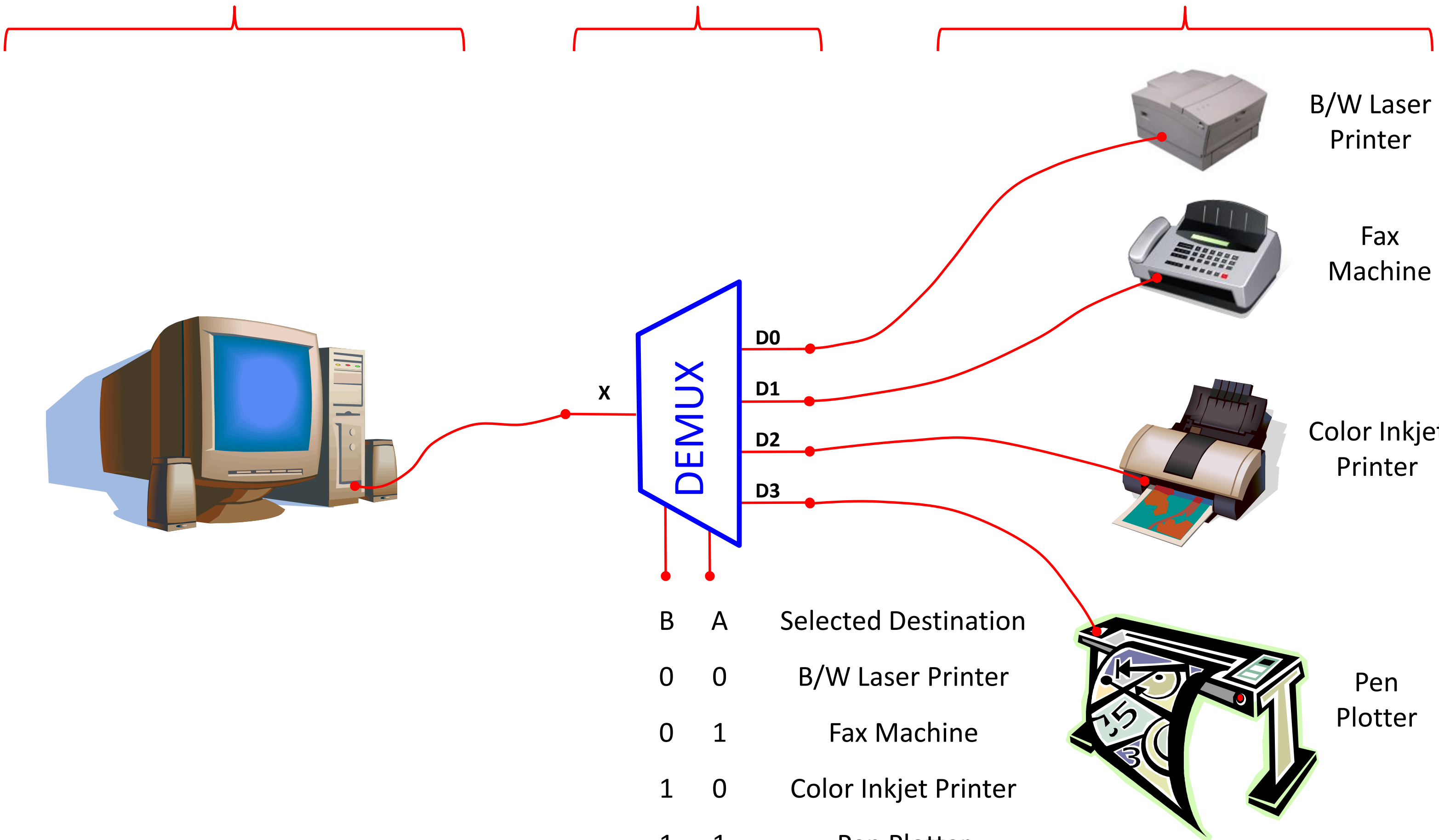
DEMUX Types

→ 1-to-2 (1 select line)
→ 1-to-4 (2 select lines)
→ 1-to-8 (3 select lines)
→ 1-to-16 (4 select lines)



A typical application of DEMUX

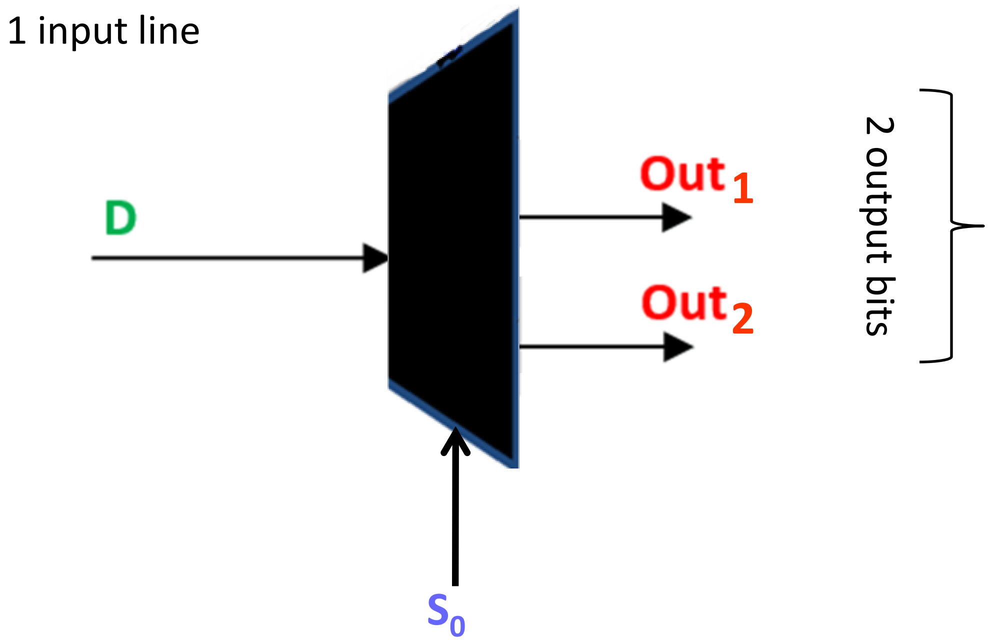
Single Source | Selector | Multiple Destinations



B	A	Selected Destination
0	0	B/W Laser Printer
0	1	Fax Machine
1	0	Color Inkjet Printer
1	1	Pen Plotter

1:2 De-multiplexer (DEMUX)

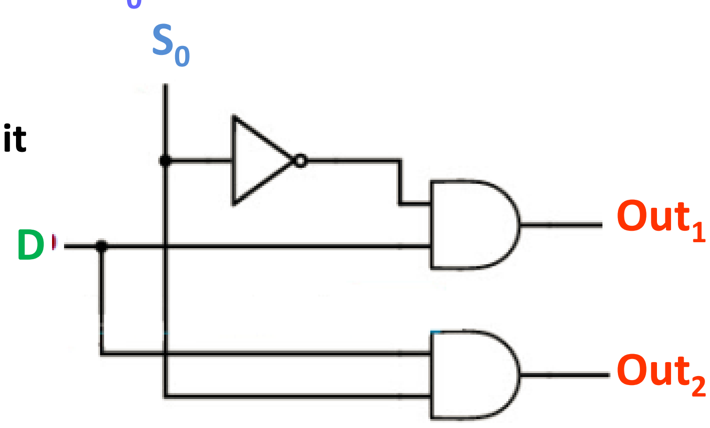
Block diagram



Truth table

S_0	D	Out_1	Out_2
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

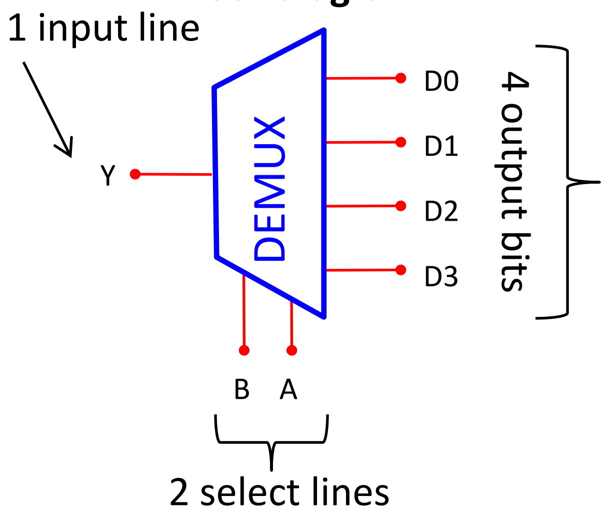
Logical circuit



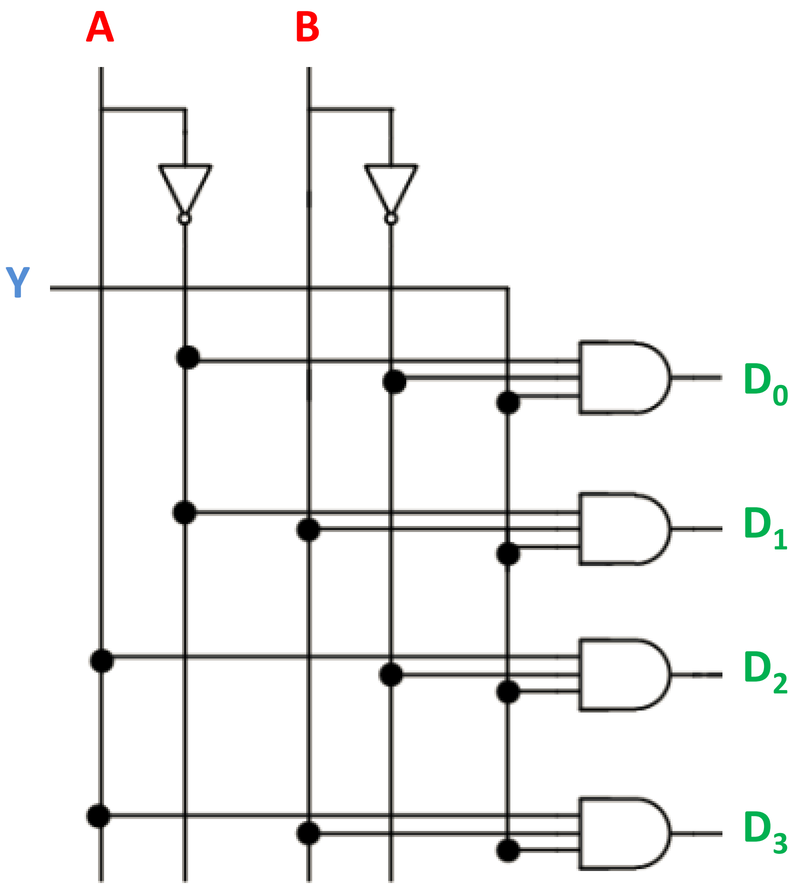
- When S0 is 0, input D is connected to Out_1
- When S0 is 1, input D is connected to Out_2

1:4 De-multiplexer (DEMUX)

Block diagram



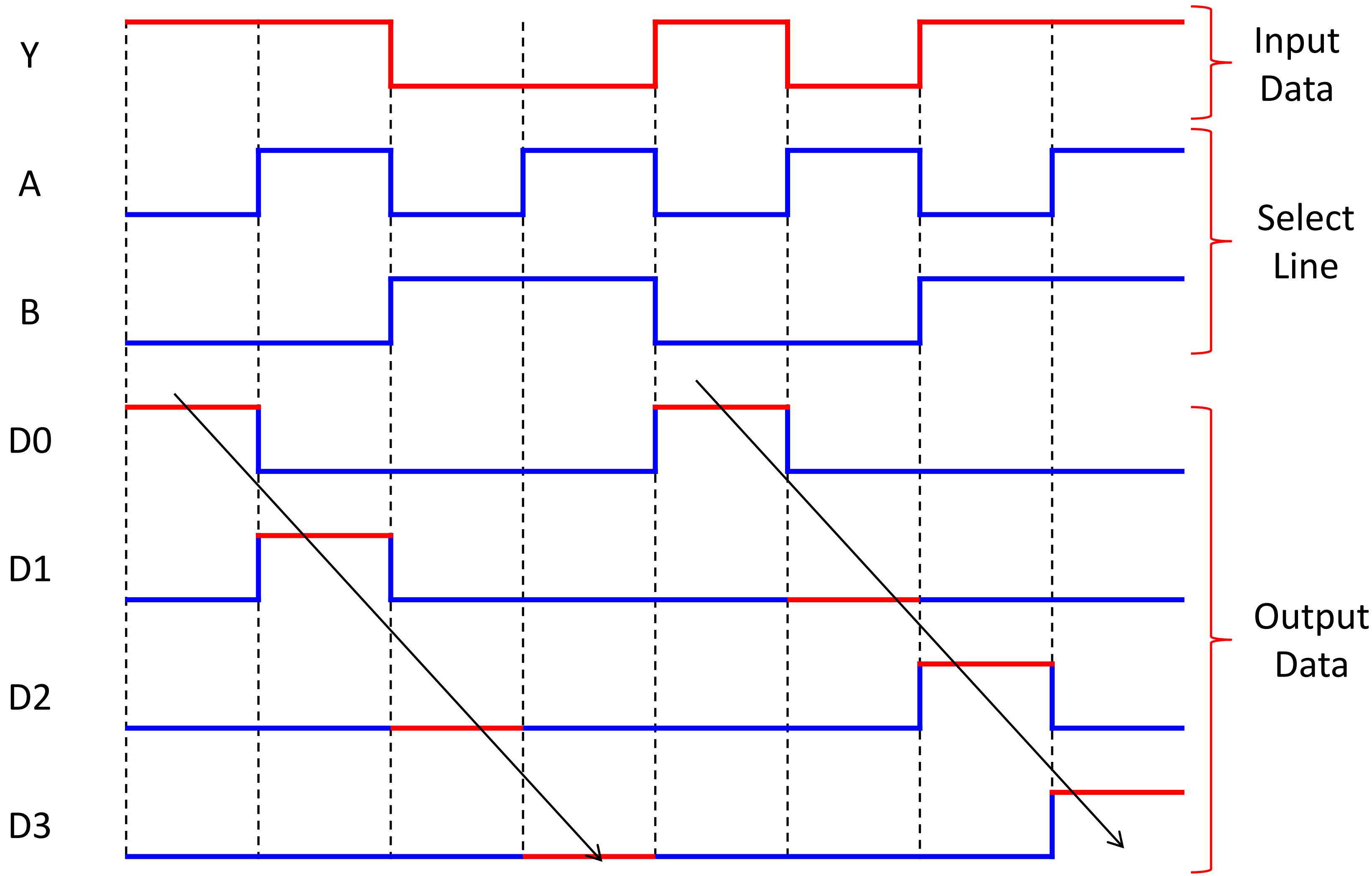
Logical circuit



Truth table

B	A	D0	D1	D2	D3
0	0	Y	0	0	0
0	1	0	Y	0	0
1	0	0	0	Y	0
1	1	0	0	0	Y

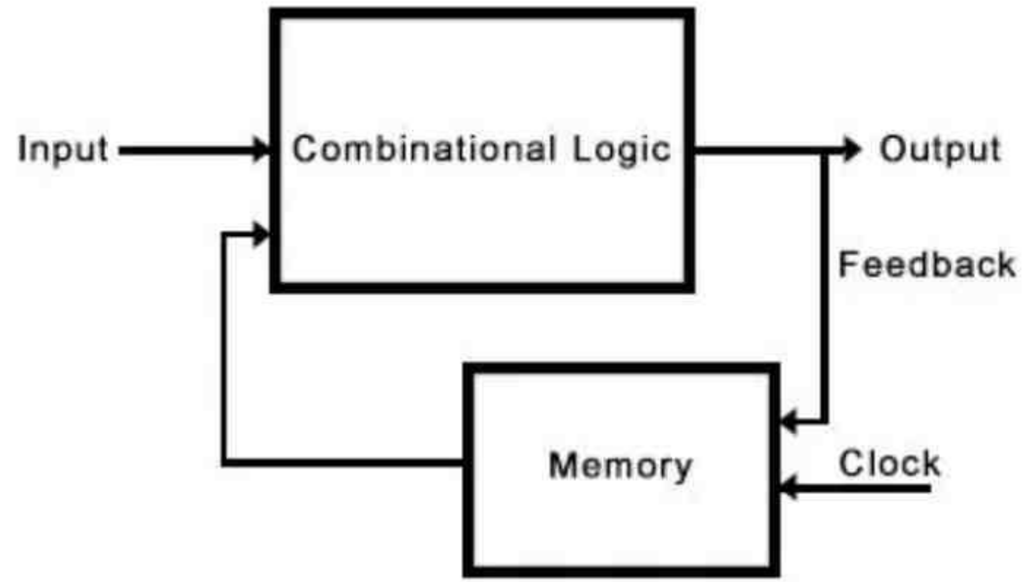
1:4 De-multiplexer waveforms



SEQUENTIAL CIRCUITS

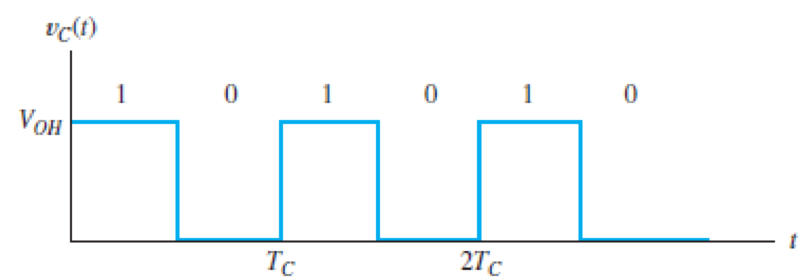
Sequential circuits

Synchronous Sequential circuit



- MEMORY – remember past values

- CLOCK signal – Periodic logic-1 pulses



Asynchronous sequential circuits

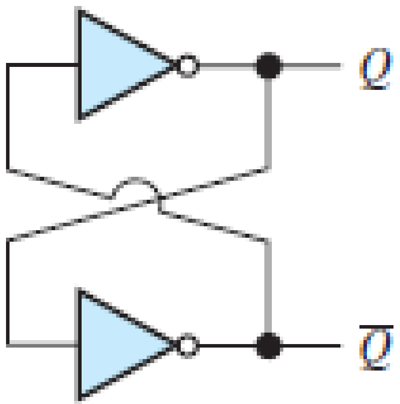
Sequential circuits – Flip flops

Basic building block of sequential circuits – FLIP FLOP (FF)

➢ Two stable operating states possible in a flipflop,
1 bit of information (0,1) can be stored

➢ Different types – based on how the clock and input signals control the state (o/p) of the flipflop

Simplest FF – using inverters



❖ O/p of top inverter – HIGH, o/p of bottom inverter – LOW.

❖ Hence labeled as $\overline{Q}$

❖ O/p of top inverter – LOW, o/p of bottom inverter – HIGH.

❖ Any of these states possible and then can remain in this state indefinitely

Acknowledgements

1. Allan R. Hambley, ‘Electrical Engineering - Principles & Applications, Pearson Education, First Impression, 6/e, 2013
2. https://www.circuitstoday.com/half-adder
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