VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Slot: A1

Fall Semester 2020-2021

Continuous Assessment Test –II

Programme Name & Branch: MIC & SCOPE **Class Number:** VL2020210105225

Course Code: EEE1024 **Course Title:** Fundamentals of Electrical and Electronics Engineering

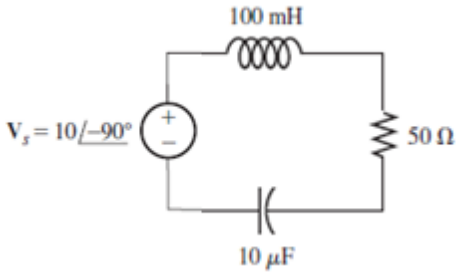
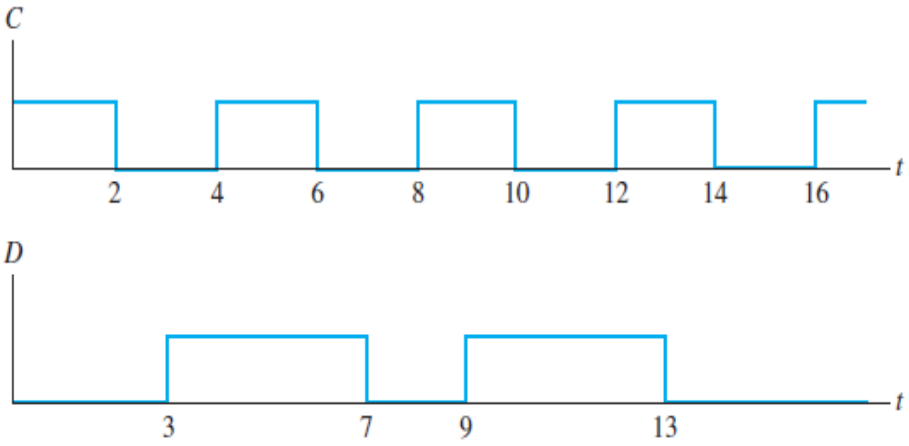
Exam Mode: Online **Exam Duration:** 45 mins **Maximum Marks:** 30

Faculty Name: Prof. Sanchit Khatavkar

General instruction(s):

Refer MS Forms and Teams

(Marks distribution: 5 questions x 6 = 30 Marks)		
S.No.	**Question**	**Course Outcome (CO)**
1.	Prove the distributive law for AND operation of 3 logical inputs A, B and C using truth tables. (Law statement – 2marks, Intermediate steps – 2marks, Final – 2marks)	CO_03
2.	Convert the following- (Each sub-question: 3 marks – 2 marks for working, Final - 1 mark) a) **782.23_{10}** to binary b) **10011110_2** to hexadecimal	CO_03
3.	Given: $v_1(t) = 100\cos(\omega t + 45^0)$ and $v_1(t) = 100\sin(\omega t + 60^0)$. a) Using phasors, reduce the sum $v_s(t) = v_1(t) + v_2(t)$ to a single term of the form $V_m\cos(\omega t + \theta^0)$ (3marks) b) Draw a phasor diagram showing V_1, V_2 and V_3 and state the phase relationships between each pair of these phasors. (3 marks)	CO_02

4.	In the circuit given below, a) find the complex impedances (2 marks) b) the current in the circuit (1 mark) c) the Active power, Reactive power and Apparent power supplied by the source (3 marks) 	CO_02
5.	a) Explain briefly (in 1-2 sentences only) the SET and RESET state of a **SR flip flop or SR latch**. Draw the circuit symbol. (3 marks) b) Draw the output waveform (Q) for a **NEGATIVE edge triggered D flip flop**. (3 marks) The input waveforms of the D flip flop are given below. 	CO_03