Ex. No.: 6 **Date:10.09.2020**

Design of Half Adder and Full Adder Circuits

Aim:

To get the stimulated waves of half adder and full adder and verify it with theoretical values.

Apparatus/Tool required:

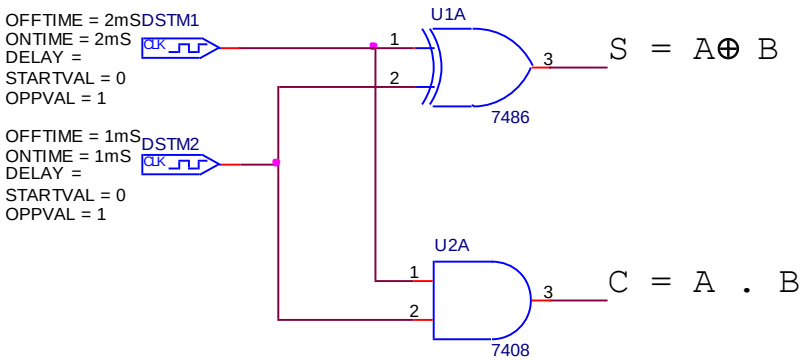
ORCAD / PSpice simulator - > **7400 Library – 7408, 7432 & 7486**
Source Library - Digclock

Simulation Settings: **Analysis Type - Time Domain**

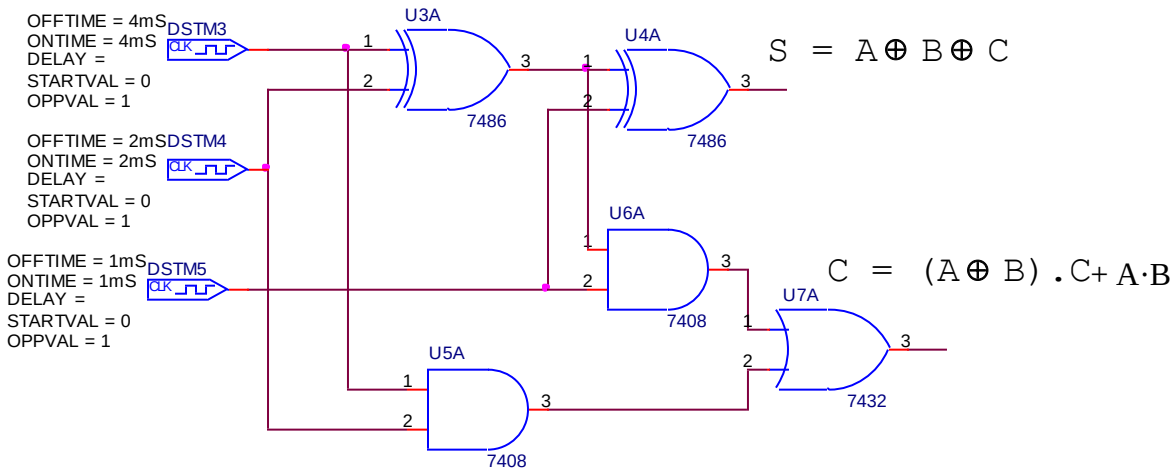
Run to time: 4ms (for Half Adder)
Run to time: 8ms (for Full Adder)

Circuit Diagram:

Half – Adder Circuit

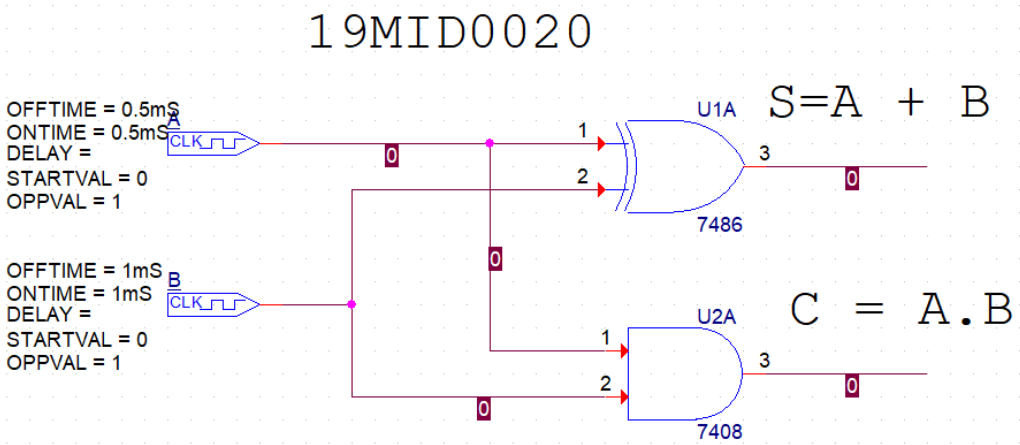


Full – Adder Circuit



Theory:

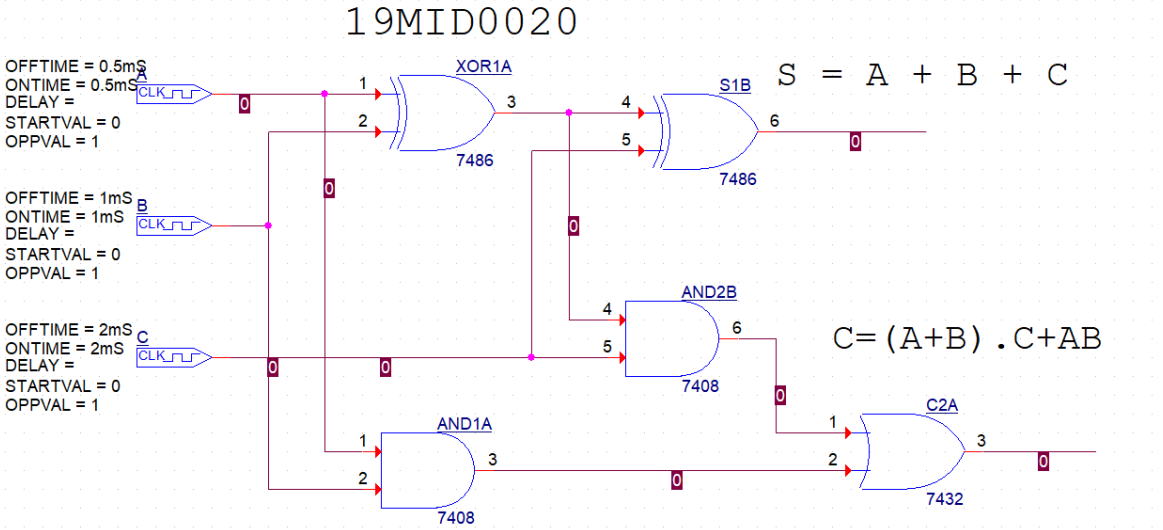
Half Adder Circuit:



Truth Table

A	B	S=A⊕B	C=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder Circuit

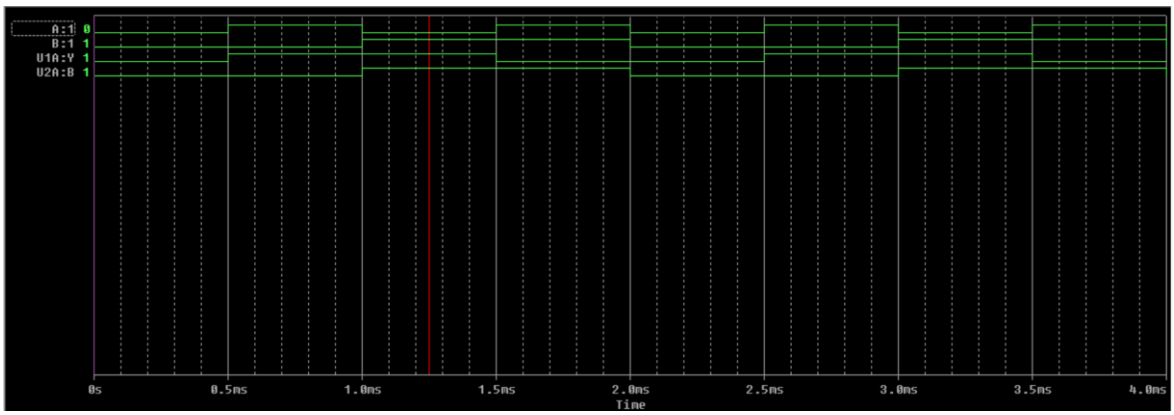


Truth Table

A	B	C	S=A⊕B⊕C	C= (A⊕B).C+A.B
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simulation Circuit Diagram and Output (Both Waveform and Truth Table):

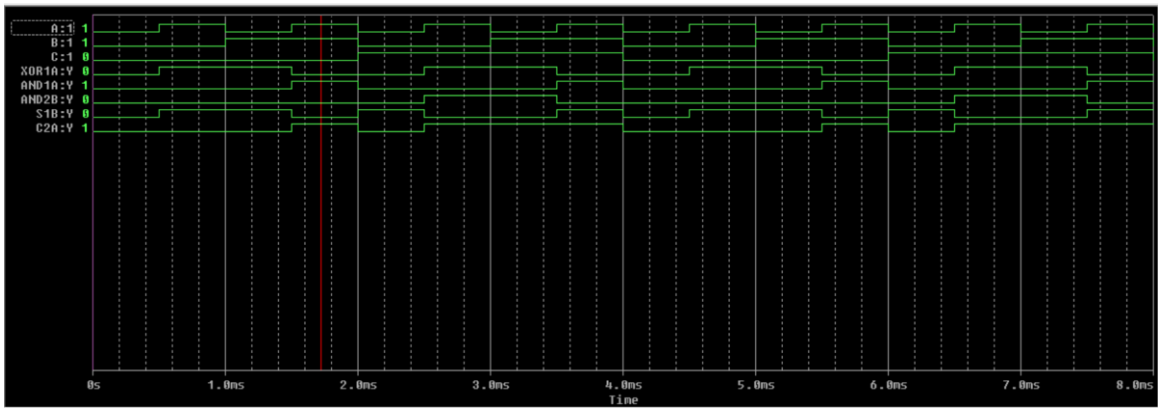
Half – Adder



Half adder:

A	B	S ⇒ A ⊕ B	C ⇒ A·B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full – Adder



Full adder:

A	B	C	A⊕B	S→ A⊕B⊕C	A⊕B·C	AB	C
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	1	0	0	0
0	1	1	1	0	1	0	1
1	0	0	1	1	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	0	0	1	1
1	1	1	0	1	0	1	1

Procedure:

i. Draw the circuit diagram for half adder using the software ORCAD PCB DESIGNER LITE(offtime&ontime(1)=2ms ;offtime&ontime(2)=1ms)
ii. Place the voltage markers at the respective outputs
iii. Create netlist and new simulation profile
iv. Run the circuit
v. Similarly draw the circuit diagram for full adder(offtime&ontime(1,2,3)=4ms;2ms;1ms)
vi. Place the voltage markers at the respective outputs
vii. Create netlist and new simulation profile
viii. Run the circuit

Libraries needed: 7400

Source:digclock

Analysis type : time domain

Run to time (for half adder): 4ms

Run to time (for full adder):8ms

Result:
The theoretical values and the simulated results are same for both half and full adders

Inference:
Hence the theoretical values and stimulated results are verified.

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