3 – Bus system Architecture

✓ Microprocessor is a very simple machine that endlessly follows the sequence

1. Fetch the next instruction in sequence from memory
2. Execute the instruction
3. Go to step 1.

✓ Fetch – Memory read operation
↳ Byte or word pointed by PC is transferred from memory to the instruction register in the CPU.

✓ Execution – requires additional memory reads – include a memory write, an I/O read, an I/O write, an internal CPU activity.

✓ In all, there are 5 unique operations or bus cycles Possible

1. Memory read
2. Memory write
3. I/O read
4. I/O write
5. Bus idle [not requiring access to memory or I/O]

✓ 3 sets of wires (or buses)
↳ Transfer of data between the CPU and the memory and I/O units.

✓ Look at the timing between the address data and control buses for each of the (active) bus cycle types.

Bus cycle Timing

- ✓ Shows bus cycle timing for the 4 active bus cycle types.
- ✓ Each cycle begins with the output of memory or I/O port address during the T1 clock cycle
- ✓ The parallel lines indicate that some of the lines are assumed to be high and others low.
- ✓ Examining the address lines only it is not possible to determine if this is a memory or an I/O address.
- ✓ unable to tell the direction of the data flow
- ✓ Therefore control bus is required
- ✓

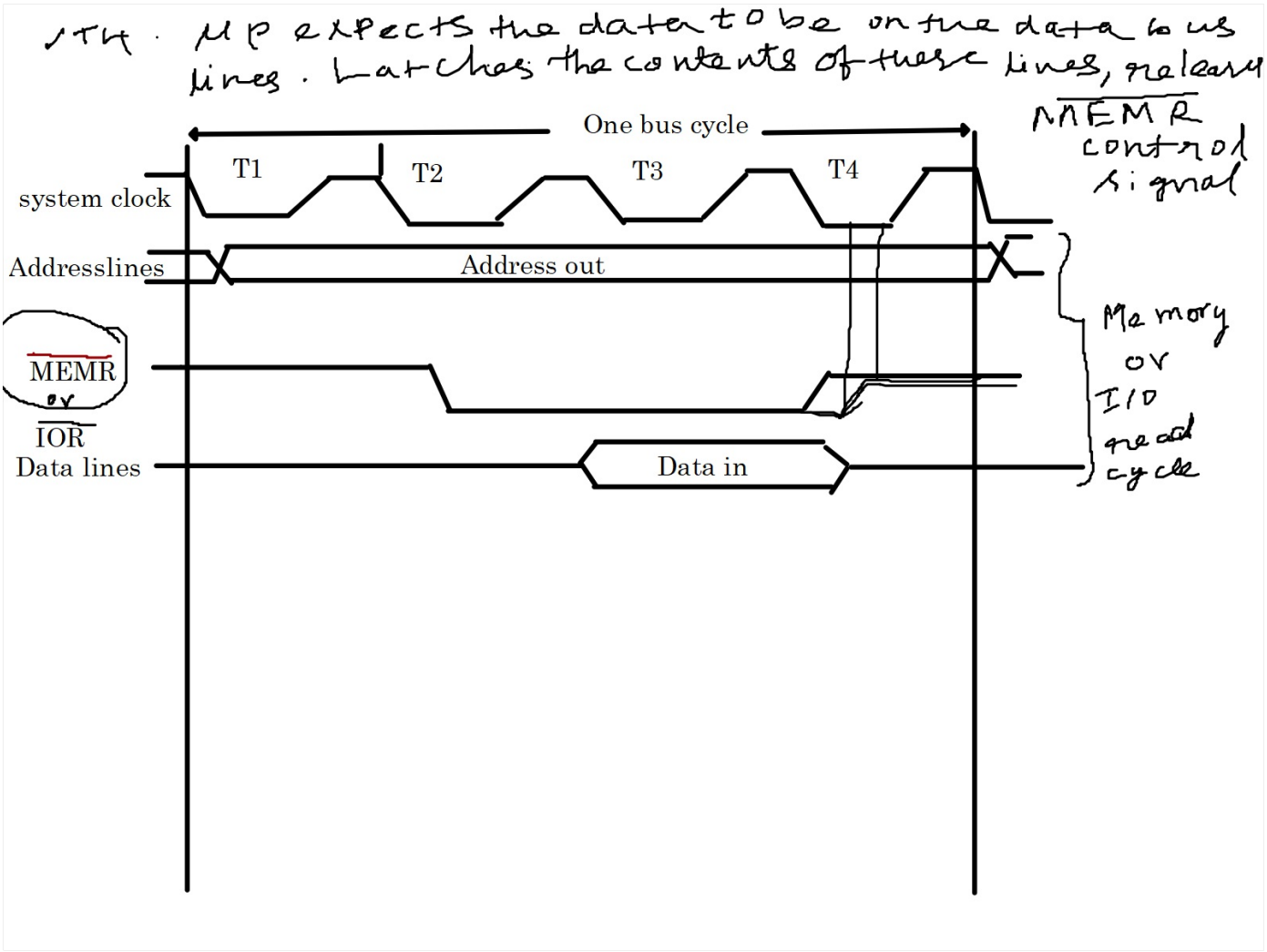
✓ This bus consist of 4 active-low signals

1. $\overline{MEMR}$
2. $\overline{MEMW}$
3. $\overline{IOR}$
4. $\overline{IOW}$

✓ T1. Processor outputs 20 bit address

✓ T2. The $\overline{MEMR}$ control line is driven low.
→ Memory unit recognizes this bus cycle as a memory read
→ Prepares to place addressed byte or word onto the data lines.

✓ T3. MP configures its data bus lines for input. 'Look up' the data byte or word


T4. MP expects the data to be on the data bus lines. Latches the contents of these lines, releases
One bus cycle
T1
T2
T3
T4
system clock
Addresslines
Address out
MEMR
or
IOR
Data lines
Data in
MEMR control signal
Memory or I/O read cycle