TABLE 2.2 ADDRESSING MODES OF THE 8086/88 MICROPROCESSOR

Addressing mode	Coding example: Object code	Mnemonic	Segment for memory access	Symbolic operation	Description
Immediate	B8 00 10	MOV AX,1000H	Code	AH ← 10H; AL ← 00	Source of data is within instruction
Register	8B D1	MOV DX,CX	Within CPU	DX ← CX	Source and destination of data are CPU registers
Direct	8A 26 00 10	MOV AH,[MEMBDS][a]	Data	AH ← [1000H]	Memory address is supplied within the instruction
Register indirect	8B 04	MOV AX,[SI]	Data	AL ← [SI]; AH ← [SI + 1]	Memory address is supplied in an index or pointer register
	FF 25	JMP [DI]	Data	IP ← [DI + 1:DI]	
	FE 46 00	INC BYTE PTR[BP][b]	Stack	[BP] ← [BP] + 1	
	FF 0F	DEC WORD PTR[BX][b]	Data	[BX + 1:BX] ← [BX + 1:BX] − 1	
Indexed	8B 44 06	MOV AX,[SI + 6][c]	Data	AL ← [SI + 6]; AH ← [SI + 7]	Memory address is the sum of the index register plus a displacement within the instruction
	FF 65 06	JMP [DI + 6][c]	Data	IP ← [DI + 7:DI + 6]	
Based	8B 46 02	MOV AX,[BP + 2][c]	Stack	AL ← [BP + 2]; AH ← [BP + 3]	Memory address is the sum of the BX or BP base registers plus a displacement within instruction
	FF 67 02	JMP [BX + 2][c]	Data	IP ← [BX + 3:BX + 2]	
Based and indexed	8B 00	MOV AX,[BX + SI]	Data	AL ← [BX + SI] AH ← [BX + SI + 1]	Memory address is the sum of an index register and a base register
	FF 21	JMP [BX + DI]	Data	IP ← [BX + DI + 1:BX + DI]	
	FE 02	INC BYTE PTR[BP + SI][b]	Stack	[BP + SI] ← [BP + SI] + 1	
	FF 0B	DEC WORD PTR[BP + DI][b]	Stack	[BP + DI + 1:BP + DI] ← [BP + DI + 1:BP + DI] − 1	
Based and indexed with displacement	8B 40 05	MOV AX,[BX + SI + 5][c]	Data	AL ← [BX + SI + 5] AH ← [BX + SI + 6]	Memory address is the sum of an index register, a base register, and a displacement within instruction
	FF 61 05	JMP [BX + DI + 5][c]	Data	IP ← [BX + DI + 6:BX + DI + 5]	
	FE 42 05	INC BYTE PTR[BP + SI + 5][b,c]	Stack	[BP + SI + 5] ← [BP + SI + 5] + 1	
	FF 4B 05	DEC WORD PTR[BP + DI + 5][b,c]	Stack	[BP + DI + 6:BP + DI + 5] ← [BP + DI + 6:BP + DI + 5] − 1	

Strings	A4	MOVSB	Extra,Data	[ES:DI] ← [DS:SI]
				If DF = 0, then
				SI ← SI + 1; DI ← DI + 1
				If DF = 1, then
				SI ← SI − 1; DI ← DI − 1
					The memory source address is register SI in the data segment, and the memory destination address is register DI in the extra segment

[a]MEMBDS is assumed to point at location 1000H in the data segment. The brackets are optional.

[b]BYTE PTR and WORD PTR avoid the ambiguity of byte or word access.

[c]The displacement is added to the pointer or base register as a 2's-complement signed binary number.