RSG3 No. 11

# VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Authorization Seal

## Test : CAT- I / CAT- II / Mid-Term

Register No.: 19MID0020

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Programme : Int M.Tech Data Science School : SCOPE

Slot : F1 Session : FN/AN/EVN

Course Code: CSI 2006 Class NBR: VL2021220502134

Course Title: MICROPROCESSOR AND INTERFACING

Faculty Name : Prof. : Mr. P Naresh

Date of Exam : 1/4/22 No.of pages written : 11

Signature of the Invigilator : 1/4/22

Name / Emp. ID of the Invigilator : 11976

S. Prashanth.
Signature of the Student

| Q No. | Marks | Q No. | Marks | Q No. | Marks | Q No. | Marks | Q No. | Marks |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 09 | 9 | | 17 | | 25 | | 33 | |
| 2 | 08 | 10 | | 18 | | 26 | | 34 | |
| 3 | 08 | 11 | | 19 | | 27 | | 35 | |
| 4 | 08 | 12 | | 20 | | 28 | | 36 | |
| 5 | 08 | 13 | | 21 | | 29 | | 37 | |
| 6 | | 14 | | 22 | | 30 | | 38 | |
| 7 | | 15 | | 23 | | 31 | | 39 | |
| 8 | | 16 | | 24 | | 32 | | 40 | |
| Sub-Total | 41 | Sub-Total | | Sub-Total | | Sub-Total | | Sub-Total | |

Grand Total Marks :

Evaluator's Signature

Date : .....

Evaluator's Name : Prof. .....

Marks In Words .....

2) 8251 A [UART]

A → 65
B → 66
C → 67
D → 68
E → 69
F → 70
G → 71
H → 72
I → 73
J → 74
K → 75
L → 76
M → 77
N → 78

↳ transmitter
↳ even parity enabled
↳ 2 stop bits
↳ 8 bit character length
↳ frequency ⇒ 160 KHz
↳ Baud rate ⇒ 10 k

String

HICROPROCESSOR

2000 to 5000H

H ⇒ 77

$(77)_{10}$ ⇒

*) Baud rate index:

| $D_1$ | $D_0$ | |
|---|---|---|
| 0 | 0 | → X |
| 0 | 1 | → 2 |
| ✓ 1 | 0 | → 16 |
| 1 | 1 | → 64 |

Baud rate index } Frequency / Baud Rate ⇒ $\frac{160 \times 10^3}{10 \times 10^3}$ ⇒ 16

*) Stop bits

| $D_7$ | $D_6$ | |
|---|---|---|
| 0 | 0 | → X |
| 0 | 1 | → 1 bit |
| 1 | 0 | → 1½ bit |
| ✓ 1 | 1 | → 2 bit |

*) String character:

| $D_3$ | $D_2$ | |
|---|---|---|
| 0 | 0 | → 5 bit |
| 0 | 1 | → 6 bit |
| 1 | 0 | → 7 bit |
| ✓ 1 | 1 | → 8 bit |

Control word format

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

F E

*) Parity Enable / Disable

↳ $D_4$ ⇒ 0

✓ $D_4$ ⇒ 1

*) Even Parity / Odd Parity

↳ $D_5$ = 0

✓ $D_5$ = 1

ALP program to transmit the data:

| DS | ST |
|---|---|
| 2000 | 5000 |

```
START : MOV AX, @2000
        MOV DS, [redacted] AX      DS => Data segment
                                   SI => Segment Register.
        MOV SI, 5000

        MOV CL, [redacted],64H
        MOV AL, FE

        OUT 70H, FEH
        MOV AL, 11H

WAIT :  IN AL, 70H
        AND AL, 01H
        JZ WAIT
```

| CL | AL | 70H |
|---|---|---|
| 64 | ~~FE~~ 11H | FE |

Every character is waiting
even => loops on looping

[Jump if equal to zero]

dd => ready to transmit

```
        MOV AL, [SI]
        OUT 71H, AL

        INC SI      } Moving to the next character
        DEC CI

        JNZ WAIT    [Jump if Not Equal to zero]
```

Each and every character after waiting it is transmitted.

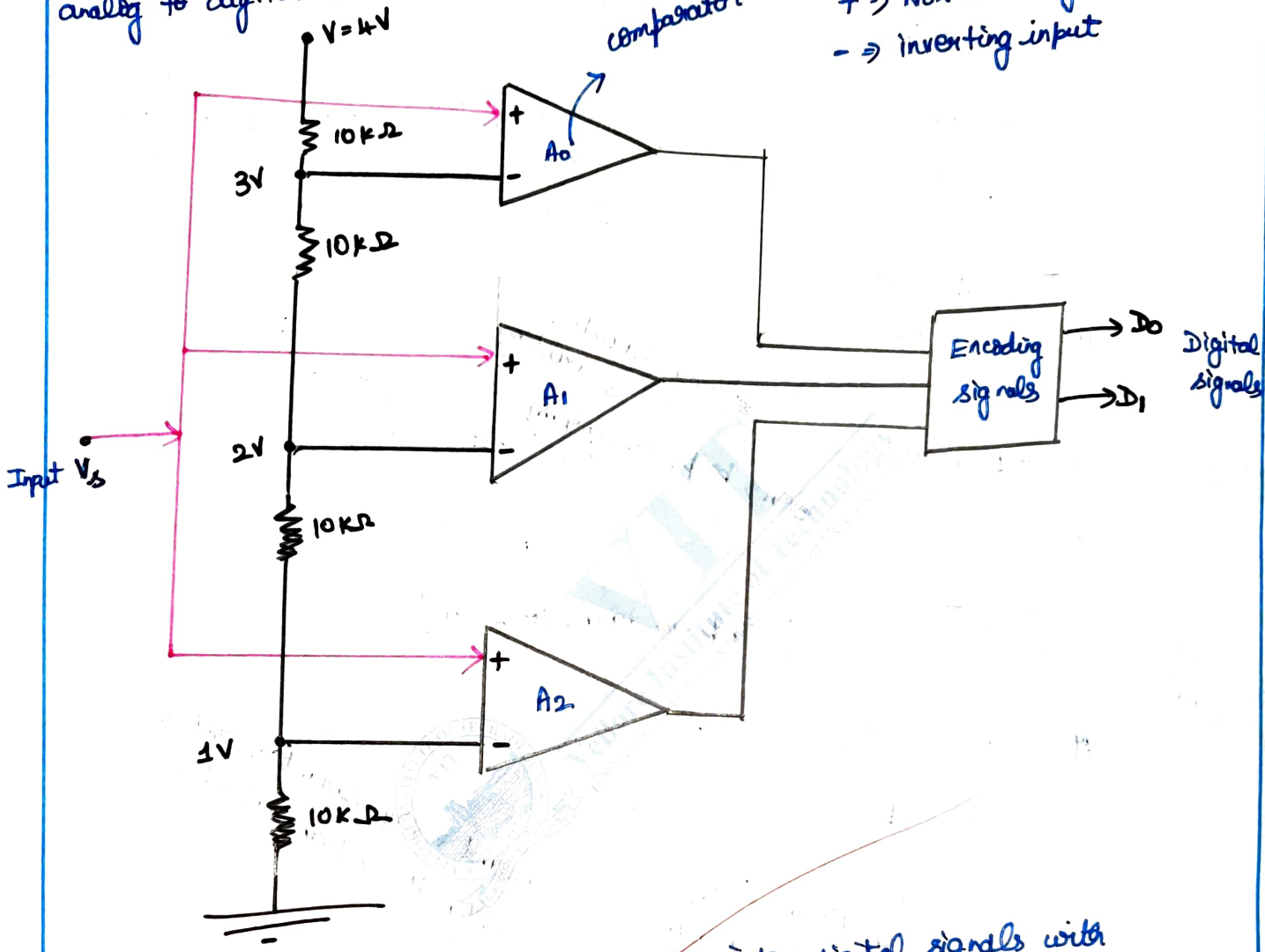
f all characters transmitted

```
        MOV AH, 4CH } Halt the program
        INT 21H

END :   Code END    } End of the program
```

4) Analog to Digital Converter

8255 (Programmable Parallel Port) device is used for these analog to digital conversion.




*) The input ~~digital~~ analog signal is converted into digital signals with the help of voltage divider and the comparator.

*) Input analog signal : non-inverting input of the comparator.

Reference voltage : inverting input of the comparator.

↑ provides

voltage divider

*) The voltage divider is the major and key accept of this conversion.

*) operational amplifier with feed back ⇒ Digital to Analog conversion

*) comparator ⇒ Analog to Digital conversion.

*) The reability and speed of the comparators are quick and rapid which serves those purpose.

*) The reference voltage must be provided with adequate resistors of each 10 KΩ which gives input to inverting input of the comparator.

*) The voltage must be grounded properly.

*) If the incoming input voltage (i.e at Non-inverting input) > reference voltage (inverting input) ; then the comparator remains high.

*) For eg: input voltage is 3V.

3V > 3V ✗ A0 ⇒ low

3V > 2V ✓ A1 ⇒ high

3V > 1V ✓ A2 ⇒ high

5) 8259 Programmable interrupt Controller:

Interrupt:

*) An interrupt is a stop signal / pause signal which is requested by the peripheral devices.

*) These requests will not be sent immediately to the CPU; they will be served by interrupt controllers and they only these interrupt controller requests the CPU.

*) Once the CPU grants ⇒ interrupt occurs

CPU not grant ⇒ No interrupt.

ICW1

| $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| 0 | $A_7$ | $A_6$ | $A_5$ | 1 | LTM | AD | SNGL | IC4 |

1 ⇒ Level triggered
0 ⇒ edge triggered.

1 ⇒ interval of 4 bytes
0 ⇒ interval of 8 bytes

$A_5, A_6, A_7$ interrupt signals.

0 ⇒ ICW4
1 ⇒ ICW1

1 ⇒ single mode
0 ⇒ cascaded mode.

ICW2

| $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| 1 | $T_7$ | $T_6$ | $T_5$ | $T_4$ | $T_3$ | $A_{10}$ | $A_9$ | $A_8$ |

## ICW3

- Master Mode

| $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| 1 | $S_7$ | $S_6$ | $S_5$ | $S_4$ | $S_3$ | $S_2$ | $S_1$ | $S_0$ |

$S_N \Rightarrow 0$ (slave Mode)

$S_N \Rightarrow 1$ (master Mode)

Slave Mode.

| $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | $ID_2$ | $ID_1$ | $ID_0$ |

## ICW4

| $A_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | SFNM | BUF | M/S | AE 0/1 | $\mu$PM |

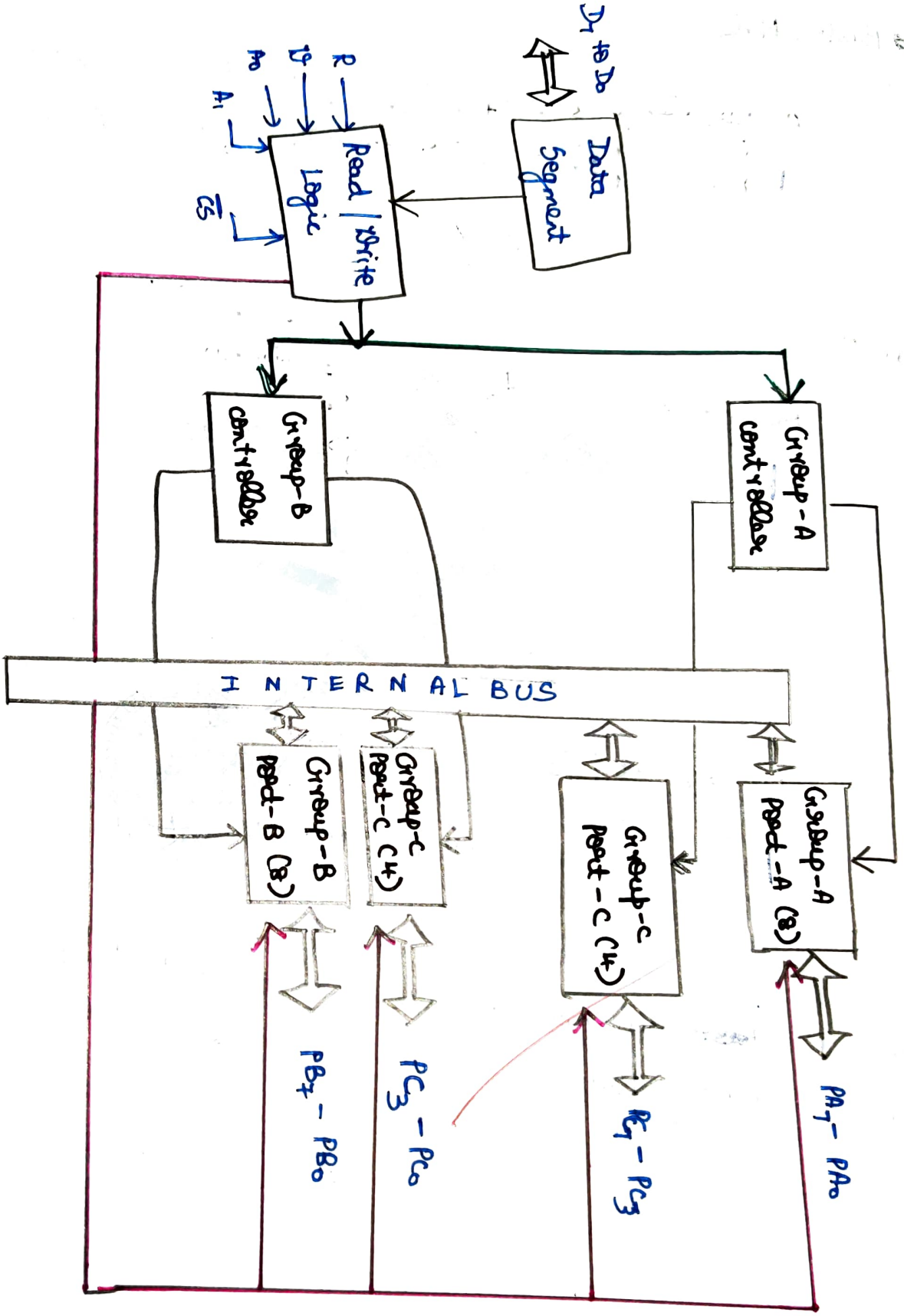
1 ⇒ Master

0 ⇒ slave.

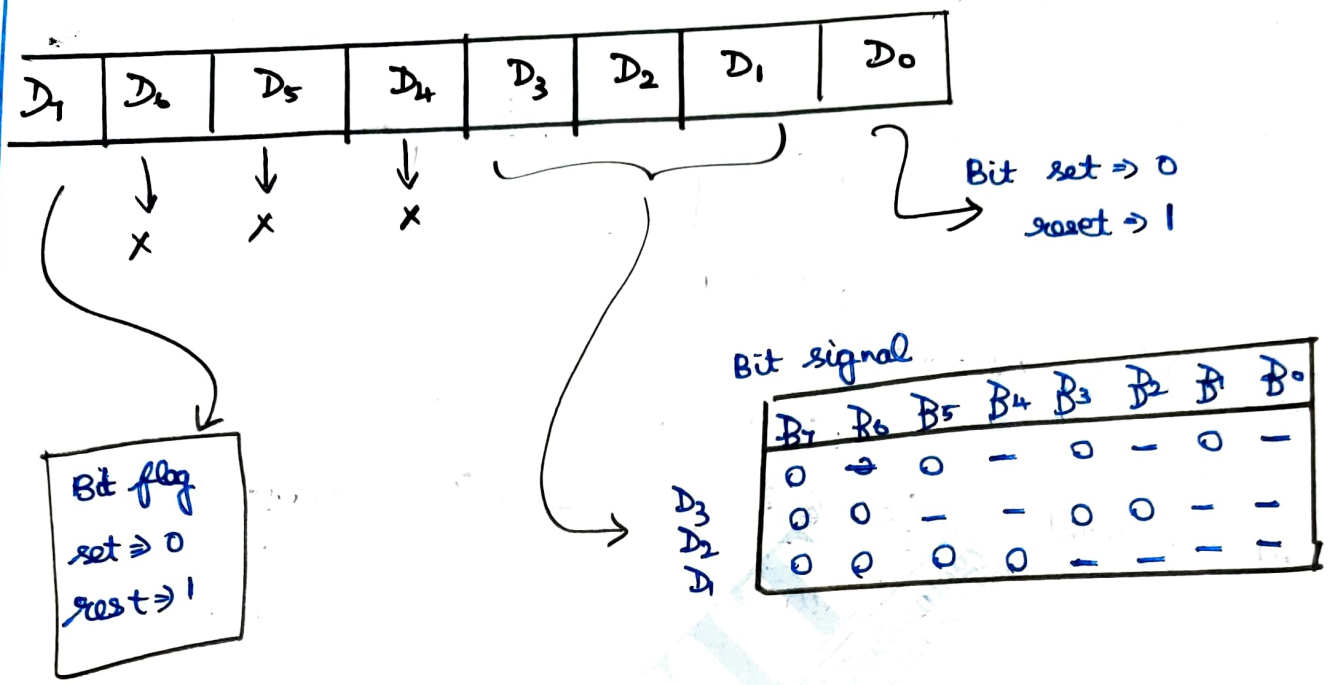
BUF ⇒ 1 ⇒ slave mode

BUF ⇒ 0 ⇒ Master Mode.

3) 8255 programmable parallel Port :



## Bit Set | Rst control word




*) The entire process takes parallely and not sequentially.

+) This indicates that the controllers are independent to each other.

*) Read | Write logic is connected to Group-B and Group A controller.

+) Then it also connected to Group-A ; Group C
Port-A Port-C

then to Group-B ; Group C
Port-B Port-C

*) All the port segments individually receives the infect.

*) These all the signals are carried by the internal bus.

1) ↳ frequence of the timer ⇒ 1.5 MHz

↳ square wave of 3 ms.

Frequency ⇒ $\frac{1}{\text{Time period}}$

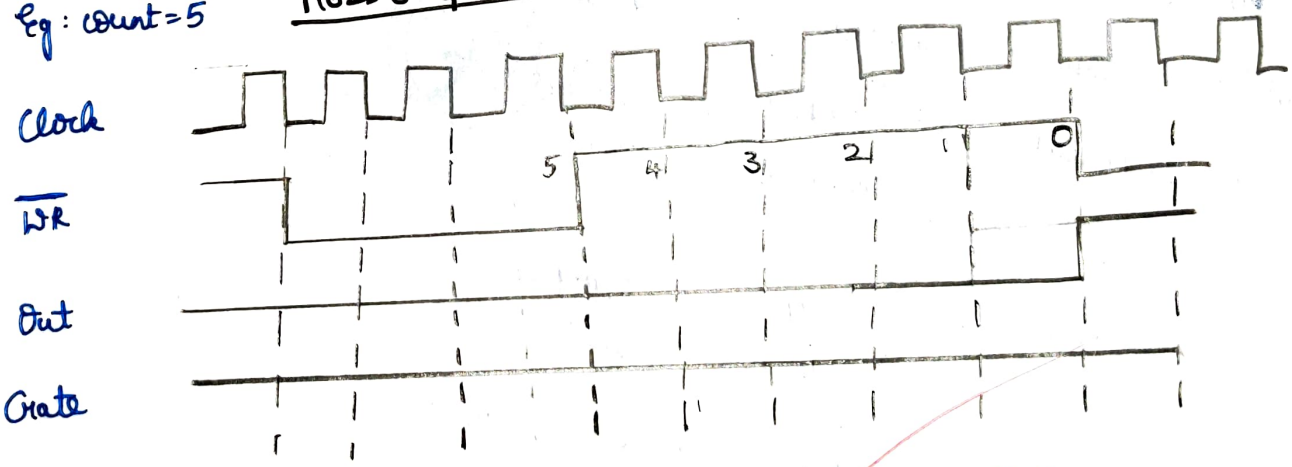
$$T \Rightarrow \frac{1}{F} \Rightarrow \frac{1}{1.5 \times 10^{6}} \Rightarrow 0.66 \times 10^{-6}\ s$$

$$\text{Number of count} \Rightarrow \frac{3 \times 10^{-3}}{0.66 \times 10^{-6}} \Rightarrow 4.54 \times 10^{3} \Rightarrow 4540$$

∴ If the wait is for 3ms; then the counter must go from 4540 to 0.

Eg: count = 5

**MODE 0 operation**



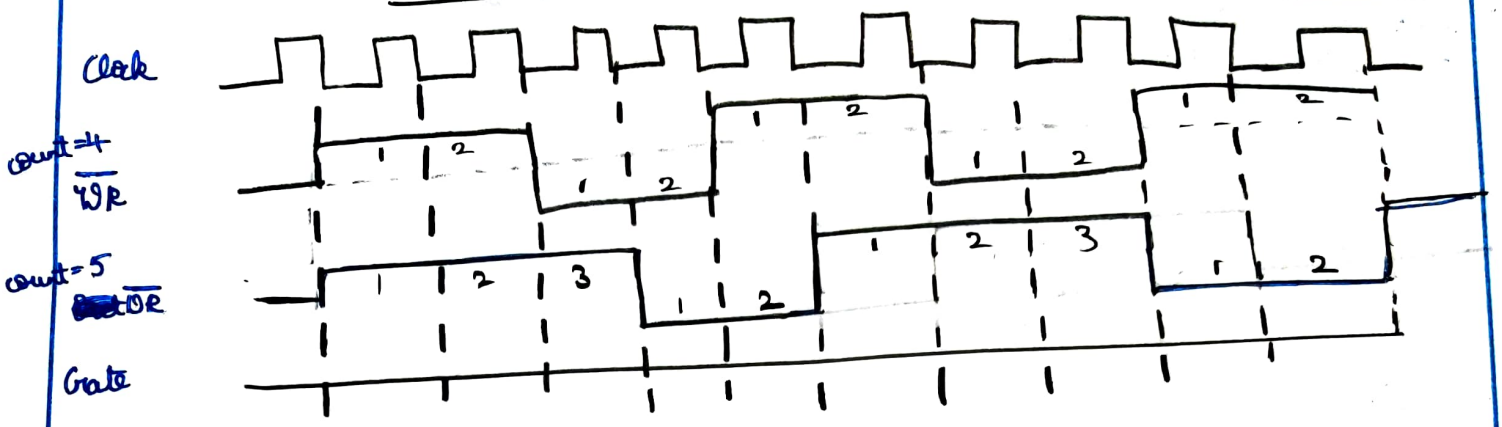

Once $\overline{WR}$ receives 5; it decrements the count from 5 to 0.

the point where $\overline{WR}$ falls to 0; the out is 1 (interrupt occures)

During the entire process Gate must be in high state.

If gate goes to 0; then $\overline{WR}$ will Not decrement

## MODE-1 operation




count=>4 Even than N/2 signals in high and low state $\frac{N-1}{2}$ $\frac{4}{2}$ => L

N+1

count=>5 Odd than $\frac{N-1}{2}$ signals in low state

$\frac{N+1}{2}$ signals in high state

## ALP program

```
START:  MOV AL, 37H
        OUT 46H, AL      → control word register

        MOV AL, 00   }
        OUT 40H, 00  }  LSB   → counter-0

        MOV AL, 15   }
        OUT 40H, 15  }  MSB

        MOV AH, 4CH  }
        INT 21       }  halting the code

END:    Code End
```

counter-0 40H
counter-1 42H
counter-2 44H
counter-3 46H
(control word re