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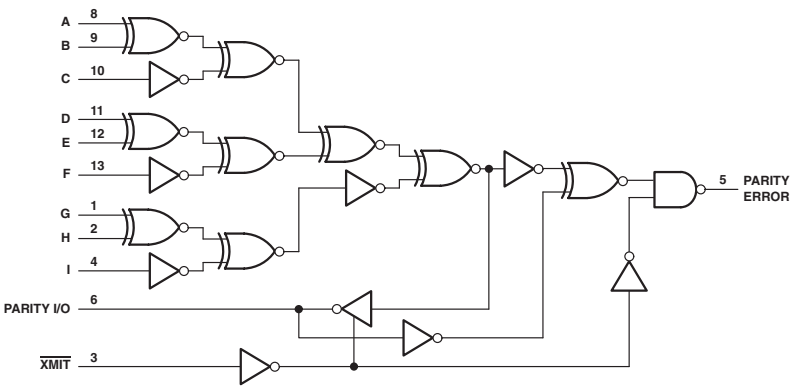
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74AS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74AS)

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h h	h l	H L
1, 3, 5, 7, 9	h h	h l	L H

h = high input level l = low input level
H = high output level L = low output level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
I_{CC}		MAX	50	0.08	0.08	mA
I_{OH}	Parity error	MAX	-2	-24	-24	mA
	Parity I/O	MAX	-15	-24	-24	mA
I_{OL}	Parity error	MAX	20	24	24	mA
	Parity I/O	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11
t_{PLH}	A to I	Parity I/O	MAX	15	9	10.4
t_{PHL}				14	107	12
t_{PLH}	A to I	Parity error	MAX	16.5	10	11.3
t_{PHL}				16.5	12	12.9
t_{PLH}	Parity I/O	Parity error	MAX	9	6.2	7.7
t_{PHL}				9	7.9	9.1
t_{PZH}	$\overline{\text{XMIT}}$	Parity I/O	MAX	13	5.3	7.3
t_{PZL}				16	8.9	11.4
t_{PHZ}				11.5	6.5	8.5
t_{PLZ}				10	6.3	7.8

UNIT: ns