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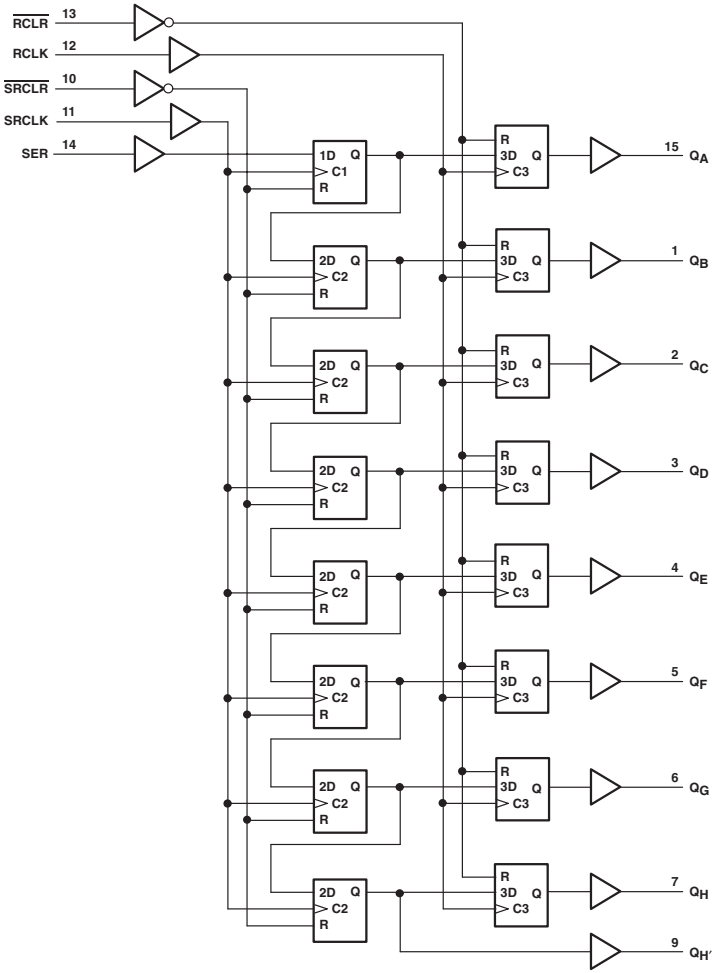
8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}		MAX	65	0.08	0.04	0.02	-	0.02	mA
I_{OH}	QH'	MAX	-1	-4	-4	-4	-6	-12	mA
	Q	MAX	-2.6	-6	-8	-8	-6	-12	mA
I_{OL}	QH'	MAX	16	4	4	4	6	12	mA
	QA to QH	MAX	24	6	8	8	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V
t_w	SRCK			MIN	25	20	5	5.5	5.5	5
	RCK				20	20	5	5.5	5.5	5
t_{su}	$\overline{\text{SRCLR}}$ ↑ to SRCK ↑			MIN	20	10	3.3	3.3	4.8	3.3
	SER to SRCK ↑				20	22	3	3	3.5	3
	SRCK ↑ to RCK ↑				40	22	5	5	8.5	5
	$\overline{\text{SRCLR}}$ ↓ to RCK ↑				40	13	5	5	9	5
	$\overline{\text{RCLR}}$ ↑ to RCK ↑				20	5	3.7	3.8	5.3	3.7
th				MIN	0	5	2	2	1.5	2
t_{PLH}		SRCK ↑	QH'	MAX	18	37	9.1	9.1	12.4	9.1
t_{PHL}					23	37	10.1	10.1	13.9	10.1
t_{PLH}		RCK ↑	QA to QH	MAX	18	37	8.3	8.3	11.1	8.3
t_{PHL}					30	37	9.7	9.7	13.1	9.7
t_{PHL}		$\overline{\text{SRCLR}}$ ↓	QH'	MAX	33	37	10.1	10.1	14	10.1
t_{PHL}		$\overline{\text{RCLR}}$ ↓	QA to QH		57	31	10.7	10.7	14.4	10.7

UNIT: ns