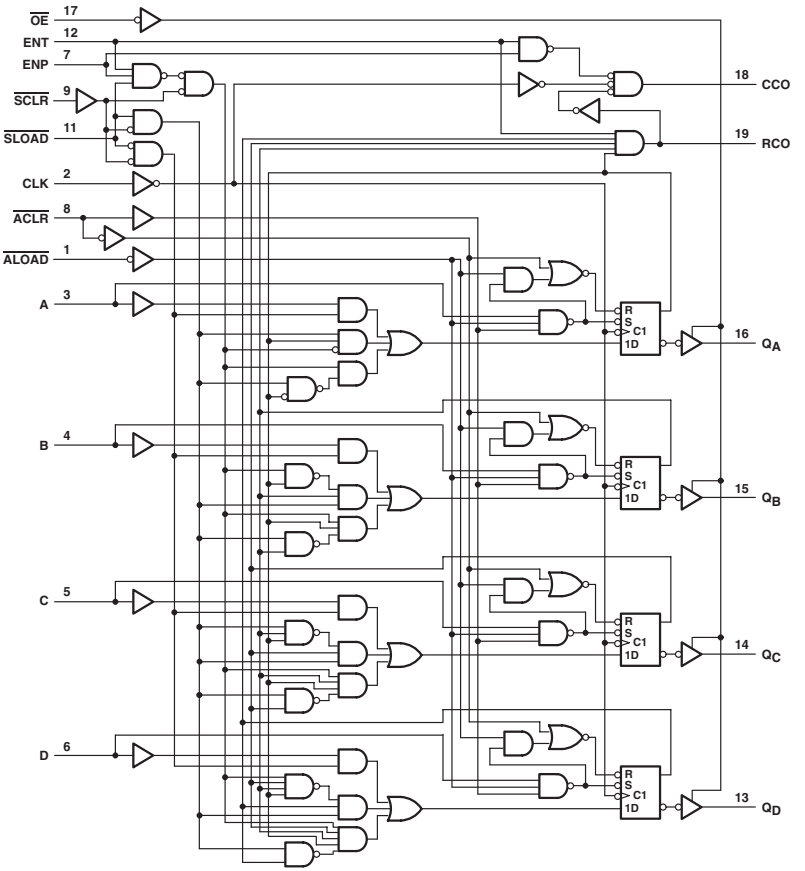
561

SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS								OPERATION
OE	ACLR	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	36	mA
I_{OH}	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO	MAX	-0.4	mA
I_{OL}	OUTPUT Q	MAX	24	mA
	CCO & RCO	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			INPUT	OUTPUT	MAX or MIN	ALS
fmax					MIN	30
tw	CLK "H"				MIN	16.5
	CLK "L"					16.5
tsu	ENP or ENT	H			MIN	20
		L				20
	A, B, C, D					20
	$\overline{SCLR}$	L				15
		H				30
	$\overline{SLOAD}$	L				15
		H				30
th					MIN	0
t_{PLH}			CLK	Q	MAX	12
t_{PHL}						18
t_{PLH}			CLK	RCO	MAX	29
t_{PHL}						24
t_{PLH}			$\overline{ALOAD}$	Q	MAX	35
t_{PHL}						23
t_{PLH}			$\overline{ALOAD}$	CCO	MAX	55
t_{PHL}						33
t_{PLH}			ENT	RCO	MAX	16
t_{PHL}						14
t_{PHL}			$\overline{ACLR}$	Q	MAX	22

UNIT fmax : MHz, other : ns