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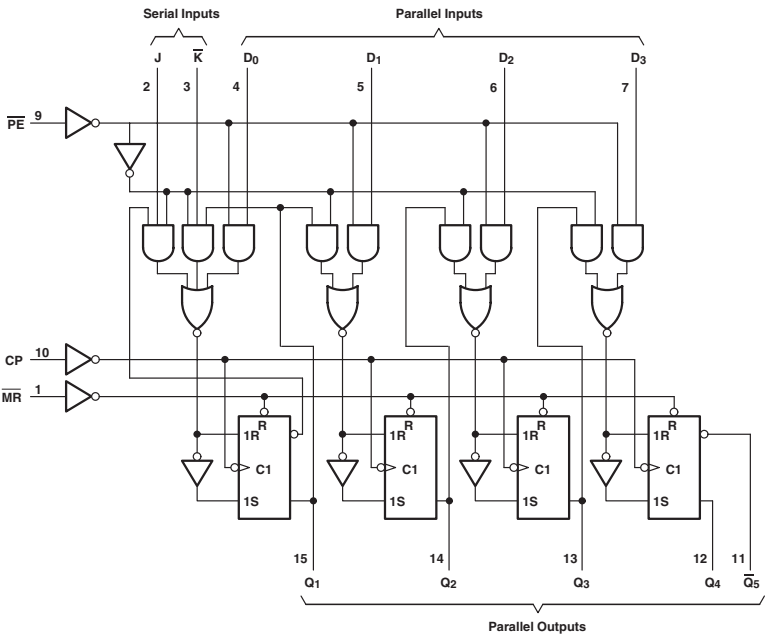
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TRUTH TABLE

OPERATING MODES	INPUTS						OUTPUT				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	dn	d_0	d_1	d_2	d3	$\overline{d2}$

H = High Voltage Level
L = Low Voltage Level,
X = Don't Care
↑ = Transition from Low to High Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,
dn (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	63	21	109	57	0.1	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
fmax				MIN	30	30	70	70	25	20
tw	Clock			MIN	16	16	7	4	20	24
	$\overline{MR}$				12	12	12	7.2	20	24
tsu	$\overline{PE}$			MIN	25	25	11	8	25	30
	Serial & Pararel Data				20	15	5	3.5	25	-
	Clear Inactive Data				25	25	9	6	25	-
TRELEASE				MAX	10	20	6	-	-	-
th				MIN	0	0	3	1	0	3
t_{PHL}		$\overline{MR}$	QA, QD	MAX	30	30	18.5	11.5	38	45
t_{PLH}		Clock		MAX	22	22	12	8.5	36	53
t_{PHL}					26	26	16.5	10.5	36	53

UNIT fmax : MHz, other : ns