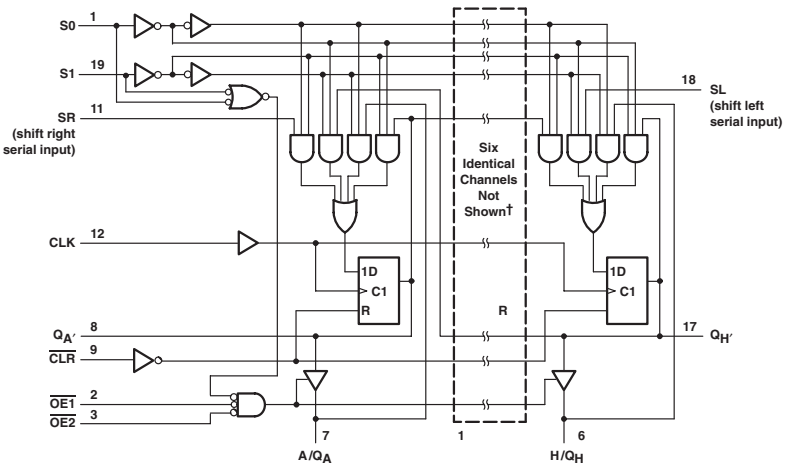
299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	$\overline{OE1}$†	$\overline{OE2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.
† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operationor clearing of the register is not affected.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	53	225	40	95	0.16	0.16	0.16	0.16	mA
I_{OH}	Q_A thru Q_H	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	mA
	$Q_{A'}$ or $Q_{H'}$		-0.4	-0.5	-0.4	-1	-4	-4	-24	-24	
I_{OL}	Q_A thru Q_H	MAX	24	20	24	24	6	4	24	24	mA
	$Q_{A'}$ or $Q_{H'}$		8	6	8	20	4	4	24	24	

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	20	50	30	70	20	16	95	90
tw	CLK (CP) high			MIN	30	10	16.5	7	24	30	5.2	5.5
	CLK (CP) low				10	10	16.5	7	24	30	5.2	5.5
	$\overline{CLR}$ (MR)				20	10	10	7	15	22	5	5
tsu	DATA "H"			MIN	20	7	16	5.5	36	30	4.5	4.5
	DATA "L"				20	5	6	5.5	36	30	4.5	4.5
	SELECT				35	15	20	8.5	36	41	9	9
	$\overline{CLR}$ (MR) INACTIVE				20	10	15	7	-	-	-	-
th	DATA			MIN	0	5	0	2	0	0	0	0
	SELECT				10	5	0	0	0	0	0	0
t_{PLH}		CLK (CD74: CP)	$Q_{A'}$ or $Q_{H'}$ (CD74: Q_0 or Q_7)	MAX	33	20	15	10	60	68	12.9	12.9
t_{PHL}					39	20	18	9.5	60	68	12.9	12.9
t_{PLH}		CLK (CD74: CP)	Q_A thru Q_H (CD74: I/O_0 thru I/O_7)	MAX	25	21	13	10	60	68	13.5	14.5
t_{PHL}					39	21	19	12	60	68	13.5	14.5
t_{PHL}		$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$ (CD74: Q_0 or Q_7)	MAX	40	21	22	10.5	60	69	11.2	12.2
t_{PHL}		$\overline{CLR}$	Q_A thru Q_H (CD74: I/O_0 thru I/O_7)		40	24	22	15	60	69	13.9	18.6
t_{PZH}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	21	18	16	9	47	48	14.9	14.9
t_{PZL}					30	18	22	11	39	45	14.9	14.9
t_{PHZ}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	20	12	8	7	56	56	14.9	14.9
t_{PLZ}					15	12	15	6.5	47	48	14.9	14.9

UNIT fmax : MHz, other : ns