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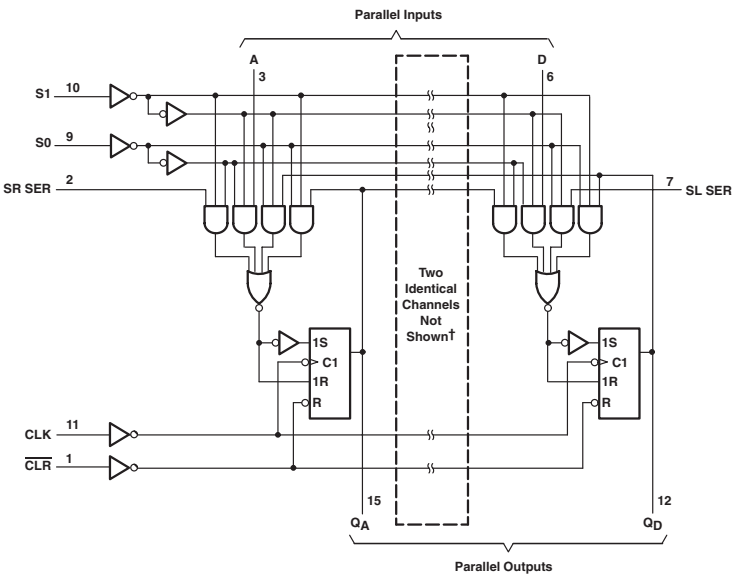
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts

Logic Diagram (SN74)



† I/O ports not shown: Q_B (14) and Q_C (13)

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS										OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	63	23	135	53	0.1	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	70	80	25	20	18
tw	$\overline{CLR}$ ($\overline{MR}$)			MIN	20	20	12	4.5	20	24	24
	CLK (CP) "H"				20	20	7	4	20	24	24
	CLK (CP) "L"				20	20	7	7	20	24	24
tsu	Mode Control			MIN	30	30	11	9.5	25	24	30
	DATA				20	20	5	4	25	21	21
	CLR (MR) INACTIVE				25	25	9	6	-	-	-
th				MIN	0	0	3	0.5	0	0	0
t_{PHL}		$\overline{CLEAR}$ ($\overline{MR}$)	ANY	MAX	30	30	18.5	12	38	42	60
t_{PLH}		CLOCK (CP)	ANY	MAX	22	22	12	7	36	53	56
t_{PHL}					26	26	16.5	7	36	53	56

UNIT fmax : MHz, other : ns