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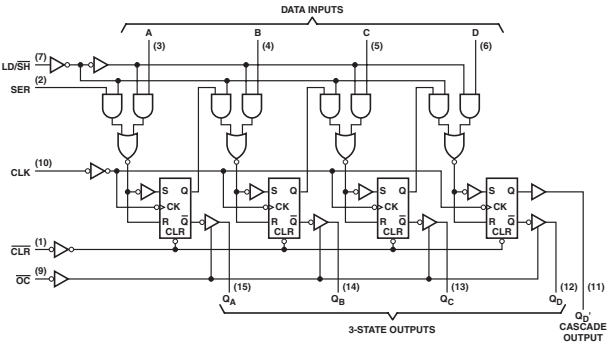
CASCADABLE SHIFT REGISTERS

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)

Logic Diagram



FUNCTION TABLE

INPUTS								3-STATE OUTPUTS				CASCADE
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D	OUTPUT QD
				A	B	C	D					
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{DO}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	34	mA
I_{OH}	QA, QB, QC, QD	MAX	-2.6	mA
	QD'	MAX	-0.4	mA
I_{OL}	QA, QB, QC, QD	MAX	24	mA
	QD'	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
fmax				MIN	30
tw				MIN	16
tsu	LD/SH			MIN	40
	OTHER			MIN	20
th				MIN	10
t_{PLH}		CLK	Q	MAX	30
t_{PHL}				MAX	30

UNIT fmax : MHz, other : ns