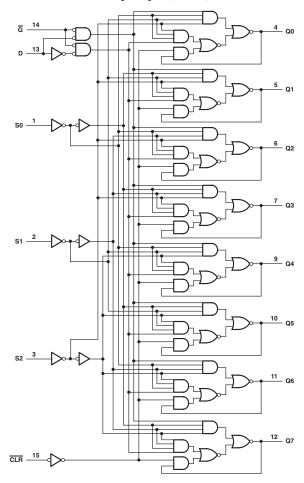
# **8-BIT ADDRESSABLE LATCHES**

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

# Logic Diagram (SN74ALS)



## LATCH SELECTION

LATCH ADDRESSEI	SELECT INPUTS							
ADDITESSEE	Α	В	С					
0	L	L	L					
1	Н	L	L					
2	L	Н	L					
3	Н	Н	L					
4 5	L	L	Н					
5	Н	L	Н					
6	L	Н	Н					
7	н	н	н					

### **FUNCTION TABLE (SN74)**

INPUT	s	OUTPUT OF	EACH	FUNCTION
CLEAR	Ğ	ADDRESSED LATCH	OTHER OUTPUT	FUNCTION
Н	L	D	Qi0	Addressable latch
н	Н	Qi0	Qi0	Memory
L	L	D	L	8-line demultiplexer
L	Н	L	L	Clear

#### ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	90	36	22	0.08	0.16	0.16	mA
Іон	MAX	16	8	8	4	4	4	mA
lor	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

TIMING KEU	OREMENTS AND SWITCHIN	G CHARACTERISTIC	ر.							
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
tw	G (CDHC/HCT: LE)			MIN	15	17	15	20	21	27
	CLR (CDHC/HCT: MR)				15	10	10	20	21	27
tsu	DATA			MIN	15	20	15	19	24	26
	ADDRESS			IVIIIN	5	17	15	19	24	26
th	DATA			MIN	0	0	0	5	0	0
	ADDRESS			IVIIIV	20	0	0	5	0	0
tPLH		CLEAR (CDHC/HCT: MR)	Any Q	MAX	25	18	12	38	47	59
tPHL .		DATA	Any Q	MAX	24	30	19	33	56	59
tPLH .					20	20	12	33	-	59
tPHL .		ADDRESS	Any Q	MAX	28	27	22	50	56	61
tplh					28	20	12	50	-	61
tPHL .		ENABLE	Any Q	MAX	20	24	20	43	51	57
tPHL .					20	24	13	43	-	57
LIBILT										

UNIT: ns