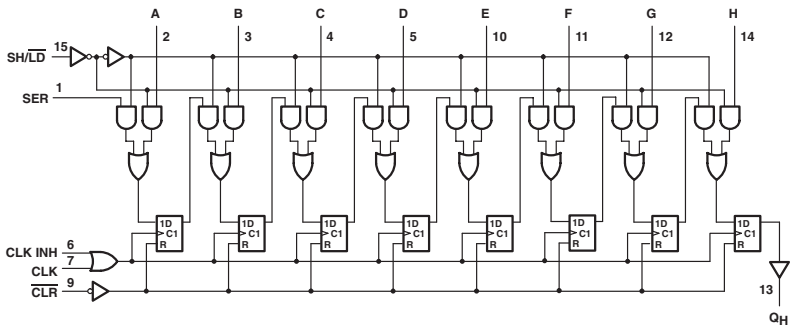
166

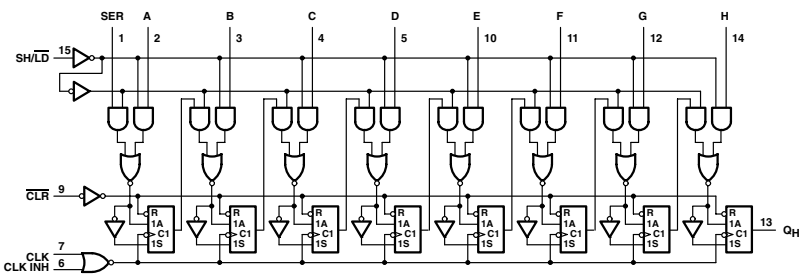
8-BIT PARALLEL-LOAD SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram (SN74LV, HC)



Logic Diagram (SN74ALS, LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{\text{CLEAR}}$	SHIFT/ $\overline{\text{LOAD}}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	8	20	4	4	4	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	25	25	45	110	25	20	16	50	85
tw	CLOCK (CD74: CP)			MIN	20	20	10	3.5	20	24	30	7	4
	$\overline{\text{CLEAR}}$ ($\overline{\text{MR}}$)				20	25	9	4	25	30	53	7	5
tsu	Mode Control			MIN	30	30	16	4	36	44	45	6	4
	DATA				20	20	7	3	20	24	24	6	4.5
th				MIN	0	0	3	0	0	1	0	0	1
t_{PHL}		$\overline{\text{CLEAR}}$	QH	MAX	35	30	14	9.5	30	48	60	18.5	12
t_{PHL}		CLOCK	QH	MAX	30	25	13	14	38	48	60	21.5	13.5
t_{PLH}					26	20	12	9	38	48	60	21.5	13.5

UNIT: fmax : MHz, other : ns