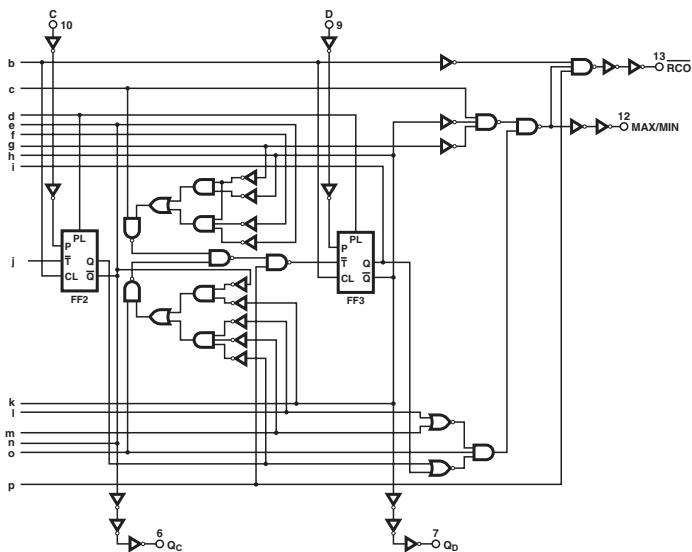
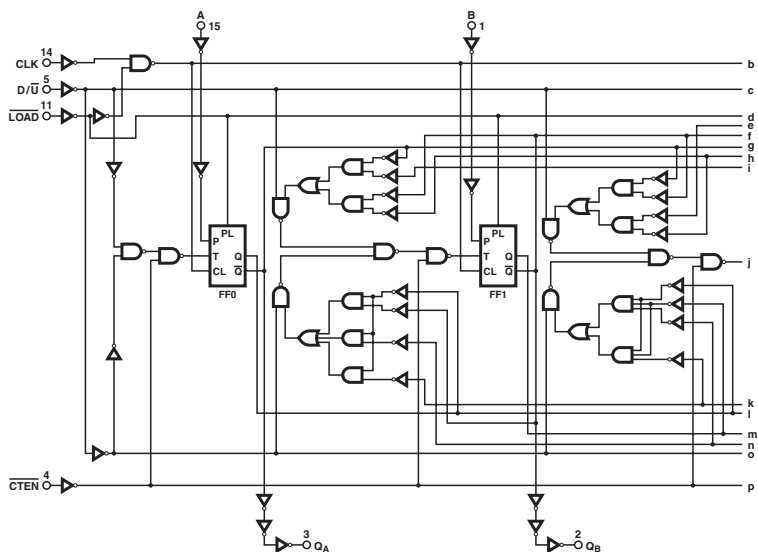




## SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

Logic Diagram




FUNCTION TABLE

INPUTS				FUNCTION
LOAD	CTEN	D/ $\bar{U}$	CLK	
H	L	L		Count up
H	L	H		Count down
L	X	X	X	Asynchronous preset
H	H	X	X	No change

D/ $\bar{U}$  or CTEN should be changed only when clock is high.

X = Don't care

 Low-to-high clock transition

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
I <sub>CC</sub>	MAX	105	35	22	0.08	0.16	mA
I <sub>OH</sub>	MAX	-0.8	-0.4	-0.4	-4	-4	mA
I <sub>OL</sub>	MAX	16	8	8	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
fmax			MIN	20	20	25	17	20
tw	CLK		MIN	25	25	20	30	30
	LOAD			35	35	20	30	24
tsu	Data, high or low		MIN	20	20	20	38	18
th	Data hold time		MIN	0	5	5	5	2
tPLH	LOAD	Q	MAX	33	33	30	66	59
tPHL				50	50	30	66	59
tPLH	DATA	Q	MAX	22	32	21	60	53
tPHL				50	40	21	60	53
tPLH	CLK	RCO	MAX	20	20	20	30	38
tPHL				24	24	20	30	38
tPLH	CLK	Q	MAX	24	24	18	48	51
tPHL				36	36	18	48	51
tPLH	CLK	MAX/MIN	MAX	42	42	31	63	63
tPHL				52	52	31	63	63
tPLH	D/U	RCO	MAX	45	45	37	57	45
tPHL				45	45	28	57	45
tPLH	D/U	MAX/ MIN	MAX	33	33	25	48	50
tPHL				33	33	25	48	50

UNIT f<sub>max</sub> : MHz other : ns