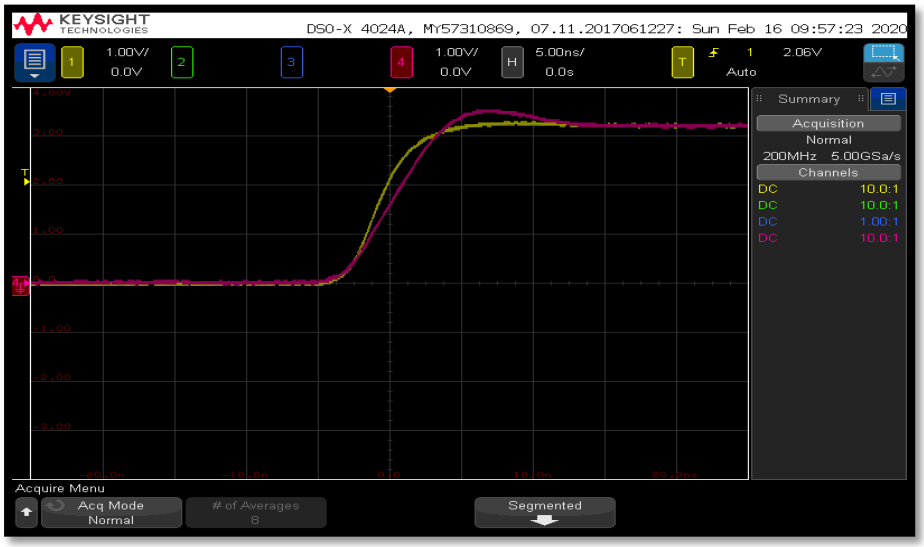
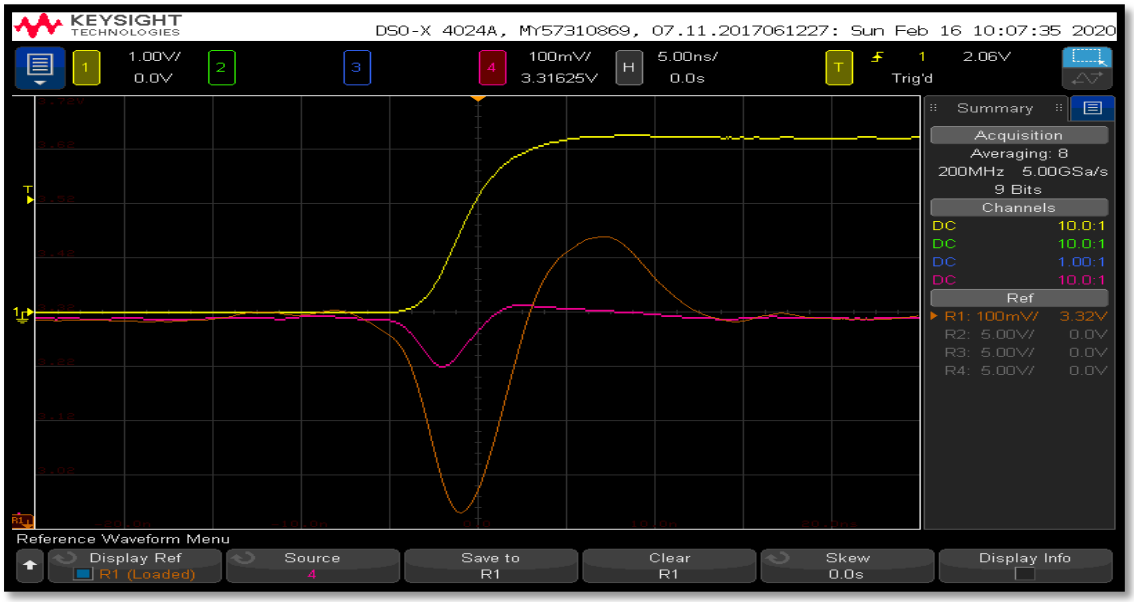
GOAL- : Testing the switching noise on our version of my PCB board

In this case, a 555 timer is used as a clock and two different hex inverter circuits are used , the only difference between those two circuits are having good and bad layout.



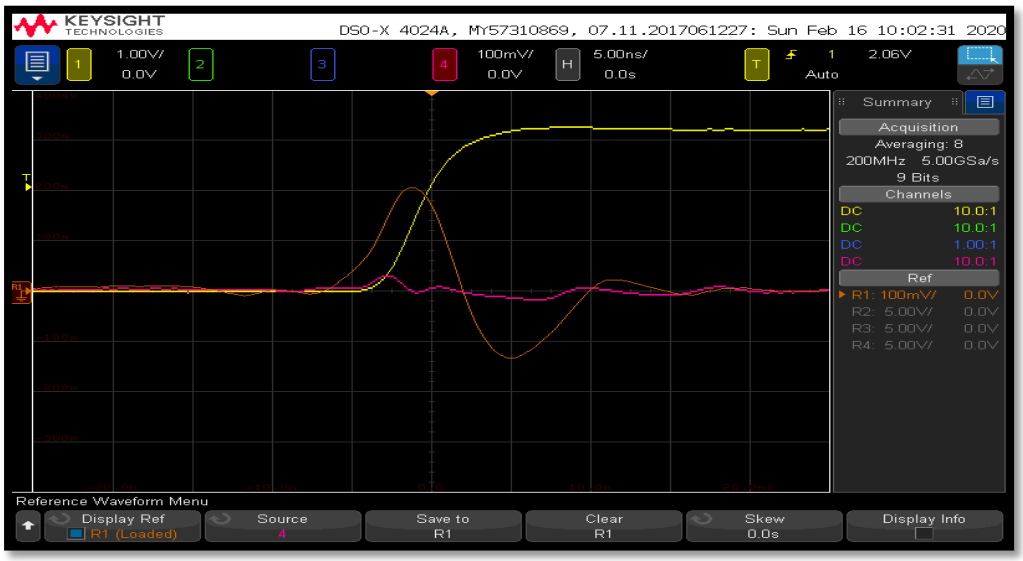
Connecting scope on both the good and bad circuits

The good layout part is having a shorter rise time which means larger di/dt which in turn means that it is having less noise and can be used for further measurements based on good I/O output.



Measured noise on quite high of both circuits in rising edge

This is the switching noise when channel 4 is connected to the bad layout part is taken as reference and then it is connected to the good layout part of the quite high side to check the switching noise. As the decoupling capacitor is connected far from the power pin of the IC in bad layout the switching noise in high signal is much more in bad layout (almost three times)as compared to the good layout.



Measured noise on quite low of both the circuits in rising edge

This is the switching noise when quite low side of the good I/O board is compared with the quite low side of the bad layout. The reason behind high switching noise in the bad layout is due to the absence of solid continuous plane as compared to good layout.