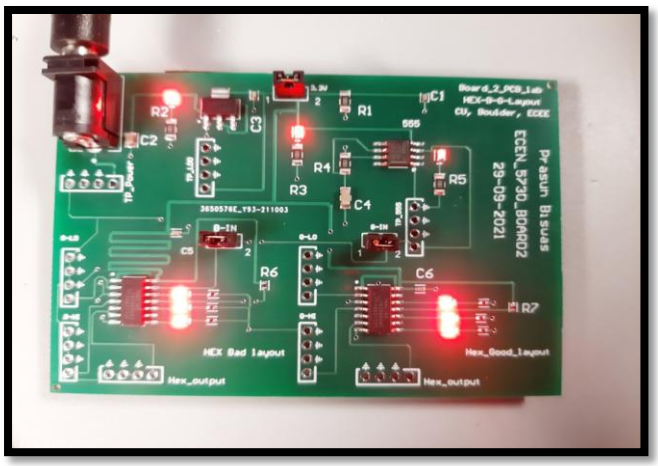
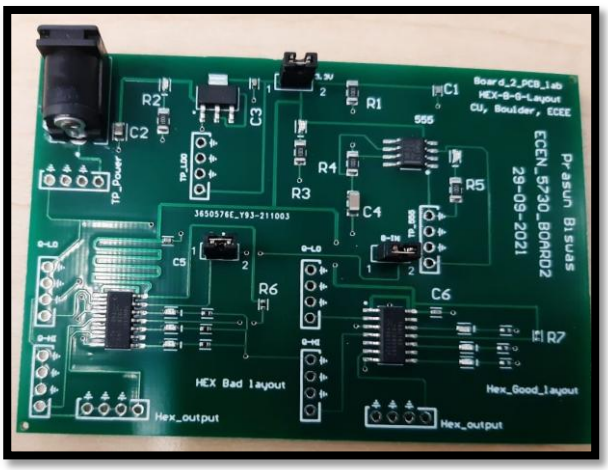
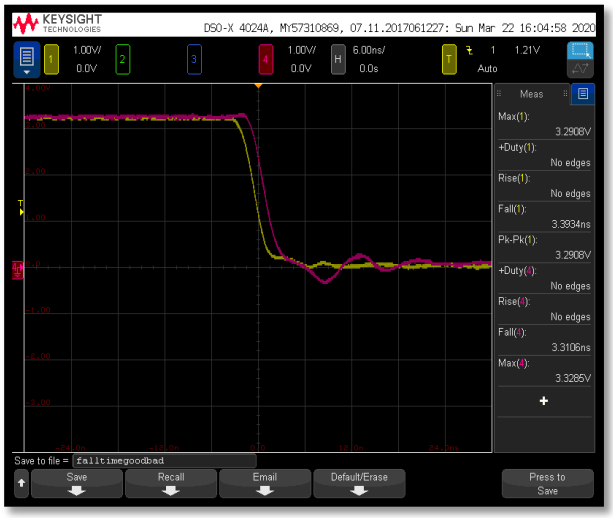
GOAL- Bring up and Test of Board 2





Board powered on

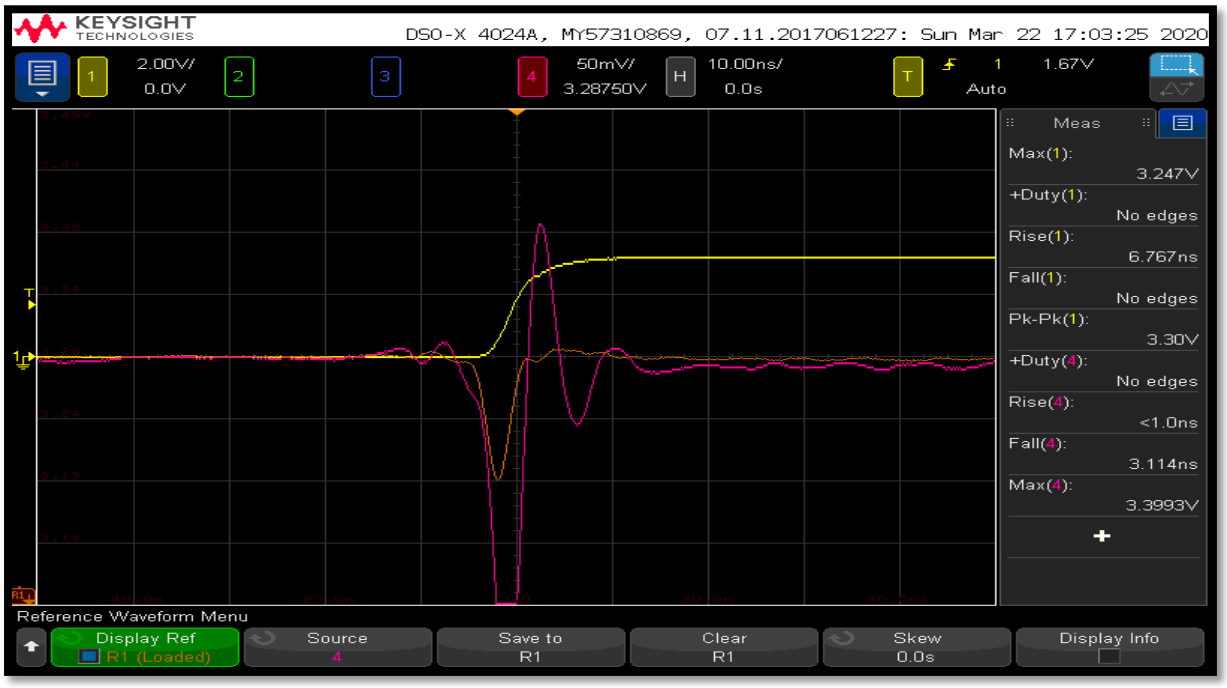


Rise time for both the hex inverter output **Fall time for both the hex inverter output**

The good layout part is having a shorter rise time which means larger di/dt which in turn means that it is having less noise and can be used for further measurements based on good I/O output.

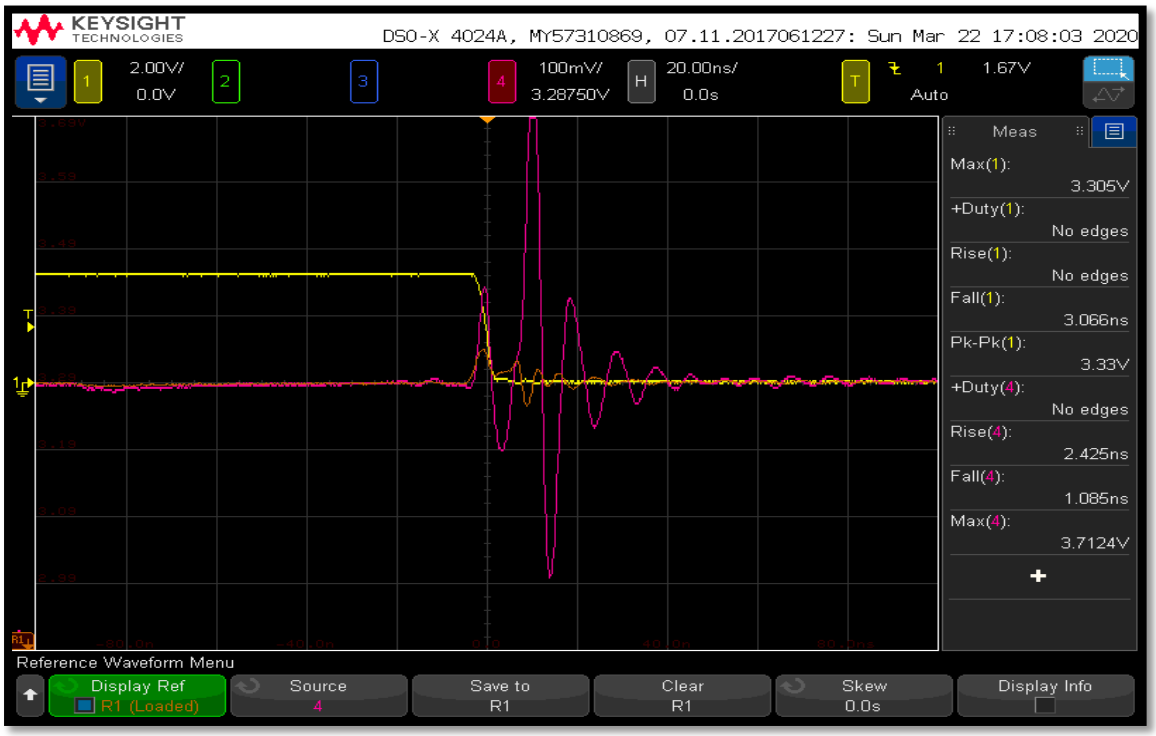
Switching signal for good and bad hex inverters

Fall time switching signal with respect to 555 **Rise time switching signal with respect to 555**

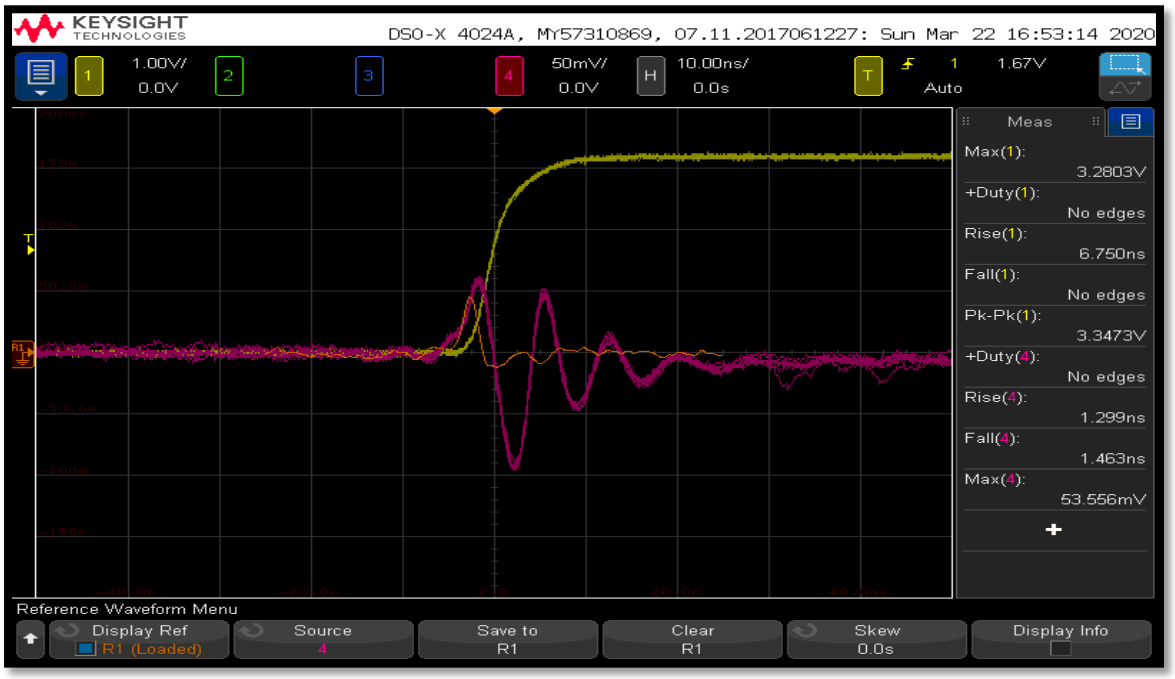


Rise time for quite high signal in with respect to good and hex inverter

Here the rise time of good hex layout is compared with the bad layout of the hex for the quite high side. The part is connected with respect to the 4th channel and good side is taken as the reference and the noise measured is much more as compared to the good layout (almost three times). This is because of the fact that capacitors are placed very far away from the power pin of the IC and it increases the loop inductance of the circuit and finally increasing the noise.

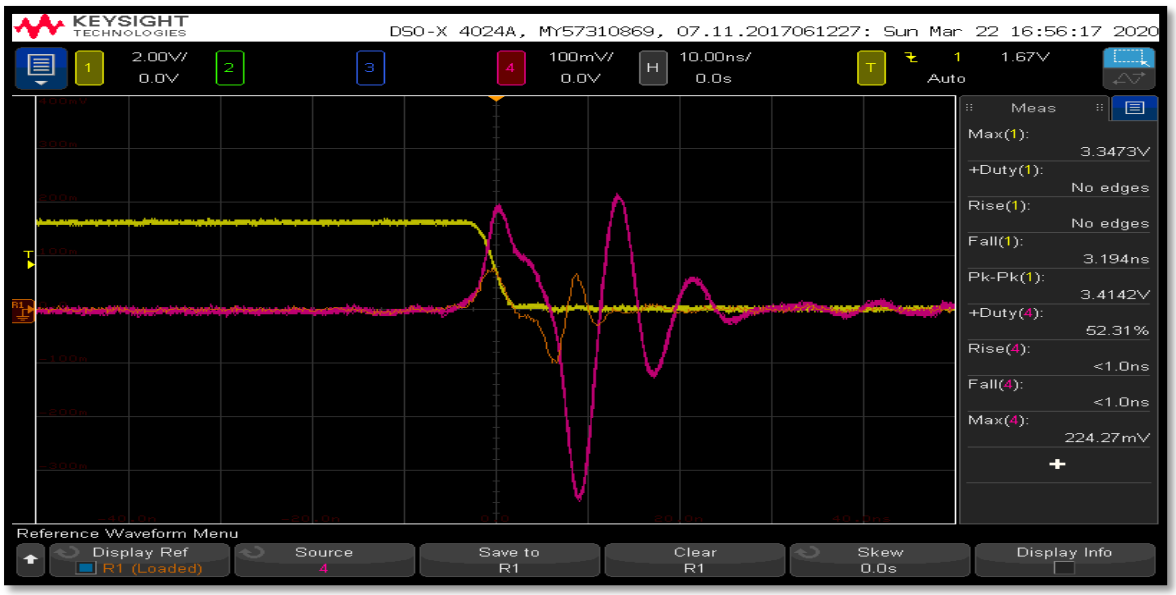


Fall time for quite high signal with respect to good and hex inverter



Rise time quite low signal for good and bad hex inverter

This is the switching noise when quite low side of the good I/O board is compared with the quite low side of the bad layout. Good design scope is taken as reference and the noise can be seen in the bad layout part. The reason behind high switching noise in the bad layout is due to the absence of solid continuous plane as compared to good layout.



Fall time quite low signal with respect to good and bad hex inverters

The seven steps for PCB production-

1. **Completing the plan of record (POR)**

   It was planned beforehand on what to design in this circuit such as the inverters which will be used and which 555 timer type (slow/fast) will be used in this particular board have been checked through the data sheet to make sure all the voltage and current recommendations are good to proceed with. Moreover, where to keep the test points are also being planned to get some required measurements.

2. **Completing the preliminary bill of materials (BOM)**
   The list of materials including capacitors, resistors, LEDs, LDO and power connector, hex inverters, 555 timers are included as the preliminary bill of materials.

3. **Completing the final schematic capture and final BOM**

   Ultimately, the schematic was drawn with the planned approach along with certain changes wherever needed. Later the final BOM was taken from the schematic set itself.

4. **Completing the board layout and order all the parts.**
   After the schematic, the board layout part was completed with as better routing as possible and short traces of the cross under path connections to reduce the noise as much as possible.

5. **Completing the assembly.**

6. **Completing the bring up, troubleshoot, and final test.**

After the board arrived, the final testing part was done with respect to good and bad layout and later also analysed where this board can be improved further with the designing process.

7. **Completing the documentation.**

- ✓ **Recommendations** on to improve my design would be still to make the cross under path much shorter than it is. Routing can be configured in a much better way which would result in shorter cross under paths when needed. This part of the design I believe, can be made much better in my next design which is to plan earlier about routing between circuits and keeping the cross under paths as less or shorter as possible.

- ✓ The **good part** I did was making the bad layout of the circuit bad and good layout much better by which I can compare the results of the two sides much more efficiently. Multiple test points have been placed to get the measurements wherever needed. The test points have also been placed in a similar style so that while measuring using the test probe in real time it doesn't provide any difficulties for the user.