AHMY_SP6LX9_LT Lab Trainer kit Technical Reference

Model No: AHMY_SP6LX9_LT

Doc. Ver.: 01.00

Technical Support:

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Mail. Id: rnd.ahmy@gmail.com

Introduction:

AHMY_SP6_LX9_LT board is an easy to use FPGA Low cost board featuring Xilinx Spartan-6 FPGA. It is specially designed for research, experimenting and learning system design with FPGAs. Spartan®-6 devices are the most cost-optimized FPGAs, offering industry leading connectivity features such as high logic-to-pin ratios, small form-factor packaging, and a diverse number of supported I/O protocols. Built on 45nm technology, the devices are ideally suited for a range of advanced bridging applications found in automotive infotainment, consumer, and industrial automation.

Board Features:

1. FPGA: Spartan-6 XC6SLX9 in TQG144 package
2. Clock & Memory section
   - Processor speed 100 MHZ.
   - Memory
     - 16 MB SPI flash memory for standalone program execution.
3. Interfaces
   - 16 no's of digital input using slide switch
   - 16 no's of user LED
   - One switch provided for manual clock
   - 2 no of input push switches.
   - 16x2 or 20x4 LCD interface
   - On board USB to JTAG programmer (using FT2232 ic).
   - Relay interface
   - Buzzer interface
   - Stepper / DC motor interface driver
   - 4x4 Matrix keypad interface
   - 4 no of 7 segment display
   - Serial communication interface through USB connector.
   - RTC interface with battery pack up option.
   - 128KB serial EEPROM memory
   - External JTAG programmer interface header

4. ADC

- No of ADC input : 2 Channels
- Resolution : 12 bit
- Sampling rate : 50KSPS
- Analog input range : 0 to 3.3V(unipolar)

5. DAC

- No of DAC output : 4 Channels
- Resolution : 12 bit
- Settling time : 6µs
- Analog output range: 0 to +5V

6. Headers

- GPIO pins are terminated in two 20 pins headers
- ADC, DAC, Relay and Stepper/DC motor pins link with phoenix connector
- USB connector for JTAG programming and USB to serial communication
- 10 pin External JTAG header for Programming
- 20 pin headers used to interface 20x4 LCD or 16x2 LCD.

Hardware Details:

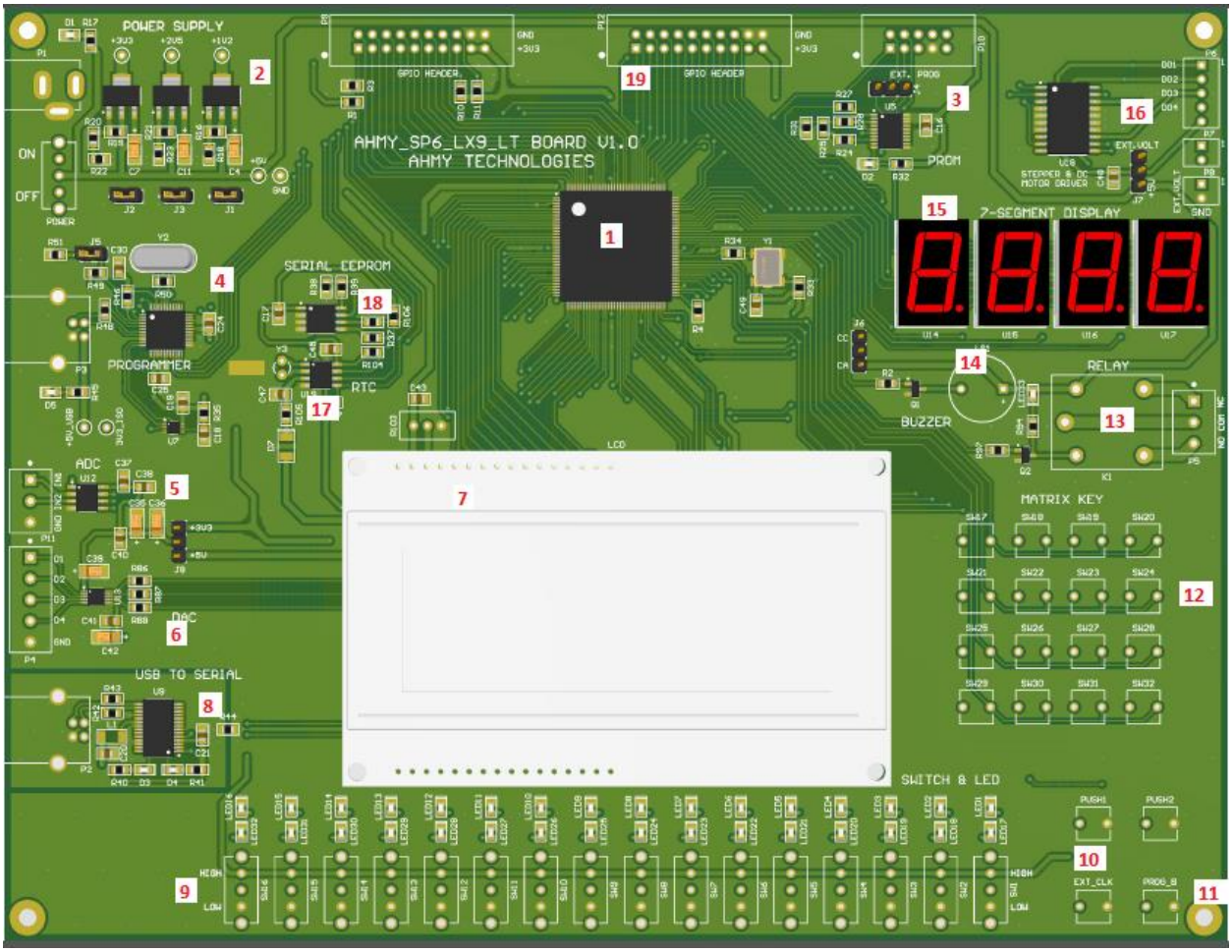


Figure 1 : AHMY_SP6_LX9_LT Board

1. Spartan 6 FPGA XC6SLX9-TQG144
2. Power supply
3. Flash memory for programming
4. FT2232 JTAG Programmer
5. ADC Section
6. DAC Section
7. LCD interface
8. USB to Serial
9. Switch & LED
10. Manual CLK & Up & Down switch
11. RESET Key
12. Matrix Keypad
13. Relay
14. Buzzer
15. 7_Segment display
16. Stepper/DC Motor interface
17. RTC
18. Serial EEPROM
19. Connectors

1. Spartan-6 XC6SLX9-TQG144

Spartan®-6 devices are the most cost-optimized FPGAs, offering industry leading connectivity features such as high logic-to-pin ratios, small form-factor packaging, and a diverse number of supported I/O protocols. This board having,144Pin Spartan-6 FPGA IC. Spartan-6 IC Number of Logic Elements/Cells having 9152, Total RAM Bits is 589824.

2. Power Supply Section:

AHMY_SP6_LX9_LT board operates single +5V build-in SMPS power supply (P1). AHMY_SP6_LX9_LT board has 3 on board voltages regulator. Its convert 5V input into +3.3V, +2.5V and +1.2V. All the voltages connected to Jumper for testing purpose (+3.3V – J2, +2.5V, J1 - +1.2V). Board ON and OFF is controlled by SPDT slide switch (Power)

3. PROM & Clock

AHMY_SP6_LX9_LT board support XCF4xx (optional) Xilinx PROM (4MB) and M25P/W25Q serial EEPROM for standalone program execution. D2 LED connected to FPGA DONE pin, it's indicate the Program execution status.

AHMY_SP6_LX9_LT board operates 100MHz clock speed from on board external clock source. Clock speed controlled by program with clock divide logic.

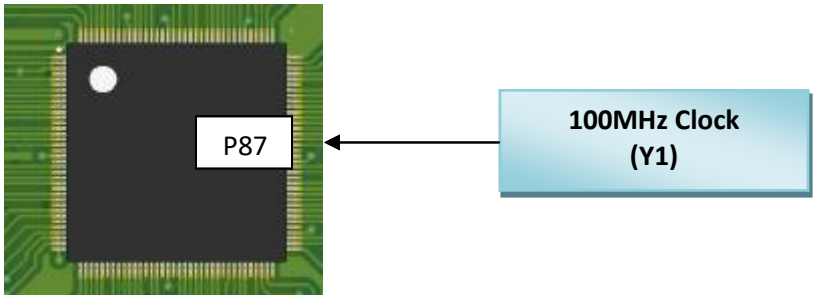


Figure 2 : Clock Source

CLK PIN NO = P87

4. FT2232 JTAG Programmer

AHMY_SP6LX9_LT board support to download the output files directly in to Spartan 6 FPGA or PROM using FT2232 USB to JTAG programmer. **AHMY_FT2232_Prog** or **xc3sprog** software is used to access the FPGA or PROM through FT2232 programmer.

5. LCD Interface

20x4 or 16x2 Numeric LCD interface Header provided in the AMHY_SP6LX9_LT Board and brightness adjustable trim pot placed top of the LCD (R82-10K). LCD Data Lines and FPGA interface details given below

FPGA Pin	LCD No	Signal Name
P7	4	LCD_RS
P8	6	LCD_EN
P9	7	LCD_D0
P10	8	LCD_D1
P11	9	LCD_D2
P12	10	LCD_D3
P14	11	LCD_D4
P15	12	LCD_D5
P16	13	LCD_D6
P17	14	LCD_D7

6. Switch & LED

16 user input selectable slide switch and 16 LEDs present in the bottom of the board. Switch and LED interface with FPGA details given below

FPGA Pin	Switch
P82	SW1
P80	SW2
P78	SW3
P74	SW4
P66	SW5
P55	SW6
P50	SW7
P46	SW8
P44	SW9
P41	SW10
P35	SW11

FPGA Pin	LED
P81	LED_1
P79	LED_2
P75	LED_3
P67	LED_4
P56	LED_5
P51	LED_6
P48	LED_7
P45	LED_8
P43	LED_9
P40	LED_10
P34	LED_11

P33	SW12	P32	LED_12
P30	SW13	P29	LED_13
P27	SW14	P26	LED_14
P24	SW15	P23	LED_15
P22	SW16	P21	LED_16

Figure 3 : Switch & LED pin mapping

7. Manual clock, UP & DOWN Key

Manual/External Clock input UP and DOWN Push button available in the AHMY_SP6LX9_LT board. All these pins are connected to FPGA GPI pins. All these pins have hardware debounce logic with +3.3V pull up resister (default value is 10. When user presses the button it connected to ground ('0').

Switch	FPGA PIN
EXT_CLK	P47
Push_UP	P105
Push_Down	P104

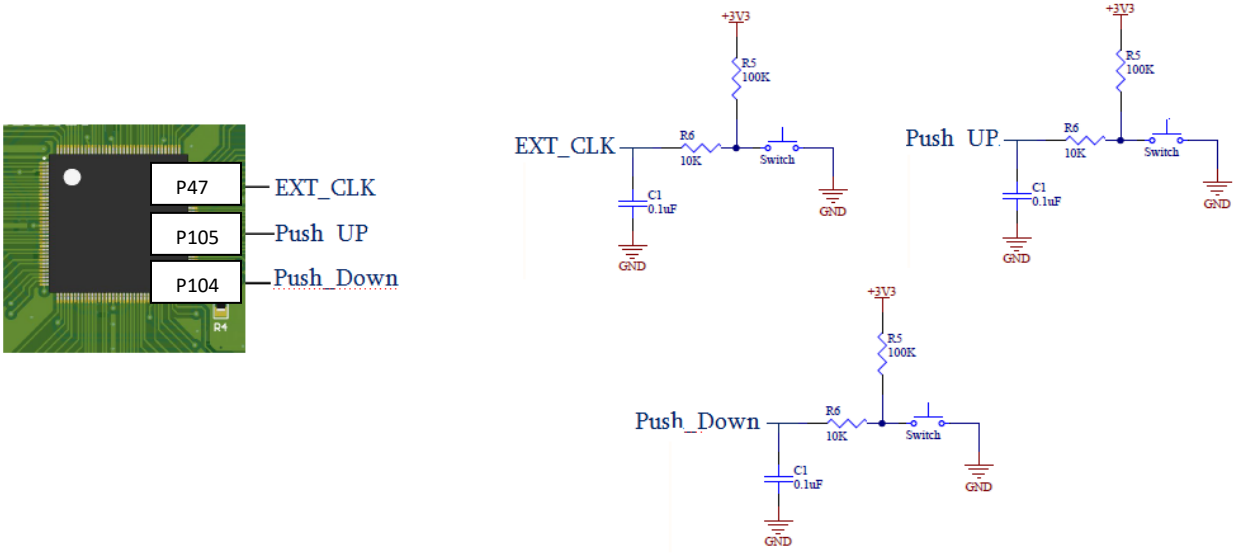


Figure 4 : Push switch pin mapping

8. Reset Key

Reset Key used to reset the FPGA.

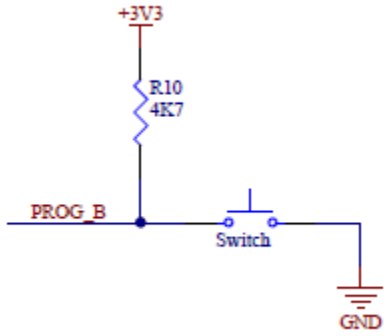


Figure 5 : Reset key

9. Matrix Keypad

The AHMY_SP6LX9_LT board has 4x4 Matrix Keypad, pin details given below. Keypads arranged by matrix format, each row and column section pulled by high, all row lines and column lines connected directly by the I/O pins

Matrix Key ROW	FPGA PIN
Mat_R1	P95
Mat_R2	P94
Mat_R3	P93
Mat_R4	P92

Matrix key Column	FPGA PIN
Mat_C1	P88
Mat_C2	P85
Mat_C3	P84
Mat_C4	P83

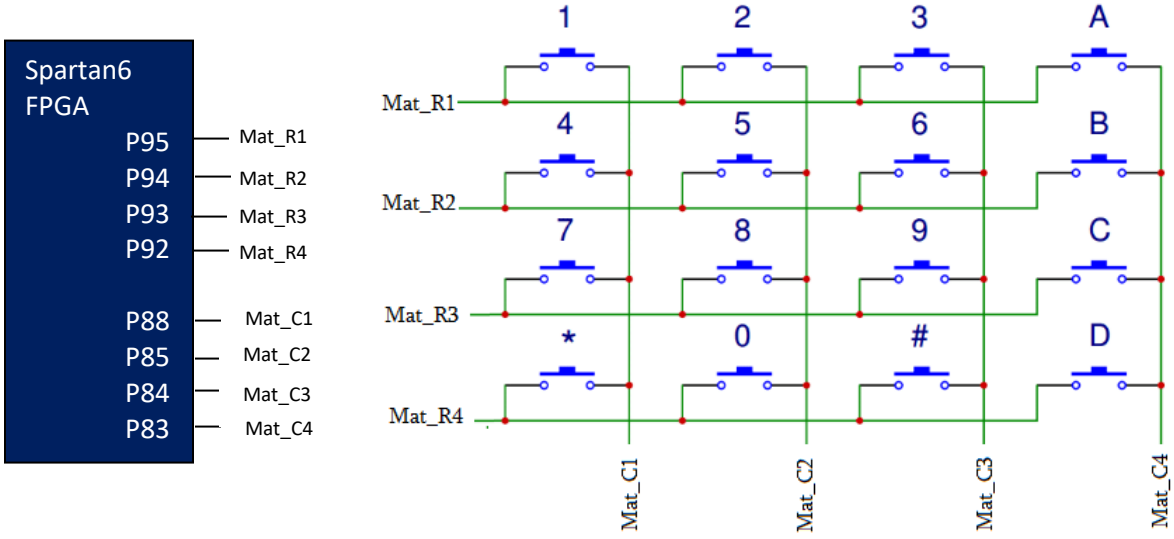


Figure 6 : Matrix Keypad

10. Relay

AHMY_SP6LX9_LT board has one on board 5V relay. Relay interface with FPGA pin details given below.

RELAY FPGA PIN → P97

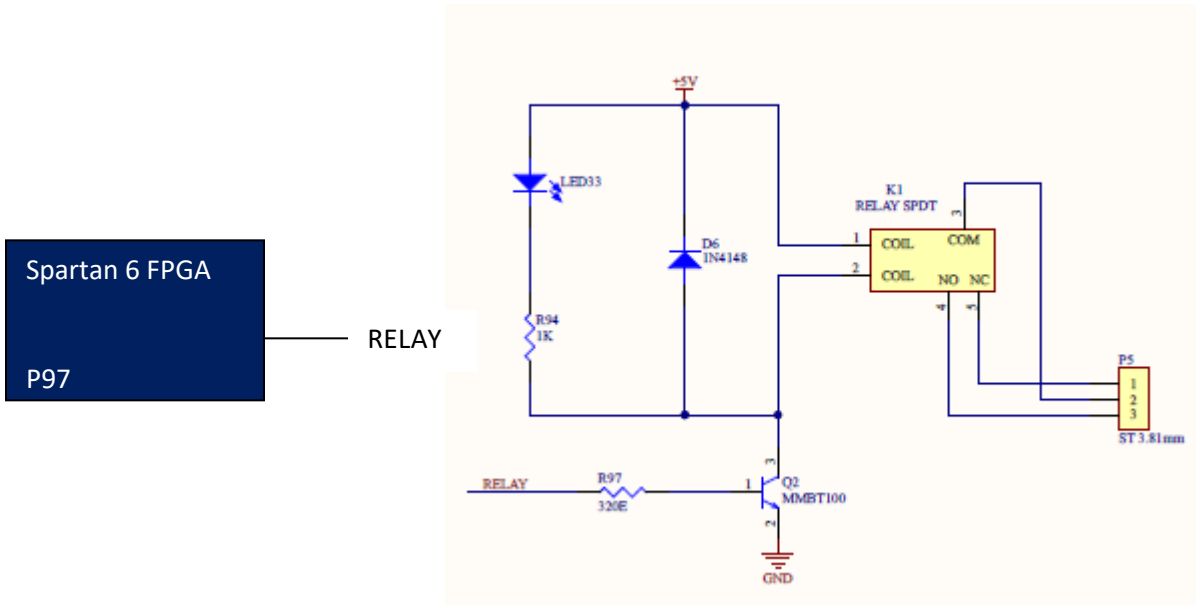


Figure 7 : Relay interface

11. Buzzer

AHMY_SP6LX9_LT board has one on board 5V Buzzer. Buzzer interface with FPGA pin details given below

BUZZER FPGA PIN → P98

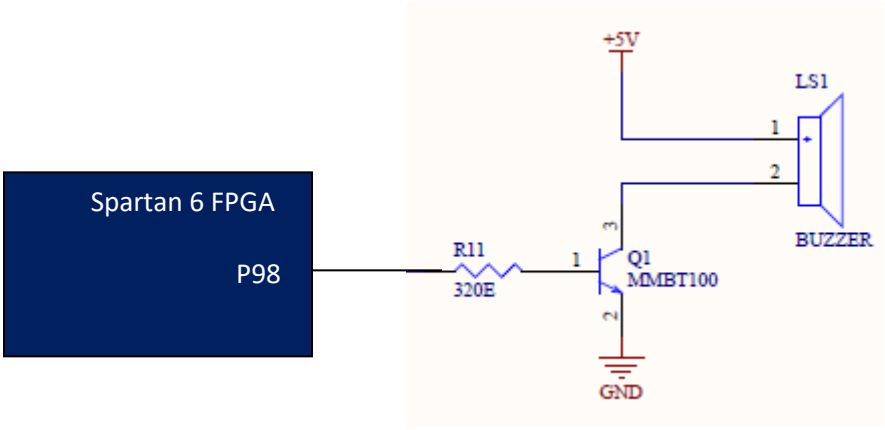


Figure 8 : Buzzer interface

12. 7 Segment display

AHMY_SP6LX9_LT board has 4 no of 7 segment display, pin details given below

Data lines	FPGA PIN
Data_A	P119
Data_B	P118
Data_C	P117
Data_D	P116
Data_E	P115
Data_F	P114
Data_G	P112
Data_DP	P111

7 Segment Selection	FPGA PIN
Disp 1	P102
Disp 2	P101
Disp 3	P100
Disp 4	P99

13. Connectors

In this section describe the all the connectors present in the AHMY_SP6LX9_LT board.

1. External programming header
2. GPIO header

13.1 External programming header

The Spartan-6 FPGA LX9 AHMY has one device in the JTAG chain, the Spartan-6 FPGA LX9 FPGA. Configuring the Spartan-6 FPGA on the S6LX9 AHMY can be performed via Boundary Scan with a JTAG download cable. The 10 pin Header details given below

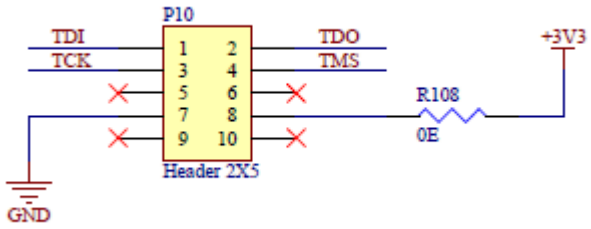


Figure 9 : External programming header

13.2 GPIO header

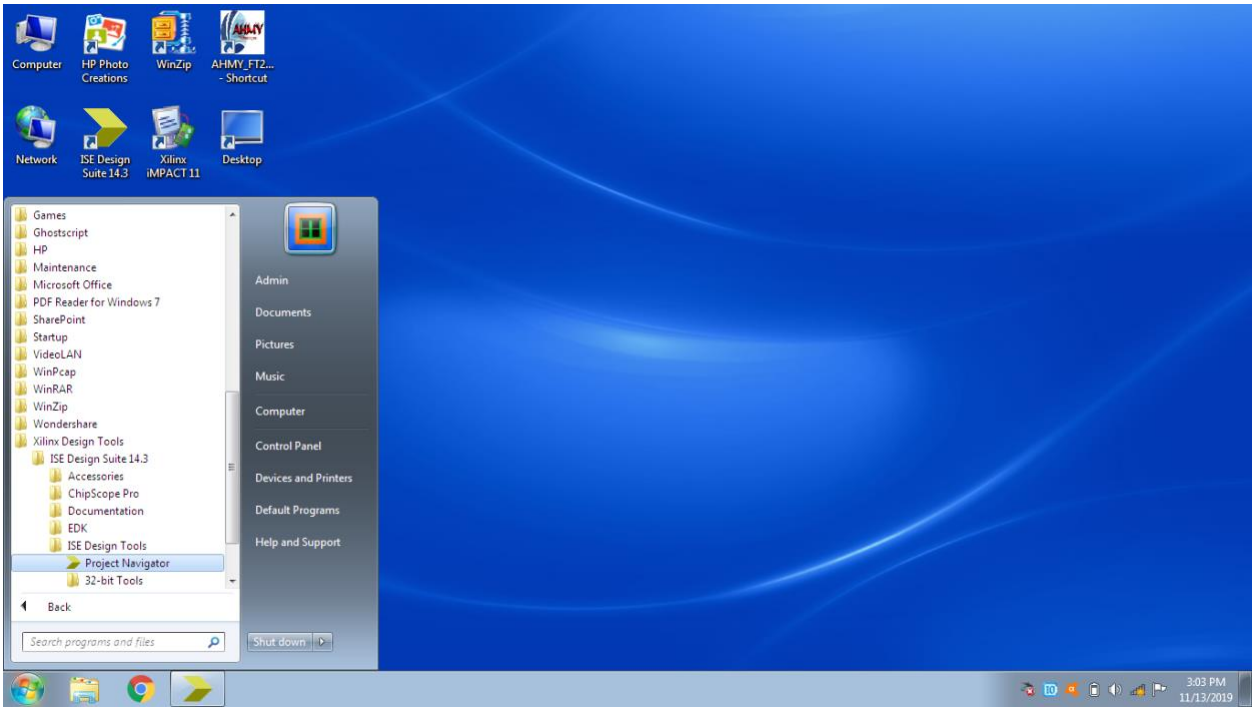
FPGA general purpose IO lines and connector details given below,

P9 Connector			
Connector Pin No	FPGA PIN No	Connector Pin No	FPGA PIN No
1	P144	2	P143
3	P142	4	P141
5	P140	6	P139
7	P138	8	P137
9	P134	10	P133
11	P132	12	P131
13	P127	14	P126
15	P69	16	P60
17	+3V3	18	GND
19	+3V3	20	GND

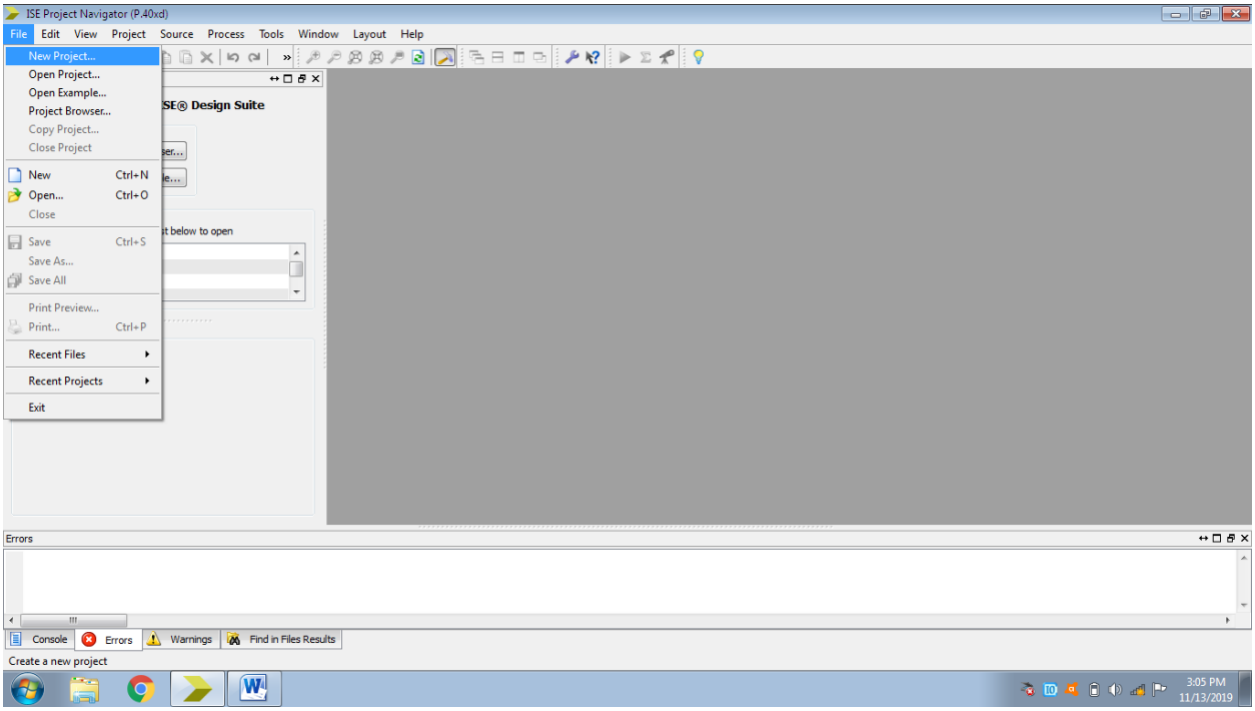
P12 Connector			
Connector Pin No	FPGA PIN No	Connector Pin No	FPGA PIN No
1	P119	2	P118
3	P117	4	P116
5	P115	6	P114
7	P112	8	P111
9	P95	10	P94
11	P93	12	P92
13	P88	14	P85
15	P84	16	P83
17	+3V3	18	GND
19	+3V3	20	GND

Working Procedure

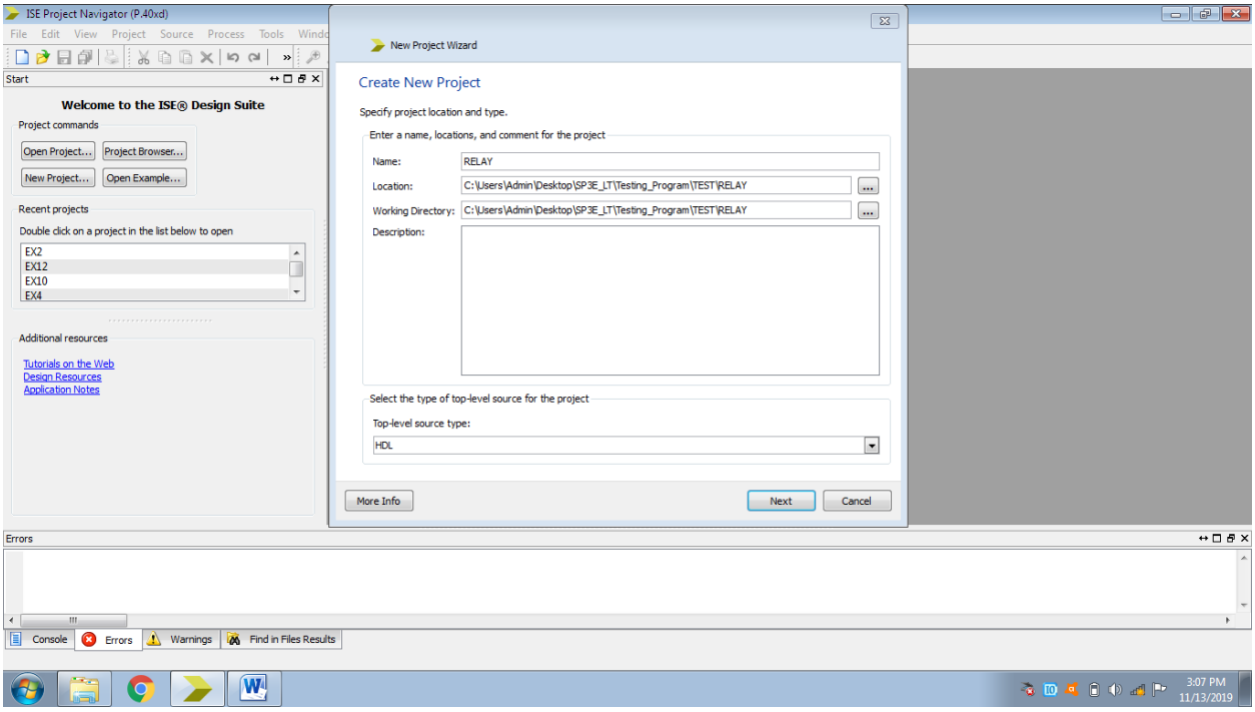
1) Go to **All Programs→ Xilinx Design Tools→ ISE Design Suite 14.3→ISE Design Tools→** Double click **-Project Navigator**



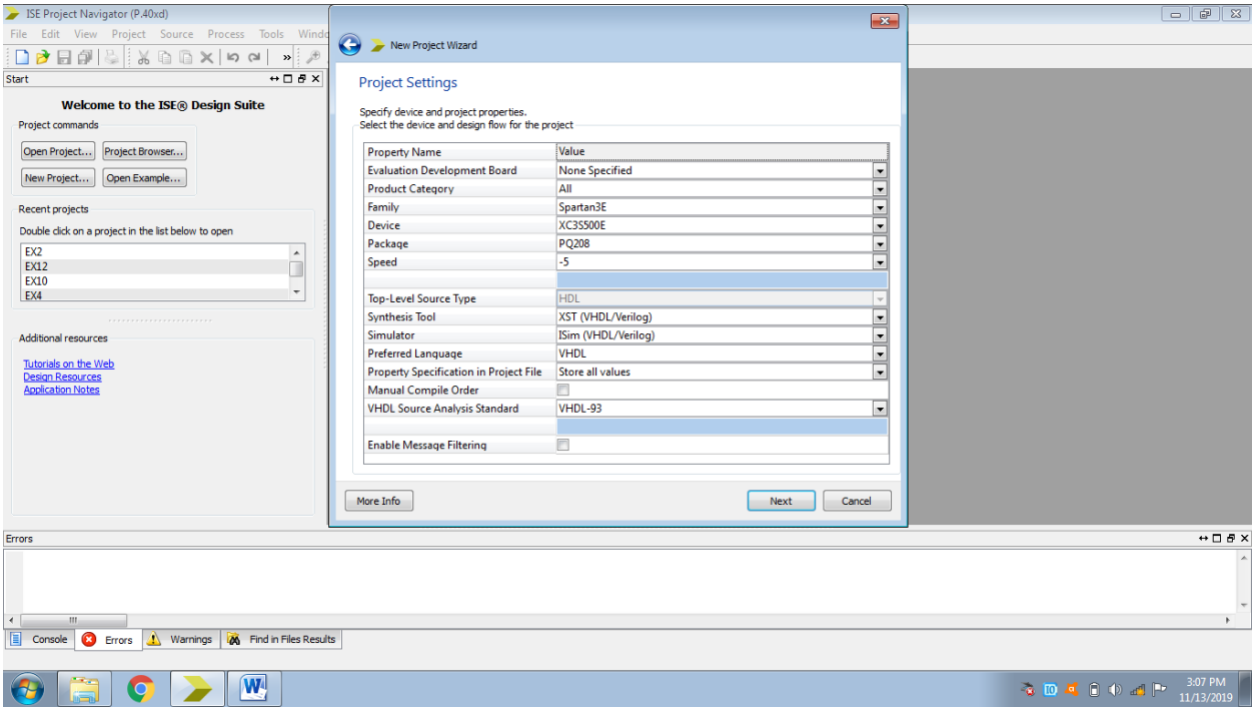
2) Go to **File→ New Project…**



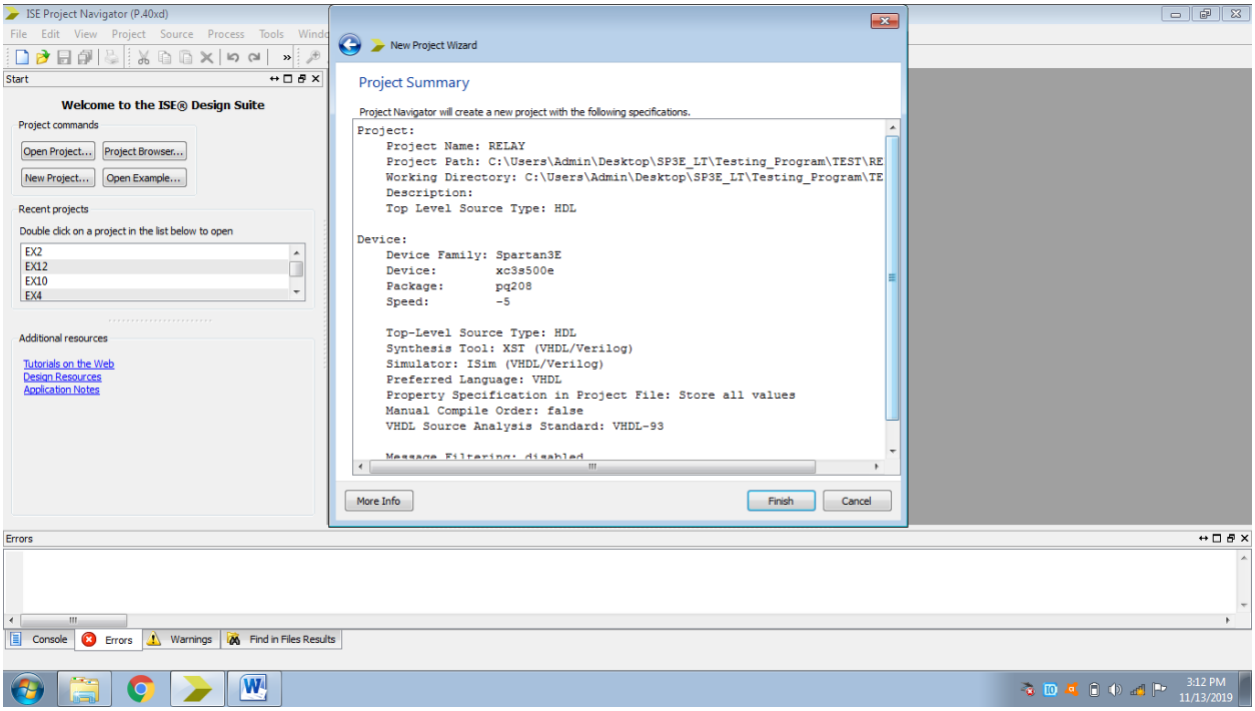
3) Give name and directory for the project then give **Next**



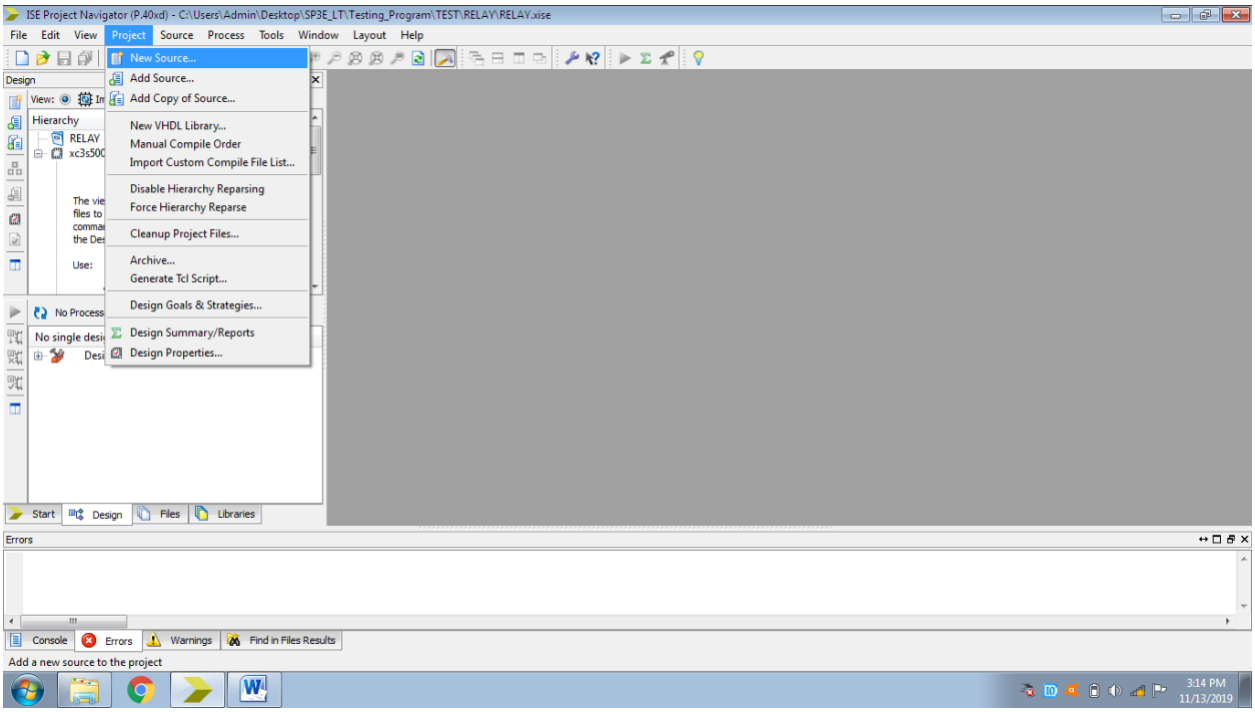
4) Select the device and design flow for the project and Give **Next**



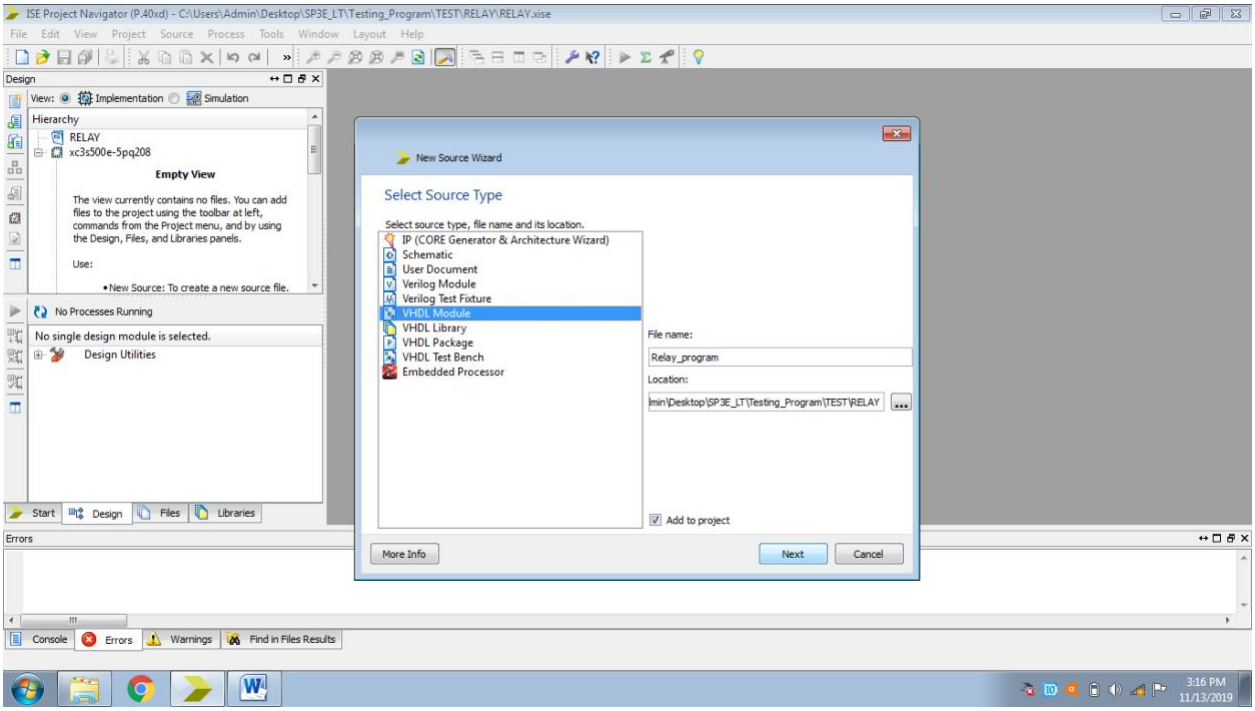
5) Check the selection press **finish**



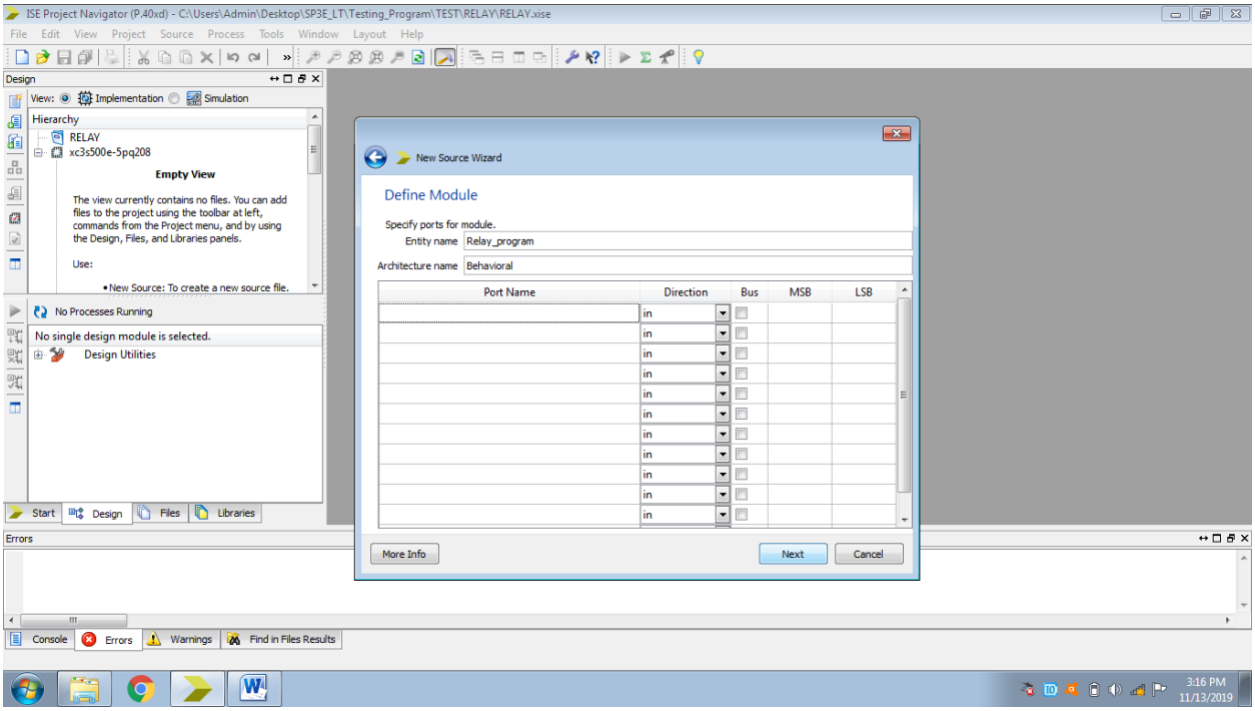
6)Go to **Project→ New Source…**



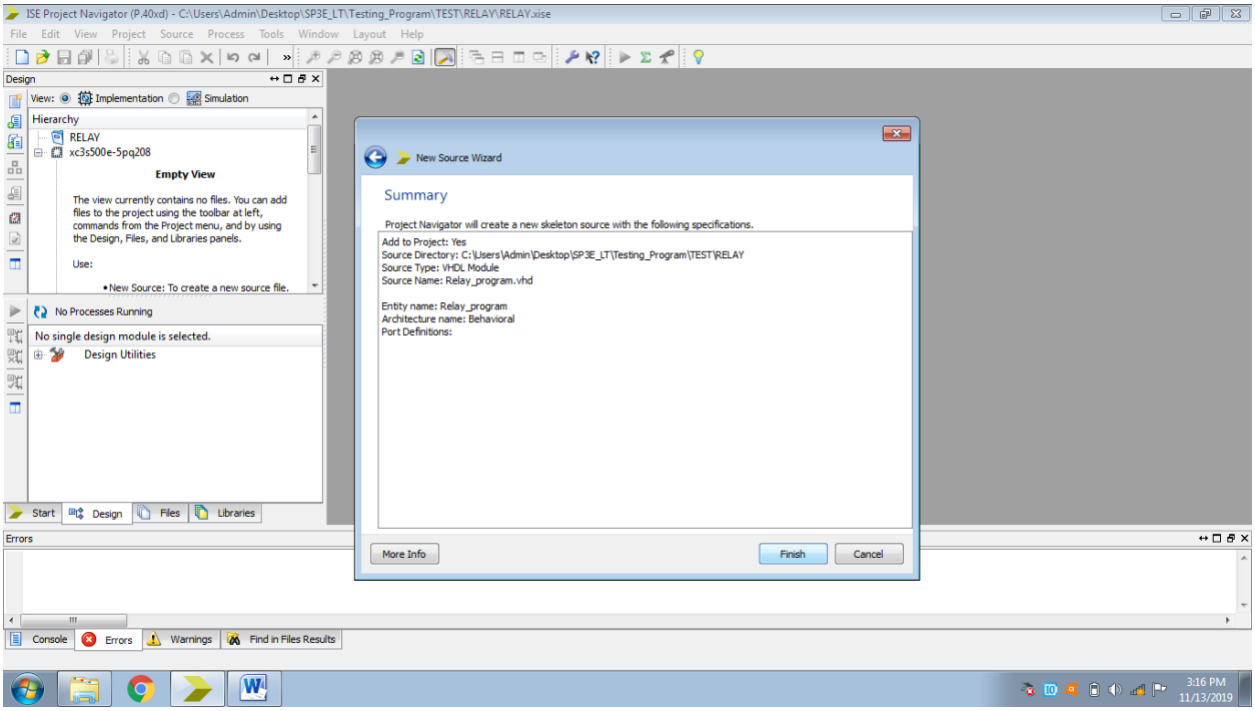
7) Select **VHDL Module** and Give the **File Name** (Don't give Space or comment words in Name), check **Location** and then Give **Next**



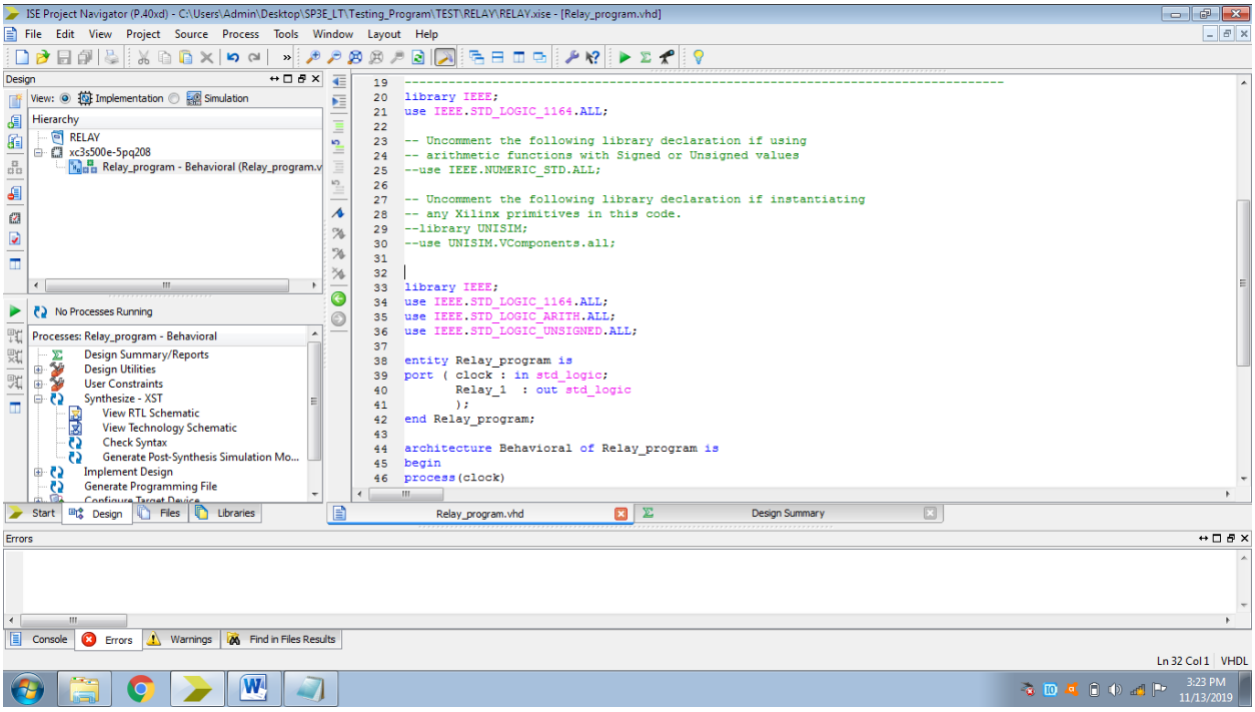
8) Assign input and output pins Or Give **Next**



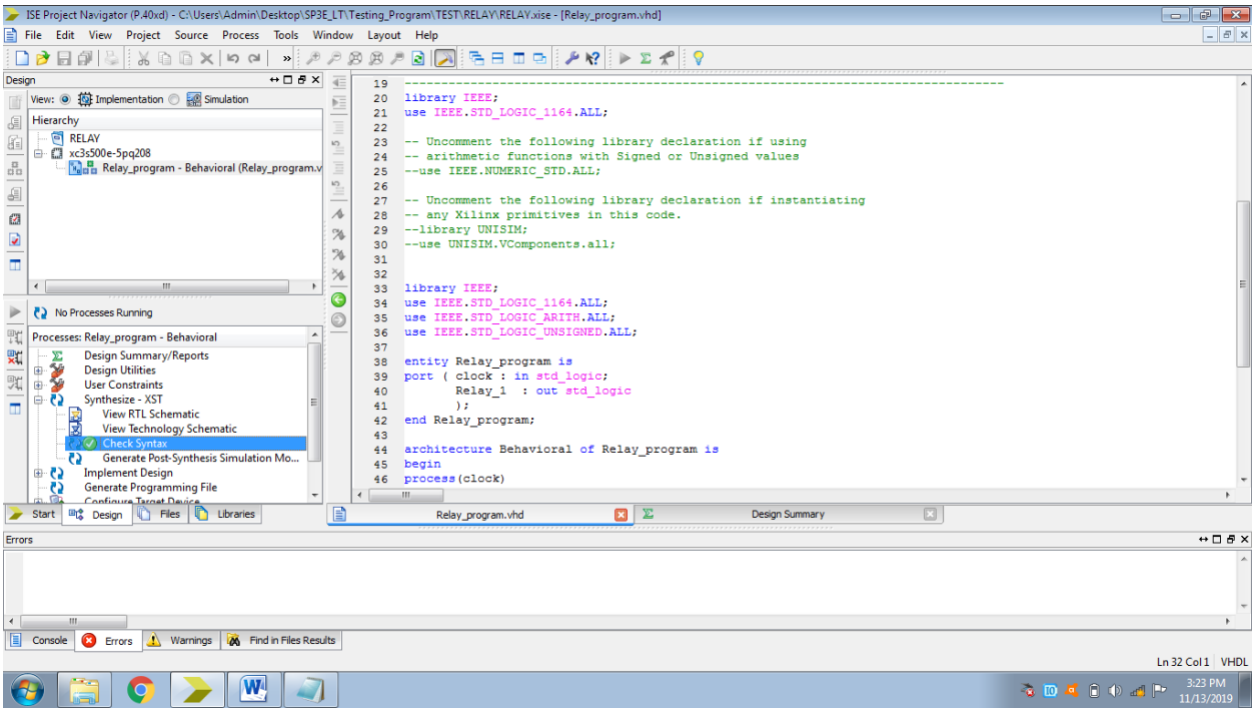
9) Check Summary and Give **Finish**



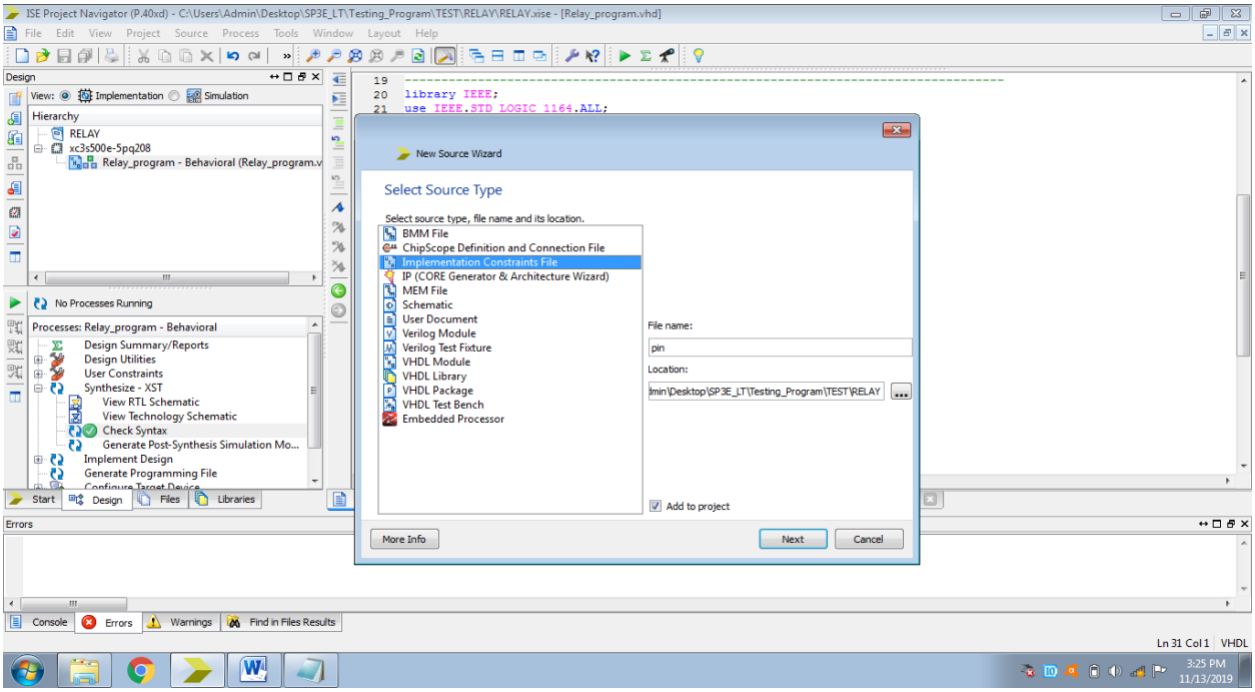
10) VHDL window will open then write the coding with structure and **Save** the file.



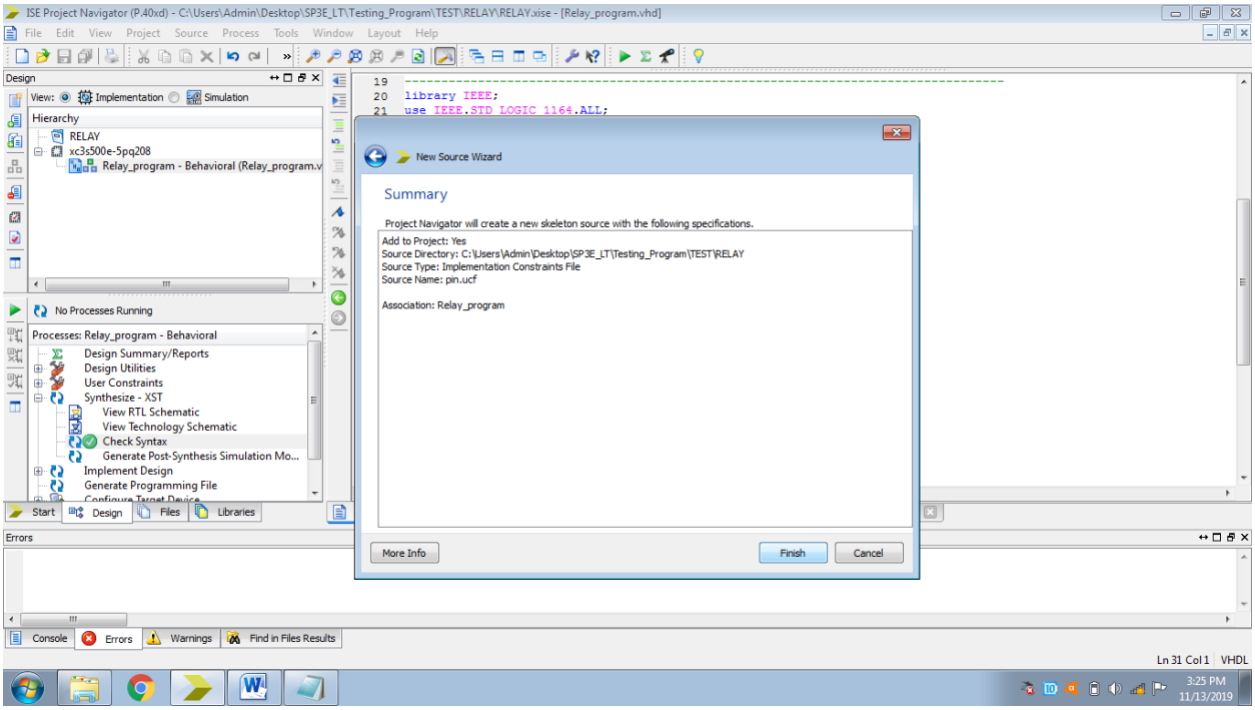
11) Right click in **synthesis** button and give run, Incase if there is no error in coding we are getting a green tick mark.



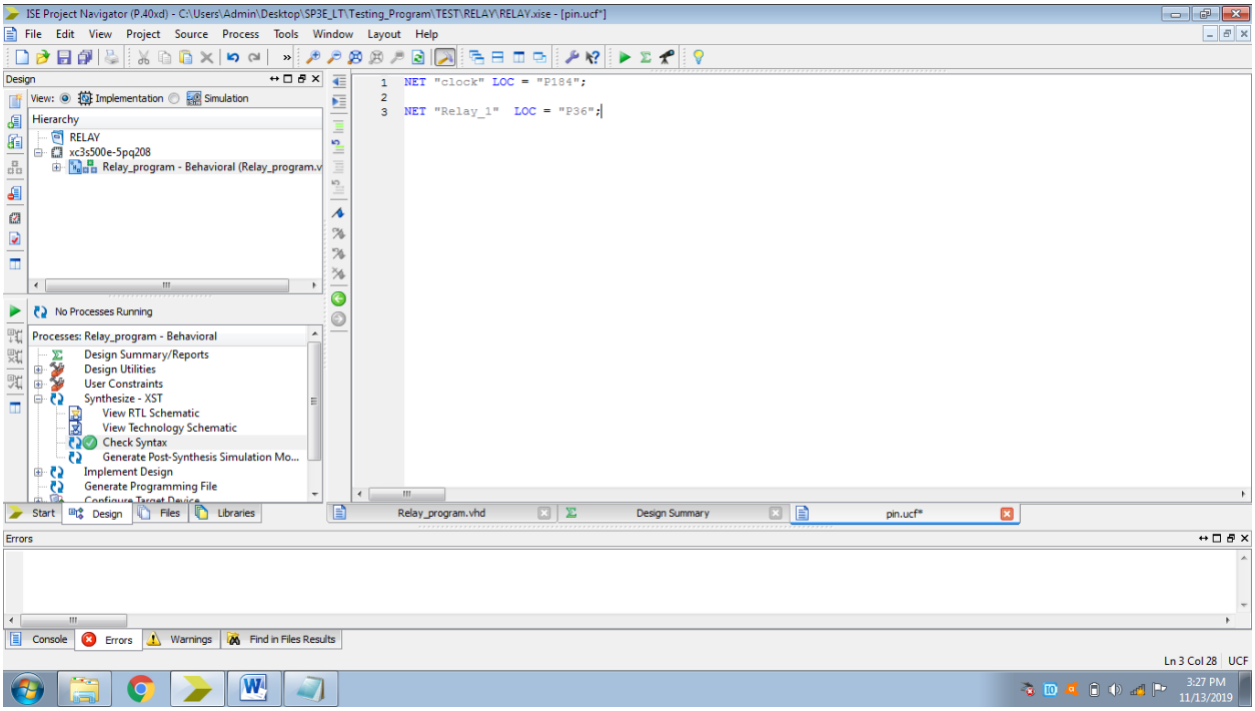
12) Go to **Project→ New Source..** → Select **Implementation Constraints File,** Give File Name and then give **Next**.



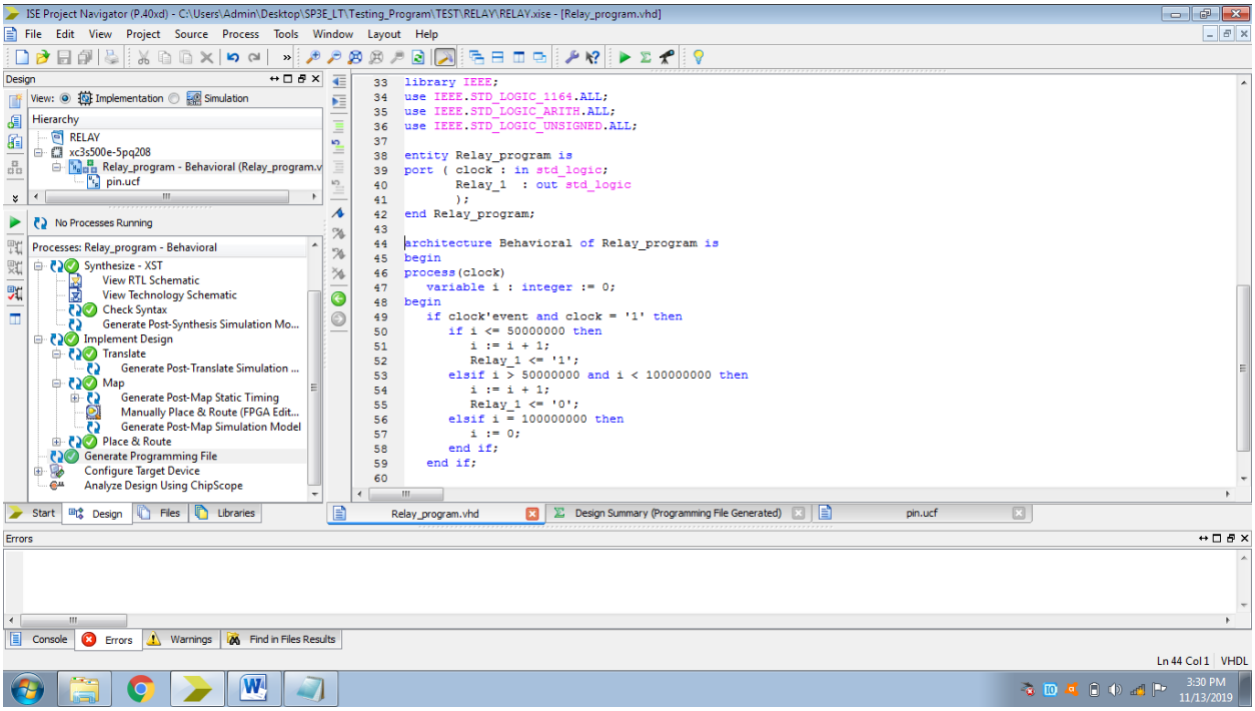
13)Check Summary and Give **finish**.



14) Assign pin number for input output variable as per given format and **Save** the File.

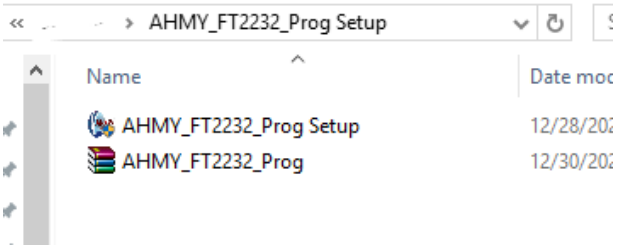


15) Right click on **Generate program file** and press run for generate bit file for FPGA board. After getting all green tick mark, Bit file will generated in project location, and then Download the bit file to the FPGA trainer.

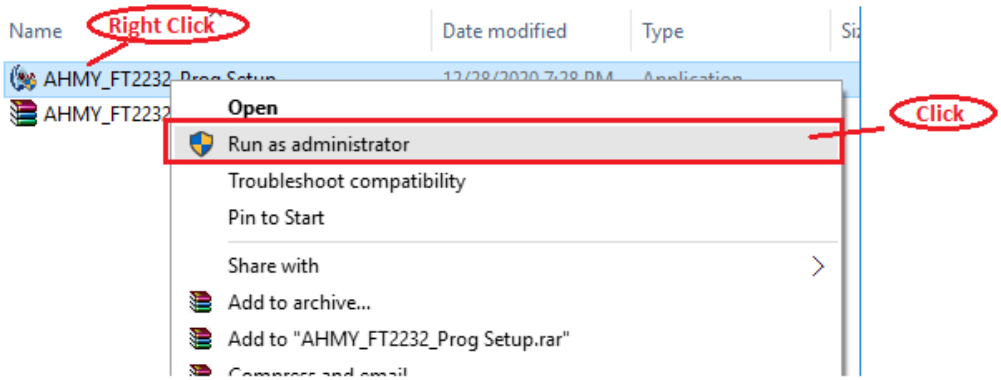

ISE Project Navigator (P.40xd) - C:\Users\Admin\Desktop\SP3E_LT\Testing_Program\TEST\RELAY\RELAY.xise - [Relay_program.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
RELAY
xc3s500e-5pq208
Relay_program - Behavioral (Relay_program.v
pin.ucf
No Processes Running
Processes: Relay_program - Behavioral
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Mo...
Implement Design
Translate
Generate Post-Translate Simulation ...
Map
Generate Post-Map Static Timing
Manually Place & Route (FPGA Edit...
Generate Post-Map Simulation Model
Place & Route
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start Design Files Libraries
Relay_program.vhd
Design Summary (Programming File Generated)
pin.ucf
Errors
Console Errors Warnings Find in Files Results
Ln 44 Col 1 VHDL
3:30 PM
11/13/2019
33 library IEEE;
34 use IEEE.STD_LOGIC_1164.ALL;
35 use IEEE.STD_LOGIC_ARITH.ALL;
36 use IEEE.STD_LOGIC_UNSIGNED.ALL;
37
38 entity Relay_program is
39 port (clock : in std_logic;
40 Relay_1 : out std_logic
41);
42 end Relay_program;
43
44 architecture Behavioral of Relay_program is
45 begin
46 process(clock)
47 variable i : integer := 0;
48 begin
49 if clock'event and clock = '1' then
50 if i <= 50000000 then
51 i := i + 1;
52 Relay_1 <= '1';
53 elsif i > 50000000 and i < 100000000 then
54 i := i + 1;
55 Relay_1 <= '0';
56 elsif i = 100000000 then
57 i := 0;
58 end if;
59 end if;
60

Software Installation steps:

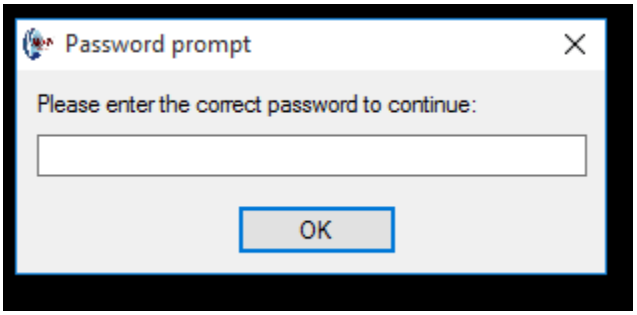
1. AHMY_FT2232_Prog Setup available in the cd delivered by AHMY technologies. Go to the AHMY_FT2232_Prog Setup folder (refer below image).



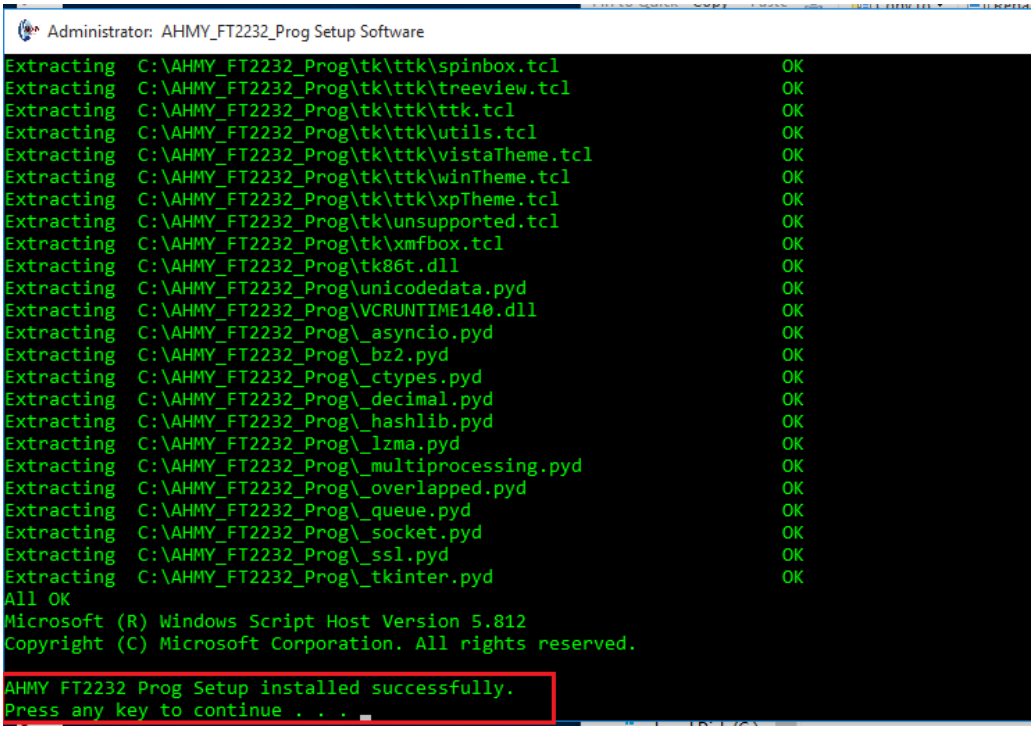
2. Run "AHMY_FT2232_Prog Setup.exe". (Make sure install "Run as administrator").



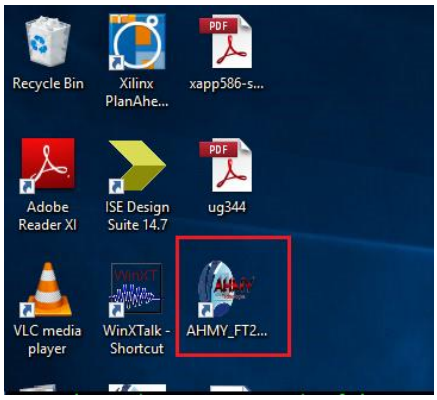
3. Next Enter Password : **AHMY**



4. After Enter password, Software installation shall start and installation status shall be printed in command window. Press any key to continue



5. Check “AHMY_FT2232_Prog” shortcut created in the Desktop.

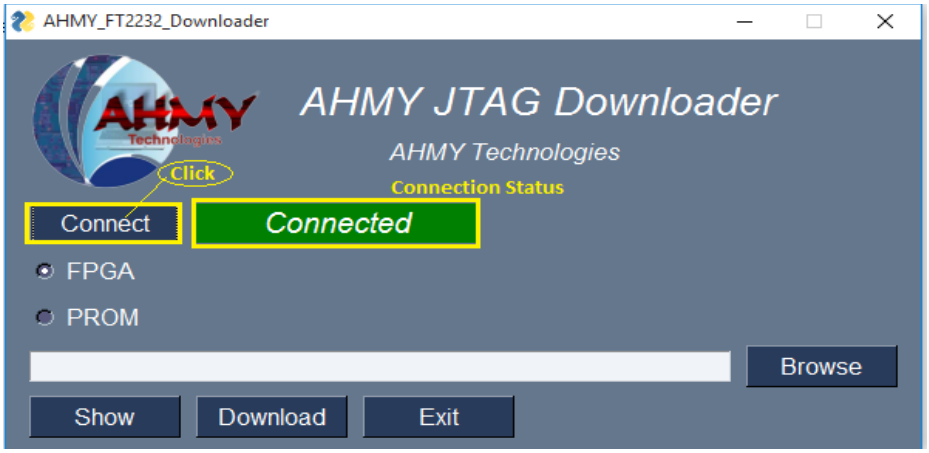


6. Install Programmer driver - **CDM21228_Setup**. Its delivered with cd.
7. Now AHMY_FT2232_Prog_Downloader software is ready to use. Enjoy ☺

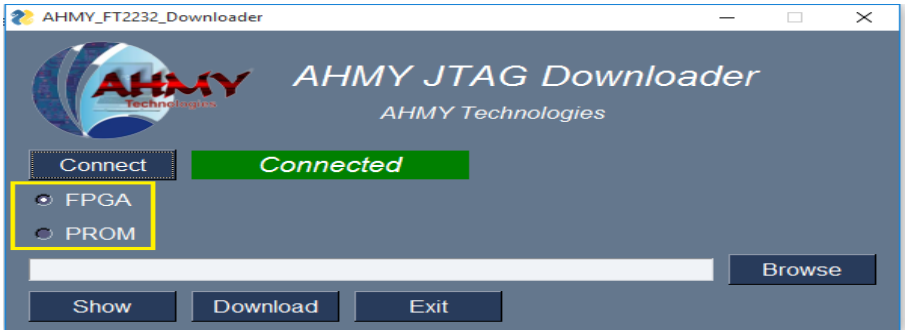
FPGA/PROM program downloading steps:

1. Open “AHMY_FT2232_Prog” icon. AHMY_FT2232_Prog software shall open.

2. Make sure FPGA board powered ON and USB cable connected With PC. Then click “Connect” button. Programmer connected status will be displayed. FPGA/PROM option enabled once board is connected successfully.



3. Select “FPGA” or “PROM” to download the .bit file.


AHMY_FT2232_Downloader
AHMY JTAG Downloader
AHMY Technologies
Connect
Connected
FPGA
PROM
Browse
Show
Download
Exit