

Lab 1: Power Management & Bootloading

ESE519 - Embedded Systems - Fall 2020

Due: Friday, September 15, 2020 23:59PM EDT

In this document, you'll fill out your responses to the questions listed in the [Lab 1 Manual](#). Please fill out your name and link your Github repository below to begin. Be sure that your code on the repo is up-to-date before submission!

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1. Derivation of Voltage divider equation for the given circuit is -
 $V - IR_1 - IR_2 = 0$ (Using KVL)

$$V = I(R_1 + R_2)$$

$$V / (R_1 + R_2) = I$$

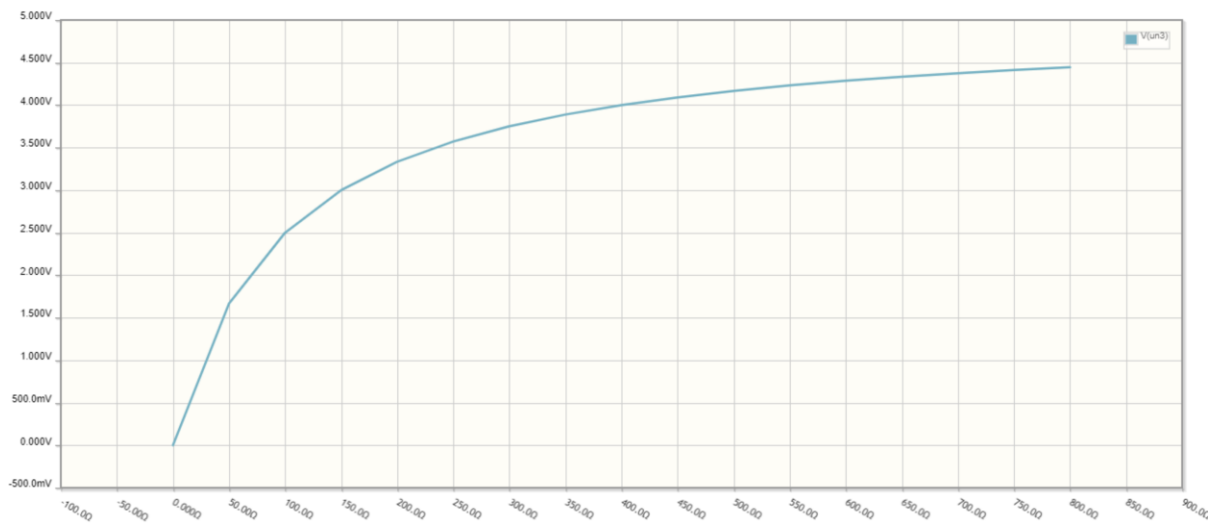
$$\text{Voltage at node 1} = I * R_2 = V / (R_1 + R_2) * R_2$$
$$= 2.5 \text{ Volt}$$

1) Applying KVL $\div 5V - IR_1 - IR_2 = 0$
 $\Rightarrow 5 = I(R_1 + R_2)$
 $\Rightarrow \frac{5}{R_1 + R_2} = I = \frac{V_1}{R_1 + R_2}$ [Using Kirchhoff's law]
New Voltage at R_2
Voltage Divider Equation $= I \times R_2 = \frac{V_1}{R_1 + R_2} \times R_2$
 $= \frac{5}{200} \times 100 = 2.5V$

2. Applying Voltage Divider with $R_1=100$, $R_2=850$

2) If $R_2 = 850$
 $V_{\text{NODE1}} = \frac{5}{100 + 850} \times 850 = 4.47V$

3.



Yes this is the expected behavior. As the resistance increases the voltage drop across the Resistor also increases (Ohm's Law) as the current remains constant in the circuit.

4.

In building cheap circuits.

Designing simple circuits

In designing circuits where power requirement of the circuit is limited to 1 Watt.

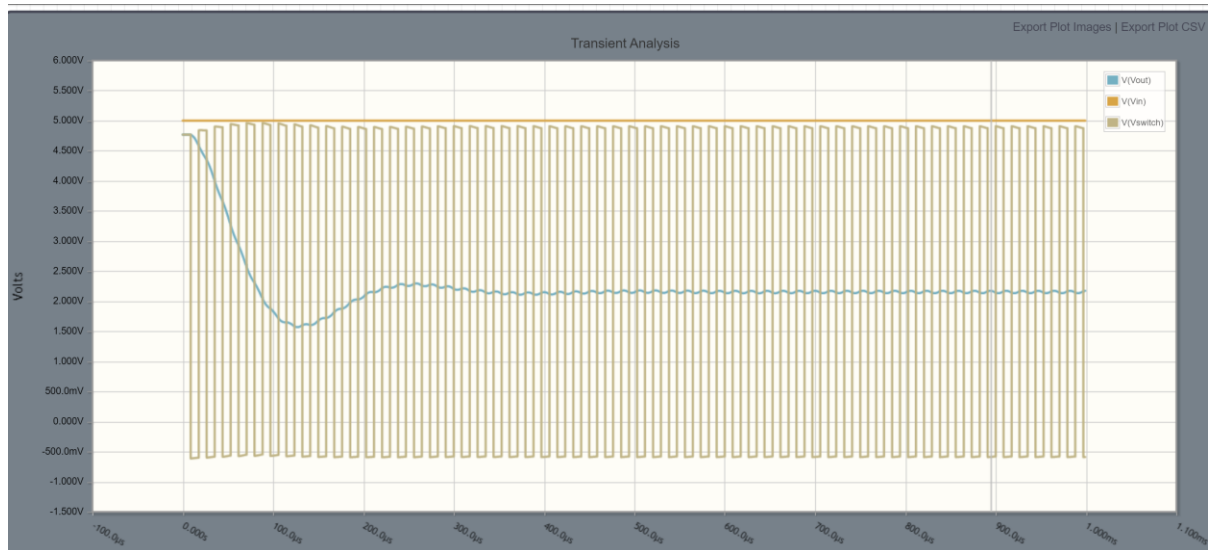
5. Off time of the pulse

6. The ideal equation (when we ignore the losses across the switch/mosfet and catch diode) to calculate the duty cycle for a given output voltage is $D = V_{out} / V_{in}$. Otherwise the equation for D is $D = V_{out} / (V_{in} * E)$ where E is the efficiency. E is generally 0.9(90%).

- For $V_{out} = 3.3 \text{ V}$; $D_{(on)} = 3.3 / (5 * 0.9) = 0.733$. $D_{(off)} = 1 - 0.733 = 0.27$ (approx.). So with $D = 0.27 - 0.28$ we get an output of 3.3V.
- For $V_{out} = 2 \text{ V}$; $D_{(on)} = 2 / (5 * 0.9) = 0.45$. $D_{(off)} = 1 - 0.45 = 0.55$ (approx.). So with $D = 0.53$ (approx to 0.55) we get an output of 2V.

The values makes sense as the losses in catch diode and switch needs to be taken under consideration while calculation.

7.



8. The output ripple voltage is the phenomenon where the voltage falls down and then rises again. The factors contributing to this phenomenon is the output capacitance (majorly), inductor, and switching frequency.

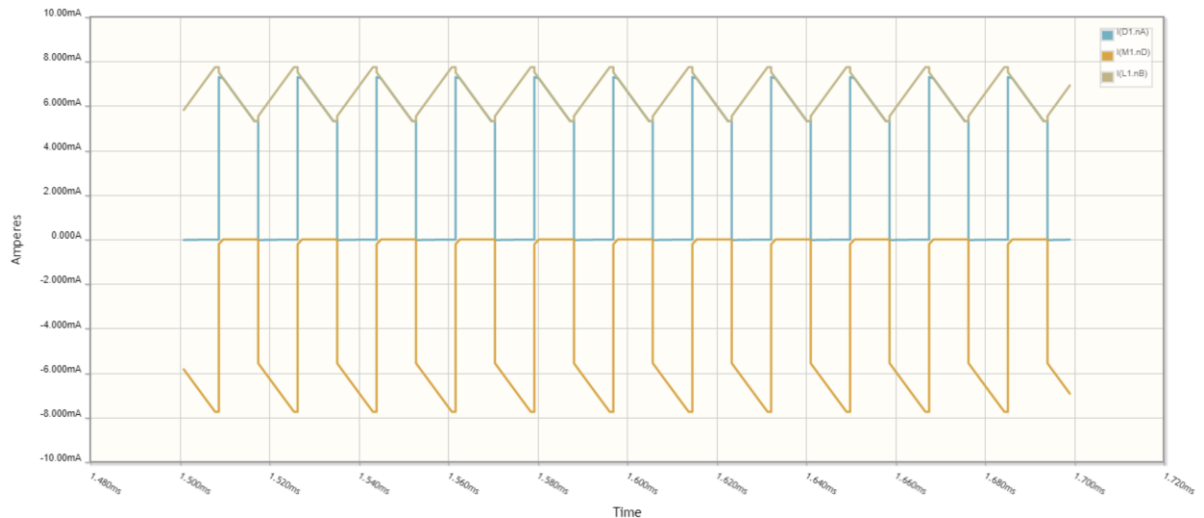
The capacitor charges and discharges initially till the voltage across it becomes stable. Hence the same ripple effect will be reflected on the output load.

The inductor too initially generates a back emf (Faraday's Law) opposing the supply voltage, hence the total voltage across the load will be always go up and then drop down initially until it becomes stable.

This explains the dip at 100us.

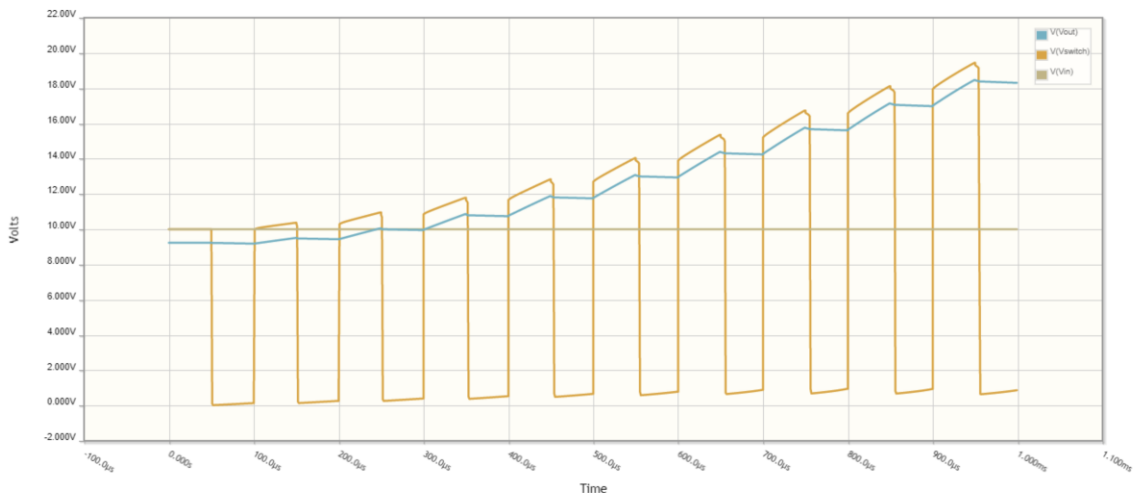
Also the output voltage is not a straight line as the capacitor keeps charging and discharging. When the supply is not connected the inductor acts as a supply source for the load. It discharges and the voltage across the load decreases until it charges back up in the next cycle.

9.



10. All the times KCL is being followed. The current in the Mosfet (pmos) is negative because current flows from source to drain. In the first half of the cycle when the diode is reverse biased ($I_{diode}=0$), $I(L)+I(diode)=I(mosfet)$ in terms of magnitude. In the next half the Mosfet turns off, $I(Mosfet)=0$. $I(Inductor)=I(Diode)$.

11.



12. The output is nearly equal to the expected value $=18.5V$. As $V_{out} = V_{in} / ((1-D) * E)$ where E is the efficiency and D is the duty cycle. Ideally $E = 1$ and V_{out} should be equal to $20V$. Other losses like voltage across the catch diode and drop in mosfet needs to be also taken in consideration while calculating V_{out} .

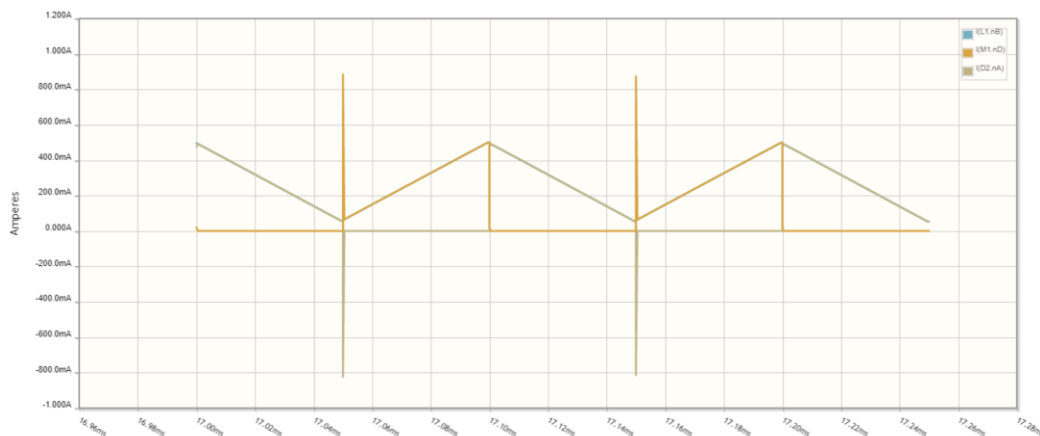
13.

Because initially in the first cycle when the switch is open, the capacitor is charged to input voltage minus one diode drop. In next cycle the switch is closed and the inductor is charged, also output capacitor stays charged since it can't discharge through the now back-biased diode. In the third cycle both inductor and capacitor

act as voltage sources to the load. Hence it takes time for the circuit to become stable.

In buck converter only the inductor was supposed to be charged before achieving stability. In boost converter both inductor and capacitor needed to be charged in the first cycle before reaching stability.

14.



15. Yes KCL is expected. In the first half (17m to 17.5m) the diode and the inductor conducts current. $I(\text{Mosfet})=0$; $I(\text{inductor}) = I(\text{diode})$ [KCL at V_{switch}]. In the next half, the inductor and the Mosfet conducts current while the diode remains reverse biased. $I(\text{inductor}) = I(\text{Mosfet})$ [KCL at V_{switch}].

16.

Jack	USB	Power Source?	NODE1	NODE2	NODE3
0V	5V	USB	-928.8u	4.99V	3.33V

10V	0V	Jack	5V	5V	3.3V
10V	5V	Jack	5V	5V	3.3V
5V	5V	Jack	4.315V	4.315V	3.3V

17. A resistive voltage divider is commonly used at the input to a comparator to set a threshold voltage for sense inputs. The threshold voltage is set by the ratio of the two resistors in the divider.
18. It is a bootloader for Arduino. It is a program that runs on startup and configures a device before the main program begins. It helps for In system programming and the script runs and allocates the program script to different parts of memory using vector table. It also configures the baud rate for the Arduino which then helps in communication with other peripherals.
- 19.

