Metal oxide Semiconductor Field effect transistor: Basic structure, types, working of n channel MOSFET Enhancement type and study of output and transfer characteristics.

Reference: Donald A Neamen, "Semiconductor Physics and Devices", Tata McGraw Hill, 4th Edition

METAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS SUMMARY

MOSFET TOPIC BEGINS:

A metal oxide semiconductor field-effect transistor (MOSFET) is a unipolar device. The current flow in a MOSFET depends on one type of majority carrier (electrons or holes). The output current of MOSFETs is controlled by an electric field that depends on a gate control voltage. There are two types of MOSFETs: enhancement MOSFETs and depletion MOSFETs.

3.1.2 n-Channel Enhancement-Mode MOSFET

Transistor Structure

Figure 3.5(a) shows a simplified cross section of a MOS field-effect transistor. The gate, oxide, and p-type substrate regions are the same as those of a MOS capacitor. In addition, we now have two n-regions, called the **source terminal** and **drain terminal.** The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the **channel region,** adjacent to the oxide–semiconductor interface.

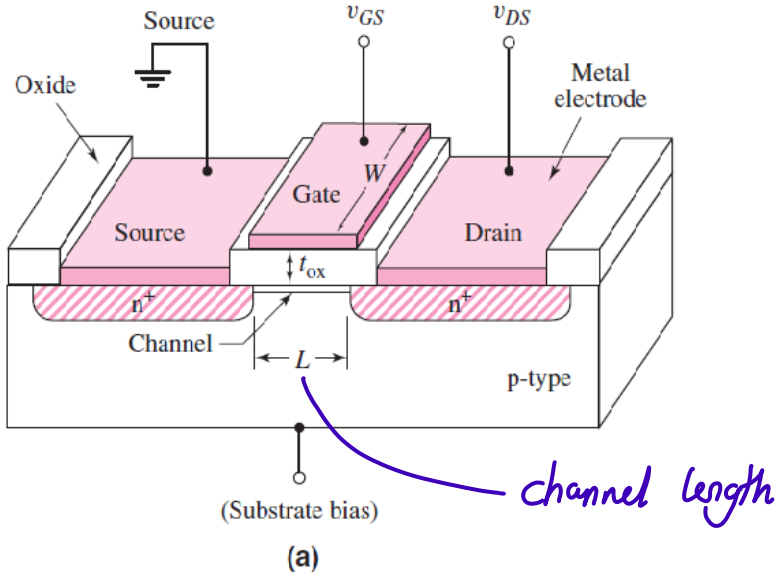

Figure 3.5 (a) Schematic diagram of an n-channel enhancement-mode MOSFET

The channel length L and channel width W are defined on the figure. The channel length of a typical integrated circuit MOSFET is less than 1 μm (10^{-6} m), which means that MOSFETs are small devices. The oxide thickness t_{ox} is typically on the order of 400 angstroms, or less.

The diagram in Figure 3.5(a) is a simplified sketch of the basic structure of the transistor.

N-channel MOSFET Enhancement type WORKING:

Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 3.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 3.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer "connects" the n-source to the n-drain,

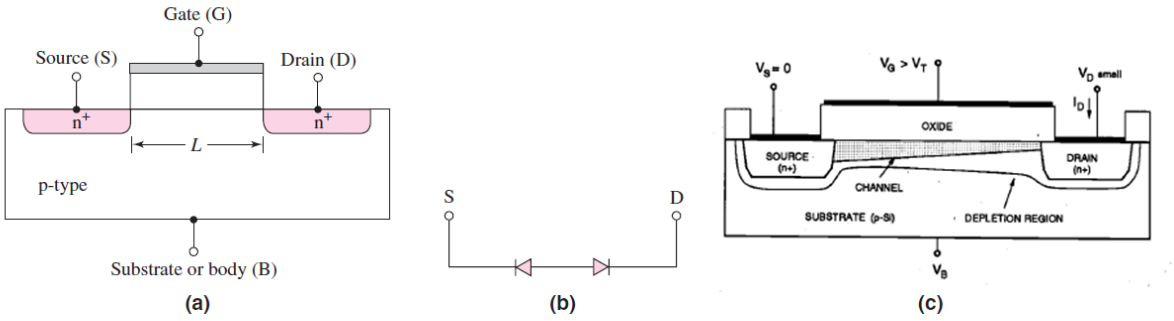

Figure 3.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

as shown in Figure 3.6(c). A current can then be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement-mode MOSFET.** Also, since the carriers in the inversion layer are electrons, this device is also called an **n-channel MOSFET (NMOS).**

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

3.1.3 Ideal MOSFET Current–Voltage Characteristics—NMOS Device

The **threshold voltage** of the n-channel MOSFET, denoted as V_{TN}, is defined[2] as the applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate. In simple terms, we can think of the threshold voltage as the gate voltage required to "turn on" the transistor.

For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge. If the gate voltage is less than the threshold voltage, the current in the device is essentially zero. If the gate voltage is greater than the threshold voltage, a drain-to-source current is generated as the drain-to-source voltage is applied. The gate and drain voltages are measured with respect to the source.

Figure 3.7(a) shows an n-channel enhancement-mode MOSFET with the source and substrate terminals connected to ground. The gate-to-source voltage is less than the threshold voltage, and there is a small drain-to-source voltage. With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero (neglecting pn junction leakage currents).

Figure 3.7(b) shows the same MOSFET with an applied gate voltage greater than the threshold voltage. In this situation, an electron inversion layer is created and, when a small drain voltage is applied, electrons in the inversion layer flow from the source to the positive drain terminal. The conventional current enters the drain terminal and leaves the source terminal. Note that a positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.

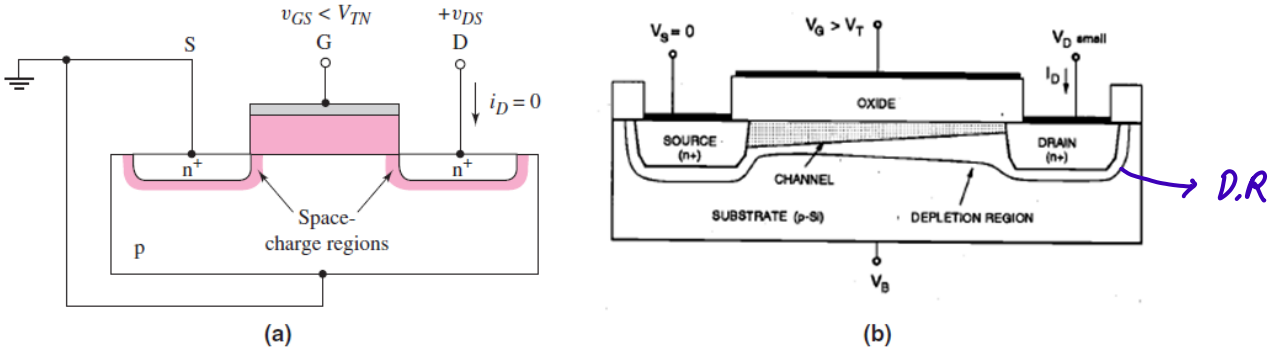

Figure 3.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

The i_D versus v_{DS} characteristics[3] for small values of v_{DS} are shown in Figure 3.8. When $v_{GS} < V_{TN}$, the drain current is zero. When v_{GS} is greater than V_{TN}, the channel inversion charge is formed and the drain current increases with v_{DS}. Then, with a larger gate voltage, a larger inversion charge density is created, and the drain current is greater for a given value of v_{DS}.

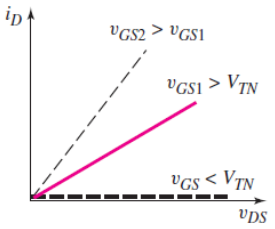

Figure 3.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

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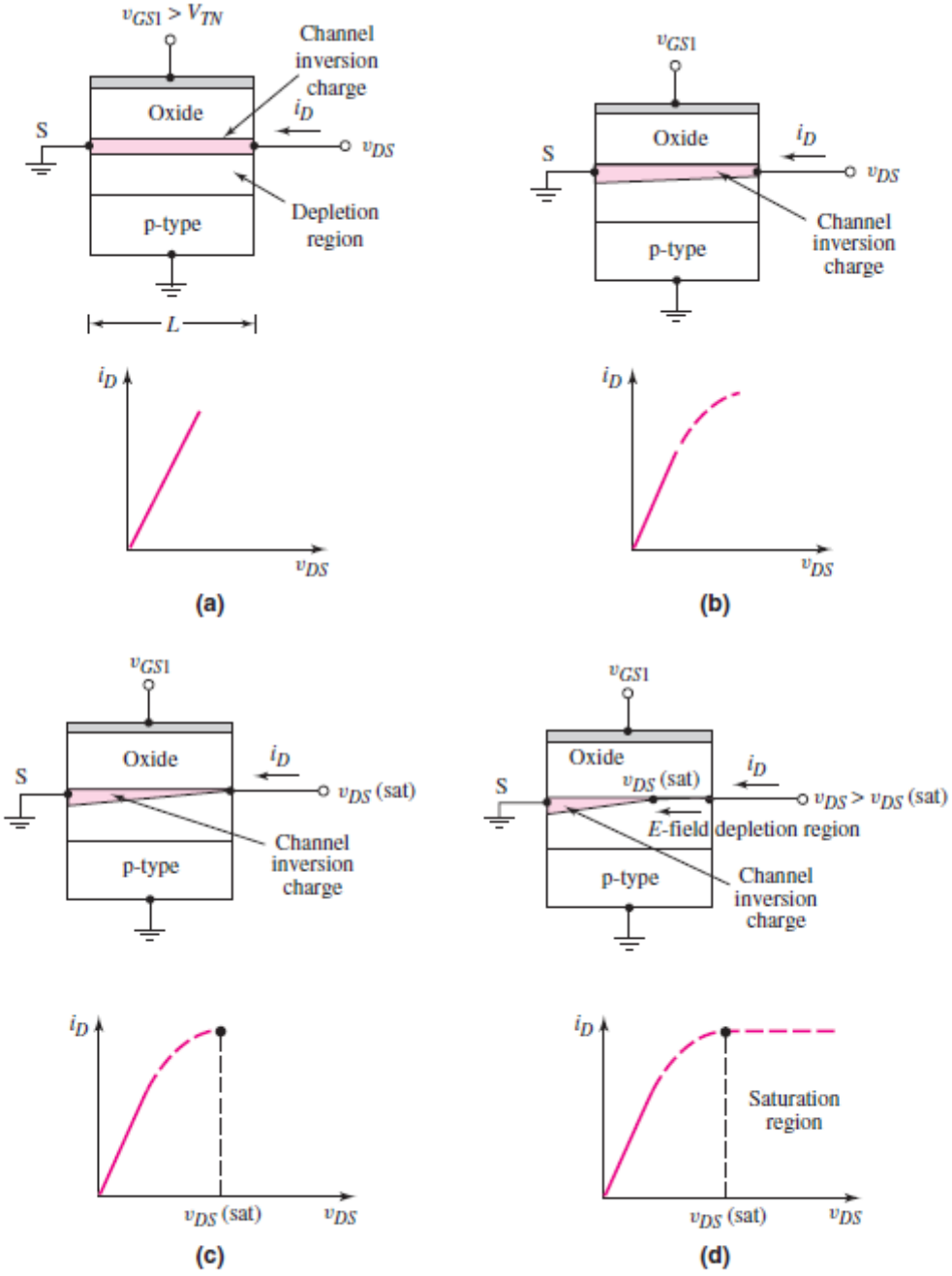

Figure 3.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for (a) a small v_{DS} value, (b) a larger v_{DS} value but for $v_{DS} < v_{DS}(\text{sat})$, (c) $v_{DS} = v_{DS}(\text{sat})$, and (d) $v_{DS} > v_{DS}(\text{sat})$

Figure 3.9(a) shows the basic MOS structure for $v_{GS} > V_{TN}$ and a small applied v_{DS}. In the figure, the thickness of the inversion channel layer qualitatively indicates the relative charge density, which for this case is essentially constant along the entire channel length. The corresponding i_D versus v_{DS} curve is also shown in the figure.

Figure 3.9(b) shows the situation when v_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the i_D versus v_{DS} curve to decrease. This effect is shown in the i_D versus v_{DS} curve in the figure.

As v_{DS} increases to the point where the potential difference, $v_{GS} - v_{DS}$, across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density at the drain terminal is zero. This effect is shown schematically in Figure 3.9(c). For this condition, the incremental channel conductance at the drain is zero, which means that the slope of the i_D versus v_{DS} curve is zero. We can write

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN} \tag{3.1(a)}$$

or

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN} \tag{3.1(b)}$$

where $v_{DS}(\text{sat})$ is the drain-to-source voltage that produces zero inversion charge density at the drain terminal.

When v_{DS} becomes larger than $v_{DS}(\text{sat})$, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, are injected into the space-charge region, where they are swept by the E-field to the drain contact. In the ideal MOSFET, the drain current is constant for $v_{DS} > v_{DS}(\text{sat})$. This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region**, which is shown in Figure 3.9(d).

As the applied gate-to-source voltage changes, the i_D versus v_{DS} curve changes. In Figure 3.8, we saw that the initial slope of i_D versus v_{DS} increases as v_{GS} increases. Also, Equation (3.1(b)) shows that $v_{DS}(\text{sat})$ is a function of v_{GS}. Therefore, we can generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure 3.10.

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I-V equation relations for NMOS - E type :

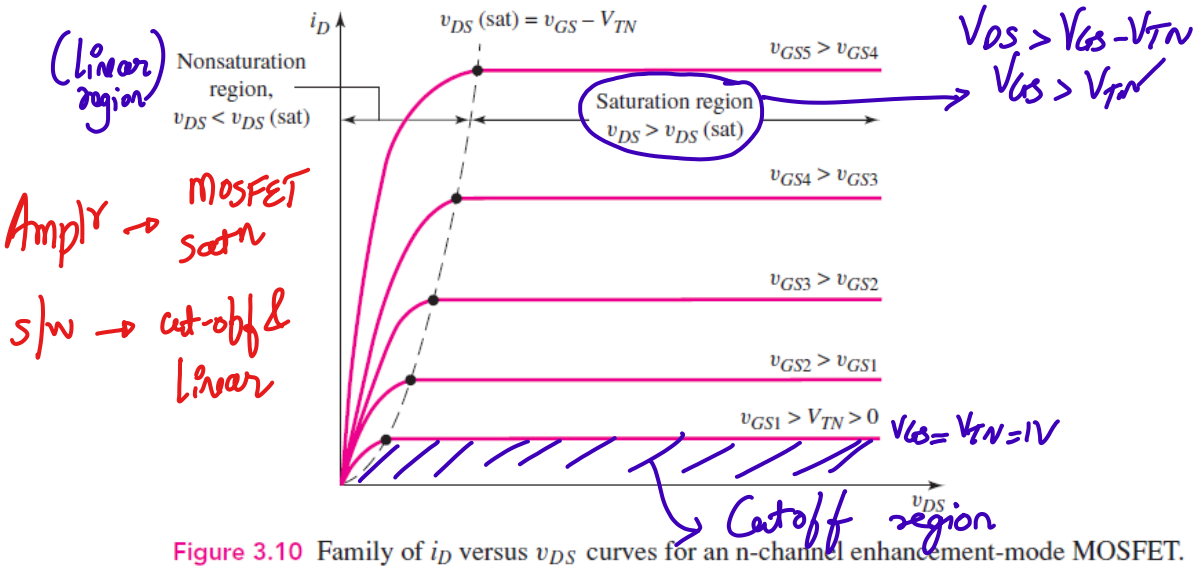

Figure 3.10 Family of i_D versus v_{DS} curves for an n-channel enhancement-mode MOSFET. Note that the v_{DS}(sat) voltage is a single point on each of the curves. This point denotes the transition between the nonsaturation region and the saturation region

The region for which $v_{DS} < v_{DS}$(sat) is known as the **nonsaturation** or **triode region.** The ideal current–voltage characteristics in this region are described by the equation

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \quad \text{(3.2(a))}$$

→ Linear region

In the saturation region, the ideal current–voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation

$$i_D = K_n(v_{GS} - V_{TN})^2 \quad \text{(3.2(b))}$$

→ Satn region

The parameter K_n is sometimes called the transconduction parameter for the n-channel device.

for an n-channel device K_n is given by

$$K_n = \frac{W\mu_n C_{ox}}{2L} \quad \text{(3.3(a))}$$

where C_{ox} is the oxide capacitance per unit area. The capacitance is given by

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. The parameter μ_n is the mobility of the electrons in the inversion layer. The channel width W and channel length L

We can rewrite the conduction parameter in the form

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} \quad \text{(3.3(b))}$$

where $k_n' = \mu_n C_{ox}$ and is called the **process conduction parameter.** Normally, k_n' is considered to be a constant for a given fabrication technology, so Equation (3.3(b)) indicates that the width-to-length ratio W/L is the transistor design variable.

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DRAW below Diagrams 3.14 and include in your answer while explaining if possible

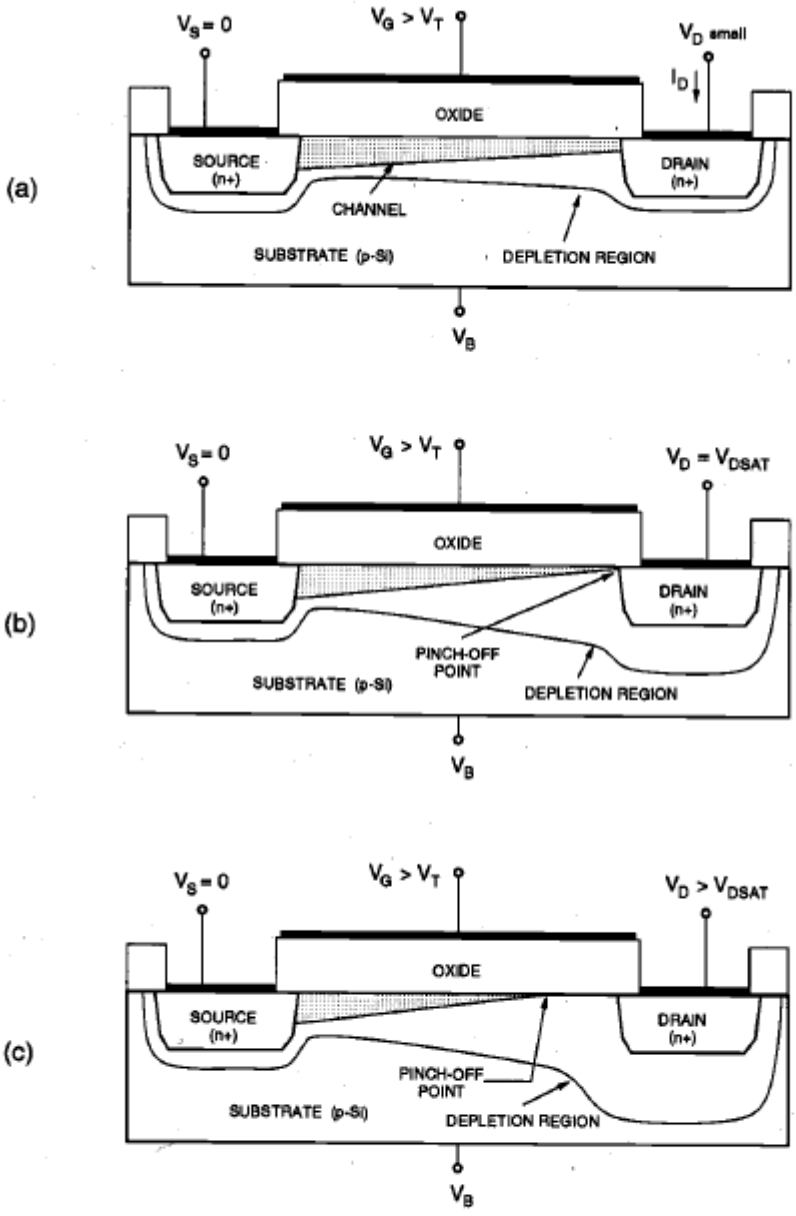

Figure 3.14. Cross-sectional view of an n-channel (nMOS) transistor, (a) operating in the linear region, (b) operating at the edge of saturation, and (c) operating beyond saturation.

INCLUDE the beyond saturation para given below too

Beyond Saturation region i.e $v_{DS} > v_{DS}(\text{sat})$ **and** $v_{DS}(\text{sat}) = v_{GS} - V_{TN}$

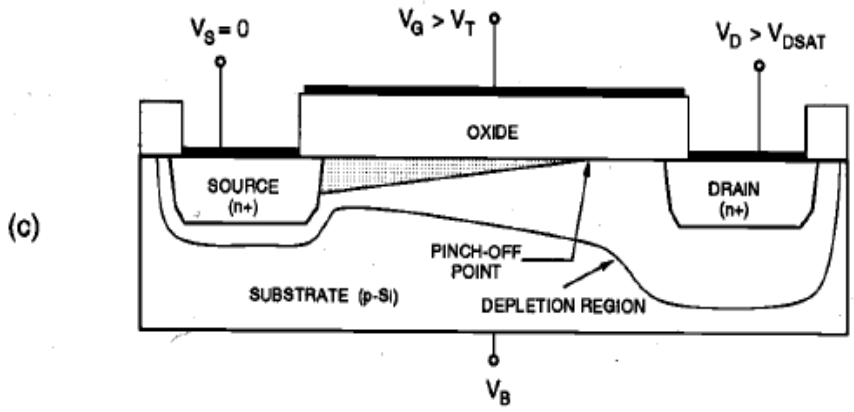

Figure 3.14. Cross-sectional view of an n-channel (nMOS) transistor, (c) operating beyond saturation.

Beyond the pinch-off point, i.e., for $V_{DS} > V_{DSAT}$, a depleted surface region forms adjacent to the drain, and this depletion region grows toward the source with increasing drain voltages. This operation mode of the MOSFET is called the *saturation mode* or the *saturation region*. For a MOSFET operating in the saturation region, the effective channel length is reduced as the inversion layer near the drain vanishes, while the channel-end voltage remains essentially constant and equal to V_{DSAT} (Fig. 3.14(c)). Note that the pinched-off (depleted) section of the channel absorbs most of the excess voltage drop $(V_{DS} - V_{DSAT})$ and a high-field region forms between the channel-end and the drain boundary. Electrons arriving from the source to the channel-end are injected into the drain-depletion region and are accelerated toward the drain in this high electric field, usually reaching the drift velocity limit. The pinch-off event, or the disruption of the continuous channel under high drain bias, characterizes the saturation mode operation of the MOSFET.

TRANSFER CHARACTERISTICS DERIVED FROM OUTPUT CURVE:

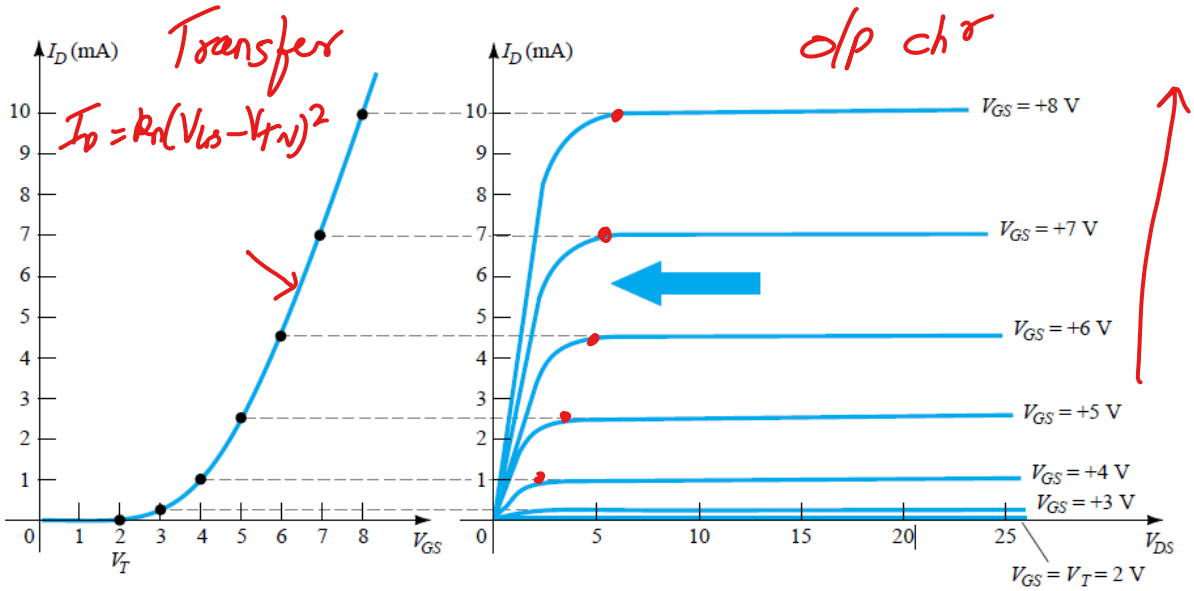

Figure 5.35 Sketching the transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics.

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (5.13)] where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

$I_D = k_n(V_{GS} - V_T)^2$

$k_n = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$

NOTE: k here is also denoted as k_n