Metal oxide Semiconductor Field effect transistor: Basic structure, working of n channel MOSFET Depletion type and study of output and transfer characteristics.

Reference: Boylestad, "Electronic devices and Circuit theory"

METAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

6.7 DEPLETION-TYPE MOSFET

As noted in the introduction, there are three types of FETs: JFETs, MOSFETs, and MESFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation; the name MOSFET stands for *m*etal–*o*xide–*s*emiconductor *f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at I_{DSS}, and also has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 6.27. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that in Fig. 6.27. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric*, which sets up opposing (as indicated by the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations.

Basic Operation and Characteristics

In Fig. 6.28 the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 6.29.

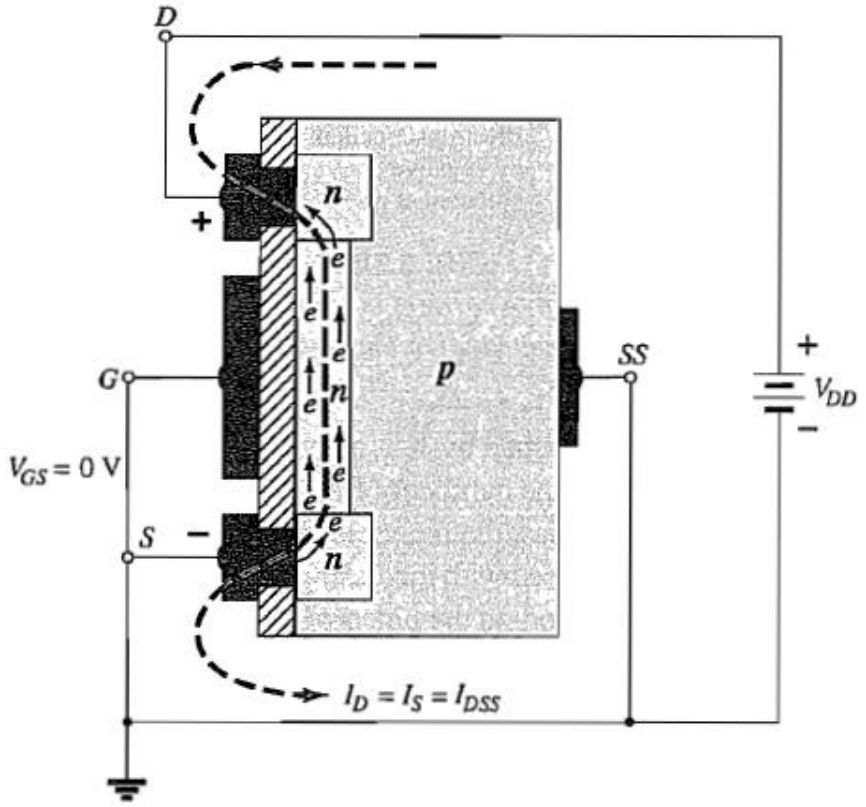

FIG. 6.28

n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and applied voltage V_{DD}.

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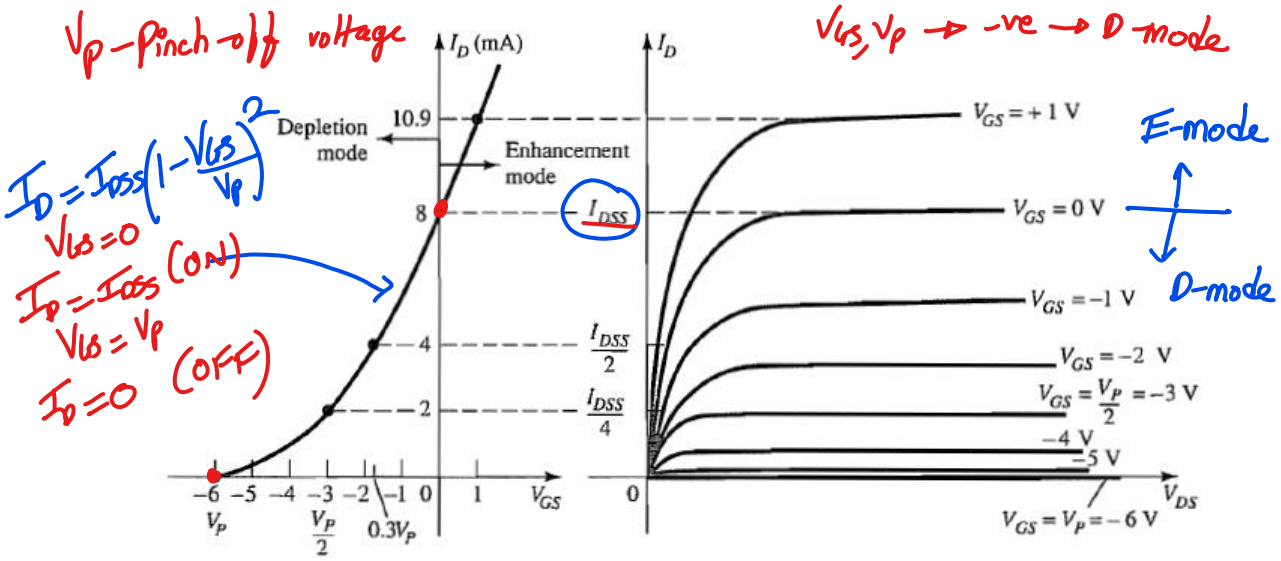

FIG. 6.29

Drain and transfer characteristics for an n-channel depletion-type MOSFET.

In Fig. → V_{GS} is set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 6.29 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.29 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 6.29 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 6.29, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region*.

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.