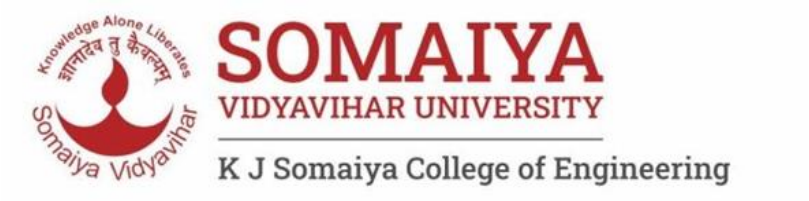

Syllabus

Honour Programme in

VLSI

(Programme commenced from AY 2024-25)

(Department of Electronics and Computer Engineering)

From

Academic Year 2024-25

(SVU-KJSCE 2.0)

(Approved by BOS dated _____, FOET dated _____,

and AC dated _____, Item No. _____)

Somaiya Vidyavihar University
K. J. Somaiya College of Engineering, Mumbai -77
(A Constituent College of Somaiya Vidyavihar University)

Honour Programme in VLSI
Teaching and Credit Scheme

Course Code	Course Category	Course Name	Teaching Scheme (Hrs.) TH – P – TUT	Total (Hrs.)	Credits Assigned TH – P – TUT	Total Credits	Semester of Major Degree
216H26C301	PC	Modern Semiconductor Devices for Integrated Circuits	3-0-0	03	3-0-0	03	III
216H26L301	PC	Modern Semiconductor Devices for Integrated Circuits Laboratory	0-2-0	02	0-1-0	01	III
216H26C401	PC	Digital Design Using Verilog HDL	3-0-0	03	3-0-0	03	IV
216H26L401	PC	Digital Design Using Verilog HDL Laboratory	0-2-0	02	0-1-0	01	IV
216H26C501	PC	Digital IC Design	3-0-0	03	3-0-0	03	V
216H26L501	PC	Digital IC Design Laboratory	0-2-0	02	0-1-0	01	V
216H26C601	PC	FPGA Based Design	3-0-0	03	3-0-0	03	VI
216H26C701	PC	Analog IC Design	3-0-0	03	3-0-0	03	VII
Total			**15-06-0**	**21**	**15-03-0**	**18**	

Evaluation Scheme

Course Code	Course Category	Course Name	LAB/TUT CA	CA		ESE	Total
				IA	ISE		
216H26C301	PC	Modern Semiconductor Devices for Integrated Circuits	--	20	30	50	100
216H26L301	PC	Modern Semiconductor Devices for Integrated Circuits Laboratory	50	--	--	--	50
216H26C401	PC	Digital Design Using Verilog HDL	--	20	30	50	100
216H26L401	PC	Digital Design Using Verilog HDL Laboratory	50	--	--	--	50
216H26C501	PC	Digital IC Design	--	20	30	50	100

216H26L501	PC	Digital IC Design Laboratory	50	--	--	--	50
216H26C601	PC	FPGA Based Design	--	20	30	50	100
216H26C701	PC	Analog IC Design	--	20	30	50	100
Total			**150**	**100**	**150**	**250**	**650**

Course Code	**Course Title**				
216H26C301	**Modern Semiconductor Devices for Integrated Circuits**				
	TH		**P**	**TUT**	**Total**
Teaching Scheme(Hrs.)	**03**		**–**	**–**	**03**
Credits Assigned	**03**		**–**	**–**	**03**
Examination Scheme	**Marks**				
	CA		**ESE**	**LAB/TUT CA**	**Total**
	ISE	**IA**			
	30	**20**	**50**	**--**	**100**

Course prerequisites: None

Course Objectives:
1. To deliver the knowledge about physics of basic semiconductor devices
2. To enhance comprehension capabilities of students through understanding of electronic devices
3. To introduce and motivate students to the use of advanced microelectronic devices
4. To create foundation for forthcoming circuit design courses

Course Outcomes

At the end of completing the course the student will be able to

CO1: Understand the fundamentals of Semiconductor physics
CO2: Ability to understand semiconductor devices through energy band diagrams
CO3: Ability to analyze characteristics of semiconductor junctions
CO4: Ability to differentiate between bipolar and unipolar conduction
CO5: Ability to understand physics of optical devices

Module No.	Unit No.	Topics	Hrs.	CO
1	**Semiconductor Physics**		**04**	**CO1**
	1.1	Evolution and uniqueness of Semiconductor Technology, Equilibrium carrier concentration, Thermal Equilibrium and wave particle duality, Intrinsic semiconductor and Extrinsic semiconductor, Energy band diagram.		
	1.2	Carrier transport, Random motion, Drift and diffusion, Excess carriers, Injection level, Carrier Lifetime, Direct and indirect semiconductors		
2	**PN Junction**		**14**	**CO2 CO3**
	2.1	**PN junction Diode:** Device Structure and fabrication, Energy Band Diagrams, Zero Applied Bias, Forward Applied Bias, Reverse Applied Bias, PN Junction current, DC forward and reverse characteristics, Small-signal equivalent circuit. (Numerical's expected)		
	2.2	**Metal Semiconductor junction:** Schottky barrier diode: V-I characteristics**,** Metal-semiconductor ohmic contacts		
	2.3	**Heterojunctions:** Heterojunction materials, Energy Band Diagrams, Two dimensional electron gas.		
3	**Bipolar Junction Transistor**		**10**	**CO2 CO3 CO4**
	3.1	BJT device structures and fabrication, Transistor Action, minority carrier distribution, Common emitter DC characteristics, Ebers-Moll Model, Hybrid-Pi model		
	3.2	HBT (Heterojunction bipolar transistor): Current gain in HBT, Basic n-p-n HBT structure with band diagram		
4	**Metal Oxide Field Effect Transistor**		**12**	**CO2 CO3**
	4.1	MOS capacitor, energy band diagrams, band bending, flat band voltage, threshold voltage, body effect (Numerical's expected)		
	4.2	MOSFET Device structure and fabrication, MOSFET linear and saturated operation (GCA), Channel length modulation, MOSFET capacitance, Small Signal equivalent circuit. (Numerical's expected)		
5	**Optical Devices**		**05**	**CO5**
	5.1	**Optical absorption:** Photon absorption coefficient, EHP generation rate.		

		Solar Cells: The pn junction, heterojunction and amorphous silicon solar cells		
	5.2	**Optocouplers:** Operation, construction, specifications and applications		
	Self-learning topics#			
		Applications of modern semiconductor devices. Semiconductor Technology trend FinFETs, GAA FET		
		Total	**45**	

Recommended Books:

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with Country	Edition with Year of Publication
1.	Donald A. Neamen	*Semiconductor Physics and Devices*	Tata McGraw Hill, India	4th Edition, 2017
2.	S. M. Sze	*Semiconductor Devices: Physics and Technology*	Wiley Education, India	3rd Edition, 2016
3.	Sung-Mo Kang,Yusuf Leblebici	*CMOS Digital Integrated Circuits*	Tata McGraw Hill, India	4th Edition, 2018
4.	David Bell	*Electronic Devices and Circuits*	Oxford, India	5^{th} Edition, 2008

<table>
<tr><th>Course Code</th><th colspan="5">Course Title</th></tr>
<tr><td>216H26L301</td><td colspan="5">Modern Semiconductor Devices for Integrated Circuits Laboratory</td></tr>
<tr><td></td><td colspan="4">TH</td><td>Total</td></tr>
<tr><td>Teaching Scheme(Hrs.)</td><td colspan="4">–</td><td>02</td></tr>
<tr><td>Credits Assigned</td><td colspan="4">–</td><td>01</td></tr>
<tr><td rowspan="3">Examination Scheme</td><td colspan="5">Marks</td></tr>
<tr><td rowspan="2">LAB / TUT CA</td><td colspan="2">CA</td><td rowspan="2">ESE</td><td rowspan="2">Total</td></tr>
<tr><td>ISE</td><td>IA</td></tr>
<tr><td>50</td><td>–</td><td>–</td><td>--</td><td>50</td></tr>
</table>

Distribution of Lab CA:

Criteria	Marks
Experiments performed, journal completion and viva	30
Quiz based on experiments conducted	20
Total	50

Term work will consist of experiments covering the entire syllabus of **"Modern Semiconductor Devices for Integrated Circuits"** (**216H26C301**). Students will be graded based on continuous assessment of their term work. Practical and oral examinations will be based on laboratory work and the entire syllabus.

Course Code	Course Title				
216H26C401	Digital Design Using Verilog HDL				
	TH		P	TUT	Total
Teaching Scheme(Hrs.)	03		–	–	03
Credits Assigned	03		–	–	03
Examination Scheme	Marks				
	CA		ESE	LAB/TUT CA	Total
	ISE	IA			
	30	20	50	--	100

Course prerequisites: Basic digital design

Course Objectives:
1. To know the basic language features of Verilog HDL and the role of HDL in digital logic design.
2. To know the behavioral modeling of combinational and simple sequential circuits.
3. To know the behavioral modeling of algorithmic state machines.
4. To know the synthesis of combinational and sequential descriptions.
5. To know the architectural features of programmable logic devices.

Course Outcomes

At the end of completing the course the student will be able to

CO1. Understand the language constructs and programming fundamentals of Verilog HDL.
CO2. Choose the suitable abstraction level for a particular digital design
CO3. Construct Combinational and sequential circuits in different modelling styles using
CO4. Analyse and Verify the functionality of digital circuits/systems using test benches

Module No.	Unit No.	Topics	Hrs.	CO
1	**Introduction to Verilog HDL**		10	CO1 CO2
	1.1	Verilog as HDL, Levels of Design Description, Concurrency, Program structure		
	1.2	Top-down and Bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block, Verilog Data types and Operators, system tasks, compiler directives		

2	**Gate-Level Modelling**		**10**	**CO3**
	2.1	Modelling using basic Verilog gate Primitives, Description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.		
	2.2	Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Gate-level Modelling		
3	**Dataflow Modelling**		**08**	**CO3**
	3.1	Continuous assignments, Delay specification, expressions, operators.		
	3.2	Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in dataflow model		
4	**Behavioral Modelling**		**10**	**CO4**
	4.1	Procedural Assignments, Initial and always blocks, blocking and non-blocking statements, delay control, conditional statements, Multiway branching, loops, sequential and parallel blocks		
	4.2	Design of Decoders, Multiplexers, Flip-flops, Registers & Counters in Behavioral model.		
5	**Components Test and Verification**		**07**	**C05**
	5.1	Test Bench - Combinational Circuits Testing, Sequential Circuits Testing, Test Bench Techniques.		
	5.2	Design Verification, Assertion Verification.		
		Total	**45**	

Recommended Books:

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with Country	Edition with Year of Publication
1.	Samir Palnitkar	*Verilog HDL: A Guide to Digital Design and Synthesis*	Pearson Education, India	2nd Edition, 2009
2.	Michel D. Ciletti	*Advanced Digital Design with Verilog HDL*	PHI, India	2nd Edition, 2009
3.	Padmanabhan, Tripura Sundari	*Design through Verilog HDL*	Wiley, India	2016
4.	S.Brown, Zvonko – Vranesic	*Fundamentals of Digital Logic with Verilog Design*	McGraw Hill, India	3rd Edition, 2014

Course Code	Course Title				
216H26L401	Digital Design Using Verilog HDL Laboratory				
	TH				Total
Teaching Scheme(Hrs.)	–				02
Credits Assigned	–				01
Examination Scheme	Marks				
	LAB / TUT CA	CA		ESE	Total
		ISE	IA		
	50	–	–	–	50

Distribution of Lab CA:

Criteria	Marks
Experiments performed, journal completion and viva	30
Quiz based on experiments conducted	20
Total	50

Term work will consist of experiments covering the entire syllabus of "**Digital Design Using Verilog HDL"** (**216H26C401**). Students will be graded based on continuous assessment of their term work. Practical and oral examinations will be based on laboratory work and the entire syllabus.

Course Code	Course Title				
216H26C501	Digital IC Design				
	TH		P	TUT	Total
Teaching Scheme(Hrs.)	03		--	--	03
Credits Assigned	03		--	--	03
Examination Scheme	Marks				
	CA		ESE	LAB/CA TW	Total
	ISE	IA			
	30	20	50	--	100

Course prerequisites:
Semiconductor Devices, Foundations of Microelectronics

Course Objectives:
This course aims to equip the students with a comprehensive understanding of digital IC design. Students will learn fundamental principles, including transistor-level design, logic families, and gate sizing. The students will develop skills in analyzing and designing basic and advanced digital circuits like inverters, transmission gates, and dynamic logic circuits. Emphasis will be on optimizing transistor sizing for performance and power. By the end of the course, students will be proficient in tackling complex datapath design challenges and integrating various methodologies. This prepares them to excel in real-world scenarios in VLSI design and technology, balancing theoretical knowledge with practical application
.

Course Outcomes
At the end of the successful completion of the course, the student will be able to
CO1: Understand the fundamental principles of digital IC design, including transistor-level design, logic families, and gate sizing
CO2: Design basic digital circuits such as inverters, transmission gates, and pass-transistor logic for various applications.
CO3: Apply advanced techniques in digital IC design, including dynamic and domino logic circuits
CO4: Evaluate transistor sizing in digital IC design for performance, power, and area considerations for optimization
CO5: Design complex data path circuits using appropriate methodologies

Module No.	Unit No.	Details	Hrs.	CO
1	**Introduction to Digital IC Design**		06	CO1
	1.1	Overview of Digital IC design process, Introduction to digital IC Design flow, Stages in the design process. **Technology Scaling:** Types of scaling		
	1.2	Basics of CMOS Technology, CMOS Fabrication Process, MOSFET operation principles, CMOS logic gates		
	1.3	Introduction to CAD Tools for Digital IC Design, Introduction to simulation tools, Introduction to layout tools		
2	**Basic Digital Circuit Design**		09	CO2

	2.1	Inverter Characteristics, CMOS Inverter Operation, Voltage Transfer Characteristics, Noise Margins and Power consumption		
	2.2	Transmission Gate (TG) and Pass Transistor Logic (PTL) Design, Design of Combinational and Sequential Circuits using TG and PTL, Limitations of TG and PTL		
3	**Advanced Logic Circuit Design**		**09**	**CO3**
	3.1	Dynamic and Domino Logic Circuits: Operation and Design considerations, NORA, Zipper Design styles.		
	3.2	Clocking strategies in VLSI circuits, Clocked CMOS Circuits, Implementation of Flip-Flops using Dynamic Logic		
4	**Transistor Sizing and Layout Design**		**09**	**CO4**
	4.1	Gate sizing methodologies for performance optimization, Buffer insertion techniques, Delay modeling, and analysis in gate sizing		
	4.2	Layout Design for Digital ICs, Layout Design Rules and Guidelines, Layout optimization techniques for performance, power, and area		
5	**Data path Design**		**09**	**CO5**
	5.1	Bit adder circuits, Ripple carry adder, CLA adder, Design of 1-bit Full CLA Adder using Mirror Circuit		
	5.2	Partial-product generation, partial-product accumulation, final addition, barrel shifter		
	5.3	Design of arithmetic and logic units (ALUs) and register files		
		Total	**45**	

Recommended Books:

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with Country	Edition and Year of Publication
1.	Jan M. Rabaey	*Digital Integrated Circuits: A Design Perspective*	Pearson Education, India	*2nd* Edition, 2016
2.	Weste and Harris	*CMOS VLSI Design: A Circuits and Systems Perspective*	Pearson Education, India	4th Edition, 2020
3.	John P. Uyemura	*CMOS Logic Circuit Design*	Springer-Verlag New York, Inc., USA	1st Edition, 2013
4.	D. Ciletti Micahel	*Advanced Digital Design with the Verilog HDL*	Pearson Education, India	2nd Edition, 2017
5.	Sung-Mo Kang	*CMOS Digital Integrated Circuits*	Mc-Graw Hill, India	4th Edition, 2019

Course Code	Course Title				
216H26L501	Digital IC Design Laboratory				
	TH		P	TUT	Total
Teaching Scheme(Hrs.)	--		02	--	02
Credits Assigned	--		01	--	01
Examination Scheme	Marks				
	CA		ESE	LAB/CA TW	Total
	ISE	IA			
	--	--	--	50	50

Lab CA will comprise of a variety of components such as quizzes, onscreen exam, viva-voce, journal, etc. covering the entire syllabus of "**Digital IC Design**" (**216H26C102**) Details will be shared by the course teachers at the beginning of every semester.

Course Code	Course Title				
216H26C601	FPGA based Design				
	TH		P	TUT	Total
Teaching Scheme(Hrs.)	03		–	--	03
Credits Assigned	03		--	–	03
Examination Scheme	Marks				
	CA		ESE	LAB/TUT CA	Total
	ISE	IA			
	30	20	50	--	100

Course prerequisites: Digital Design

Course Objectives: Digital designs once built-in custom silicon is increasingly implemented in field programmable gate arrays (FPGAs), but effective FPGA system design requires an understanding of new techniques developed for FPGAs. This course deals with basic digital system design, Introduction to ROM, PLDs, CPLDs, FPGA fabrics and introduces essential FPGA concepts and programming. This course is appropriate for all the students interested in digital systems applications, FPGA programming. The course covers the technological background of FPGA both theoretically as well as practical implementation of digital solutions.

Course Outcomes

At the end of completing the course the student will be able to

CO1. Explain logic synthesis techniques – two level and multilevel synthesis
CO2. Design systems using FPGAs and CPLDs.
CO3. Design sequential machine design using FPGAs.
CO4. Design systems for low power operation.

Module No.	Unit No.	Topics	Hrs.	CO
1	**Programmable Logic Devices**		11	CO1
	1.1	Logic design fundamentals: Two level synthesis – SOP/POS forms, Logic minimization, Limitations of two level synthesis, introduction to multi-level synthesis.		
	1.2	Programmable Logic Array (PLA) architecture; Programmable Array Logic (PAL), PAL vs. PROM, Fan-in expansion feature, Architecture for sequential circuit implementation, Typical PAL chips; Complex Programmable Logic Devices (CPLD)		

2	**Programmable Gate Arrays:**		**07**	**CO2**
	2.1	Gate Array concept, Mask programmable and Field Programmable Gate Arrays; Look up tables (LUT) Configurable logic blocks (CLB), logic design using LUT's;		
	2.2	Multi-level synthesis techniques – Factoring and Functional decomposition, Shannon's Expansion Theorem; Generalized FPGA Architecture.		
3	**Sequential Circuit Design**		**06**	**CO3**
	3.1	Finite State Machines, Moore and Mealy Machines; State diagrams, State table, State assignment, derivation of next-state and output expressions, state minimization; State assignment for low power operation, CAD tools for FSM synthesis.		
	3.2	Advanced features of modern FPGAs: Block RAMs, Embedded processor, Communication ports, Analog interface.		
	3.3	Typical case studies: Simple logic functions – Decoder, encoder, multiplexer, demultiplexer, BCD to seven-segment decoder, keyboard/display interface; memory elements and arrays; sequential machine design – sequence generators, timing generators, a typical machine design (example: vending machine); A simple CPU design.		
4	**FPGA as a Hardware Debugging platform**		**11**	**CO4**
	4.1	Hardware troubleshooting methods, Looking into the chip – Logic State Analyzer and its use; Concept of Hardware emulation-simulation vs. Emulation, FPGA as a Hardware emulator, Break-points and their utility, setting break-points in FPGA based design		
	4.2	Design analysis: Static timing analysis, Power analysis, Resource utilization, noise, clock network, DRC, debugging methods.		
		Total	**45**	

Recommended Books:

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with Country	Edition with Year of Publication
1.	S. Brown and Z. Vranesic	*Fundamentals of Digital Logic with Verilog Design*	McGraw Hill Education, India	3rd Edition, 2014

2.	J. Bhasker	*A Verilog HDL Primer*	B.S. Publications, India	Reprint 2023
3.	Cem Unsalan, Bora Tar	*Digital System Design with FPGA: Implementation Using Verilog and VHDL*	McGraw Hill Education, India	1st Edition, 2017
4.	Pong P. Chu	*FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*	Wiley, India	1st Edition, 2008

Course Code	Course Title				
216H26C701	Analog IC Design				
	TH		P	TUT	Total
Teaching Scheme(Hrs.)	03		–	--	03
Credits Assigned	03		--	–	03
Examination Scheme	Marks				
	CA		ESE	LAB/TUT CA	Total
	ISE	IA			
	30	20	50	--	100

Course prerequisites: Semiconductor Devices, Foundations of Microelectronics, Digital IC Design

Course Objectives: The objective of the course is to expose the students to analog VLSI designing. The course discusses the basic building blocks of Analog circuits and their implementation in integrated circuits.

Course Outcomes

At the end of completing the course the student will be able to

CO5. Recognize and analyze tradeoffs in Analog VLSI
CO6. Design of basic building blocks of Analog VLSI Circuits.
CO7. Analyze and design MOSFET-based single-stage and differential amplifiers.
CO8. Analyze and design MOSFET-based operational amplifier

Module No.	Unit No.	Topics	Hrs.	CO
1	**CMOS Analog building blocks**		10	CO1
	1.1	**MOS Models:** Necessity of CMOS Analog design, Analog Design Octagon, MOS small signal model, body effect. **Active Current Mirror circuits:** Basic current mirrors, Cascode current mirrors, and Active current mirrors.		
2	**Single Stage Integrated Circuit Amplifiers**		12	CO2
	2.1	**Configurations:** Basic concepts, Common source stage with different loads, Source follower, and Common gate stage.		
	2.2	Cascode stage, Folded Cascode		

3	**Differential Amplifiers**		**12**	**CO3**
	3.1	Single-ended and differential operation, Basic differential pair, Common-mode response,		
	3.2	Differential pair with MOS loads, Gilbert cell		
4	**MOS Operational Amplifiers**		**11**	**CO4**
	4.1	Op-amp Design: General Considerations, performance parameters, One-stage op-amps, Two-stage op-amps, Gain Boosting, Common-mode feedback, Input range limitations, Slew Rate, Power supply rejection, Noise in op-amps.		
		Total	**45**	

Recommended Books:

Sr. No.	**Name/s of Author/s**	**Title of Book**	**Name of Publisher with Country**	**Edition with Year of Publication**
5.	B Razavi	*Design of Analog CMOS Integrated Circuits*	McGraw Hill Education, India	2nd Edition, 2017
6.	R. Jacob Baker, Harry W. Li, David E. Boyce,	*CMOS Circuit Wiley Design, Layout, and Stimulation*	Wiley, India	Student Edition, 2018
7.	P. E. Allen and D. R. Holberg.	*CMOS Analog Circuit Design*	Oxford University Press, India	3rd Edition, 2012
8.	Gray, Meyer, Lewis, Hurst	*Analysis and design of Analog Integrated Circuits*	Wiley, India	5th Edition, 2009