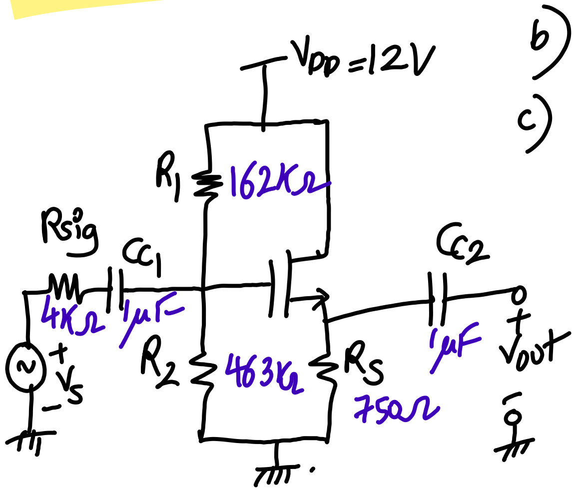
AEC lec 21 — 28/8/23

Numerical 1: Calculate a) small-slg voltage gain
b) I/P impedance
c) O/P impedance



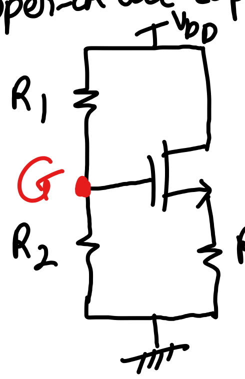
NMOS-E parameters:-
$V_{TN} = 1.5V$
$\lambda = 0.01V^{-1}$
$K_n = 4mA/V^2$

Solution: ① I_{DQ}, V_{GSQ} — 2m ② g_m, r_o — 2m ③ A_V, Z_{in}, Z_{out} — 6m

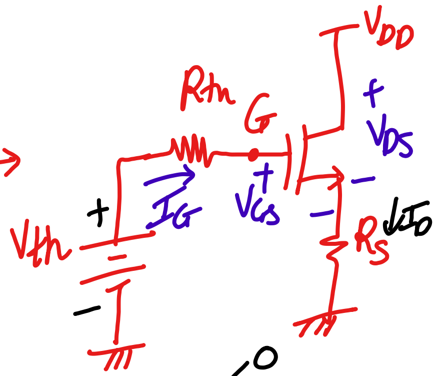
"Common-drain Amplifier"

① DC Analysis:-

① open-ckt all capacitors



T.T →



$$V_{th} = \frac{R_2}{R_1+R_2} \times V_{DD}$$

$$V_{th} = \left(\frac{463}{463+162}\right) \times 12$$

$$V_{th} = \underline{8.89}\ V$$

→ Apply KVL to G-S loop, $V_{th} - \overset{0}{I_G} R_{th} - V_{GS} - I_D R_S = 0$

$$V_{GS} = V_{th} - I_D R_S$$

$$V_{GS} = 8.89 - I_D(750) \quad \text{—} ①$$

→ Assume given device is working in saturation region

$$\therefore I_D = K_n (V_{GS} - V_{TN})^2 = 4\times10^{-3}(V_{GS} - 1.5)^2 \quad \text{—} ②$$

→ Put ② in ①, we get

$$V_{GS} = 8.89 - 3(V_{GS}^2 - 3V_{GS} + 2.25)$$

$$\rightarrow V_{GS} = 8.89 - 3V_{GS}^2 + 9V_{GS} - 6.75$$

$$\rightarrow 3V_{GS}^2 - 8V_{GS} - 2.14 = 0$$

$(\because V_{GS} > V_{TN})$ $\quad V_{GS} = \underline{2.91}\ V$ ✓ $\qquad V_{GS} = \underline{-0.245}\ V$ ✗ (Reject)

$$I_{DQ} = k_n(V_{GS}-V_{TN})^2 = 4\times10^{-3}\times(2.91-1.5)^2$$

$$I_{DQ} = 7.95\,mA$$

② Small-s/g parameters (g_m, r_o)

$$g_m = 2k_n(V_{GS}-V_{TN}) = 2\times4\times10^{-3}(2.91-1.5)$$

$$g_m = 11.28\ \frac{mA}{V}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01\times7.95\times10^{-3}}$$

$$r_o = 12.578\,K\Omega$$

③ A_v, Z_{in} & Z_{out}

98, 24, 25, 82, 44, 101,
88, 97, 100, 78, 80, 41,
67, 16, 7, 45, 4, 85,
54, 50, 40