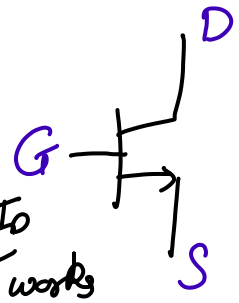
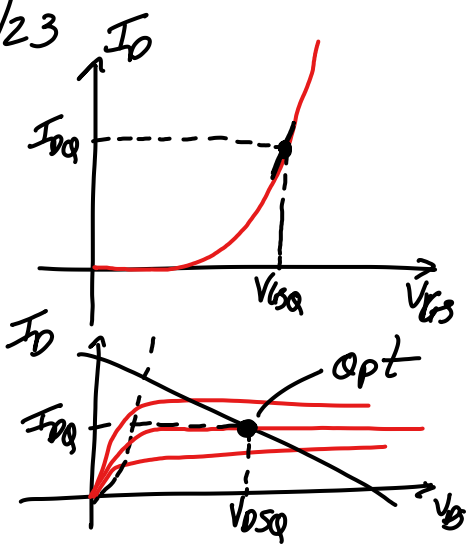
AEC lec 16 21/8/23

MOSFET DC Analysis:

→ Biasing → Setting up V_{GS} & I_D such that MOSFET works in saturation region



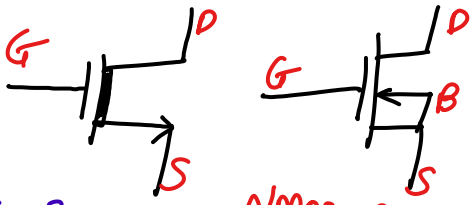


Depletion-MOSFET Biasing:

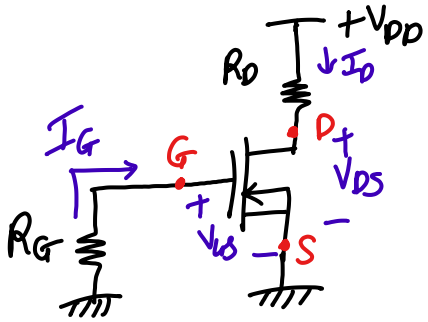
V_{GS}: -ve or +ve or 0 $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

① Zero-bias ($V_{GS}=0$)
② Self-bias (V_{GS} -ve)
③ Voltage-divider bias (V_{GS} +ve)

A] Zero-bias circuit (NMOS-D type):



NMOS-D type



KVL to G-S loop,

$-I_G R_G - V_{GS} = 0$

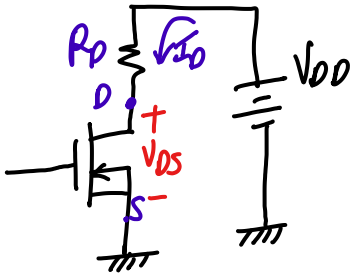
$0 - V_{GS} = 0$

$\boxed{V_{GS} = 0}$

($I_G = 0$ for MOSFET) due to presence of oxide layer

→ $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-0\right)^2$

→ $\boxed{I_D = I_{DSS}}$



KVL to DS loop,

$V_{DD} - I_D R_D - V_{DS} = 0$

$\boxed{V_{DS} = V_{DD} - I_D R_D}$

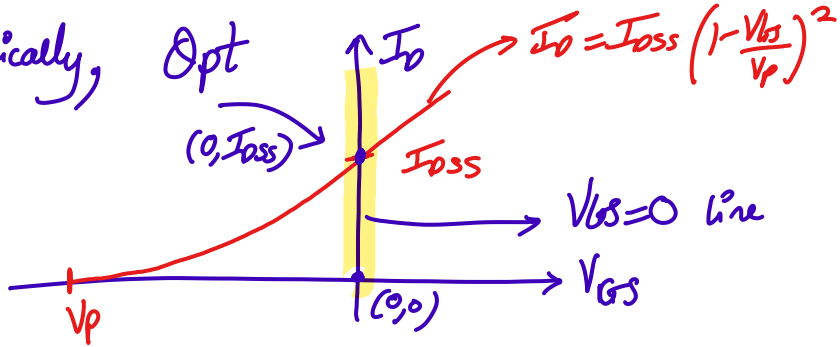
$V_{DS} = V_D - V_S = V_D = V_{DD} - I_D R_D$

To find Q-pt graphically,

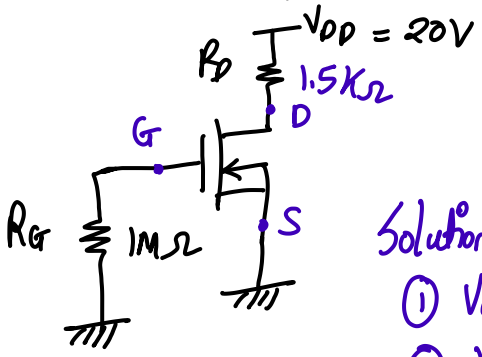
load line: $V_{GS} = 0$

Opt: (V_{GSQ}, I_{DQ})

Opt: $(0, I_{DSS})$



Numerical 1: Find the Qpt & V_{DS} for ckt shown below



$I_{DSS} = 10mA$
$V_p = -4V$

Solution:

① $V_G = 0$, $V_S = 0$

② $V_{GSQ} = 0$

③ $I_{DQ} = I_{DSS} = 10mA$

④ $Qpt \equiv (V_{GSQ}, I_{DQ}) \equiv (0, 10mA)$

⑤ $V_{DS} = V_{DD} - I_D R_D = 20 - 10m \times 1.5K = 5V$

—x—