High-Speed Hybrid-Logic Full Adder Using High-Performance 10-T XOR–XNOR Cell

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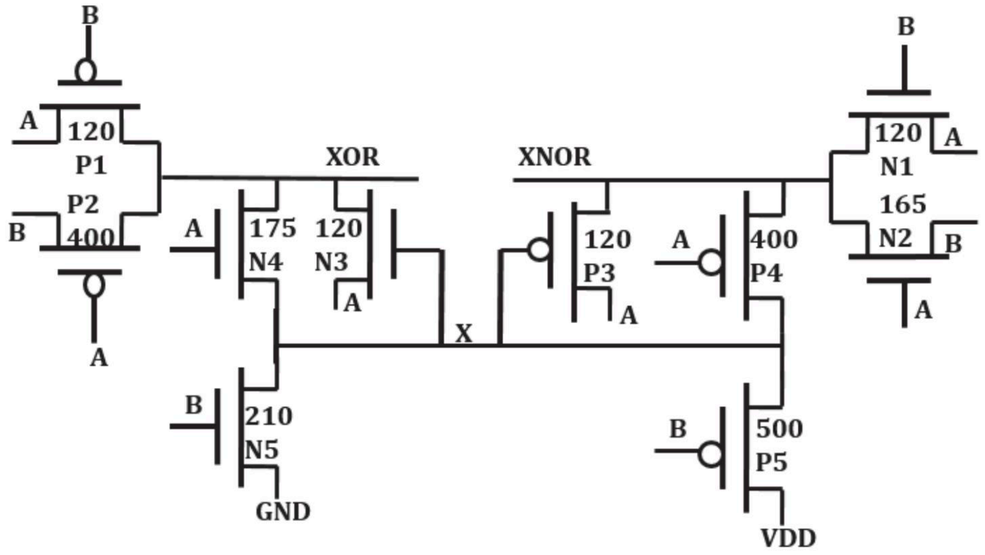
Objectives:

- Implement the High-Speed Hybrid-Logic Full Adder utilizing a 10-Transistor (10-T) 2-input XOR-XNOR cell proposed in the selected research paper.
- Design the Full Adder designs utilizing the implemented 10-Transistor 2-input XOR-XNOR Cell
- Analyze the Delay and Power Consumption Characteristics

Tools Used:

- Cadence Virtuoso

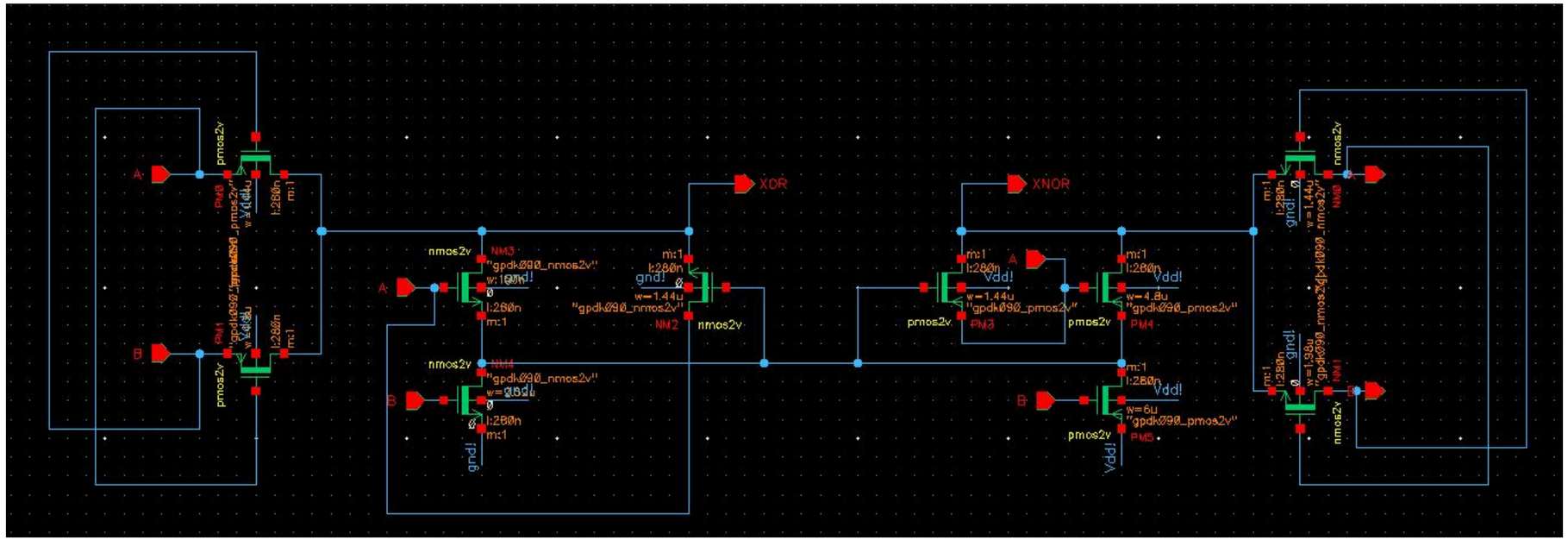
Proposed XOR-XNOR Design:



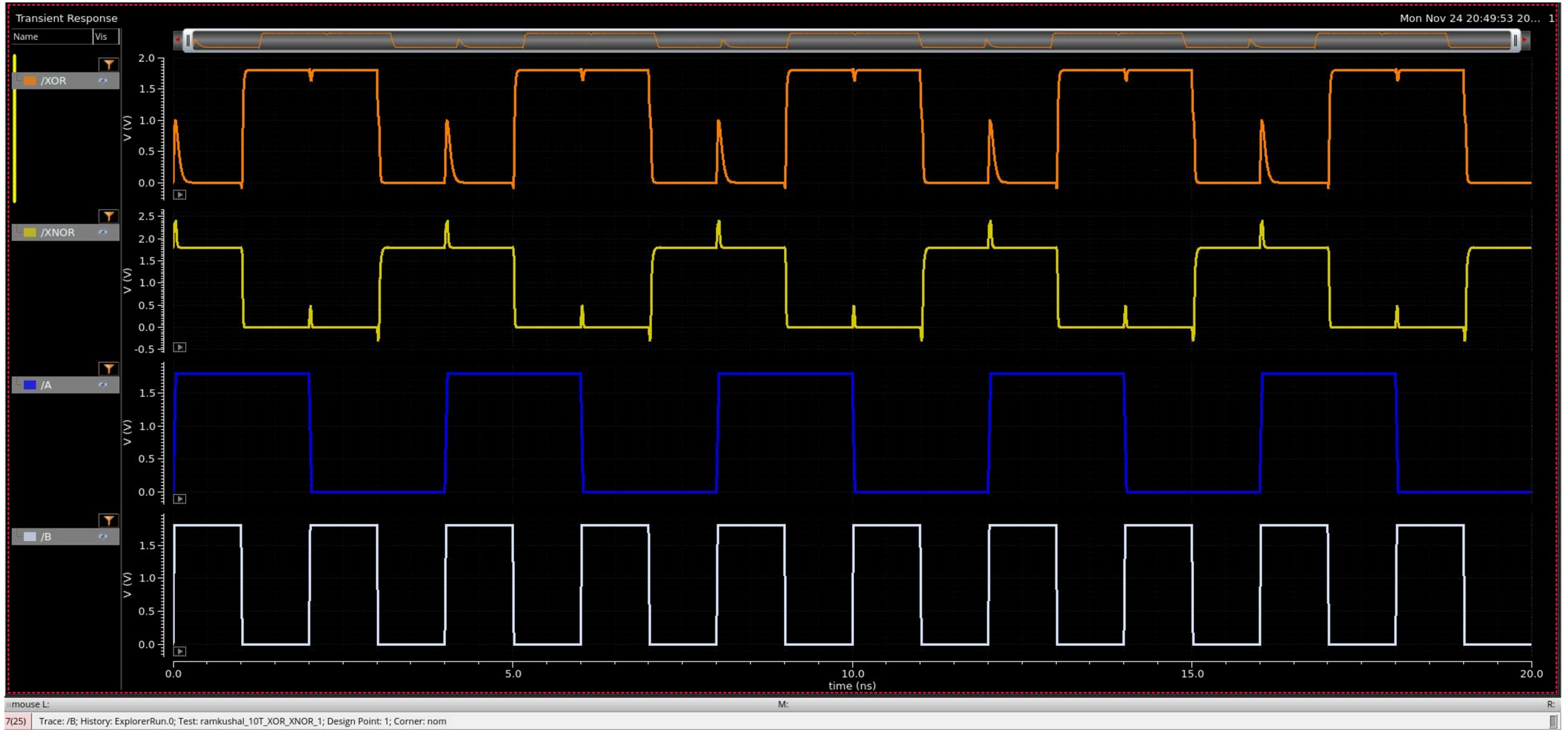
Expected Output:

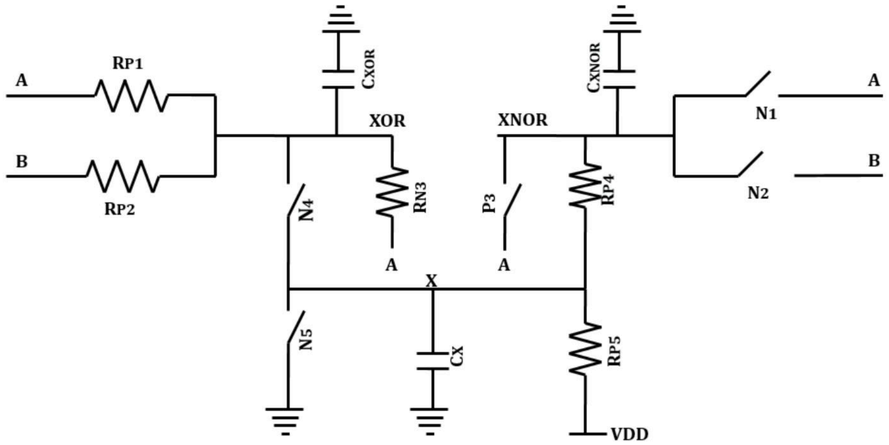
A	B	XOR	XNOR	X
0	0	0	1	X
0	1	1	0	X
1	0	1	0	X
1	1	0	1	X

Proposed XOR-XNOR Design (Transistor Level Schematic)

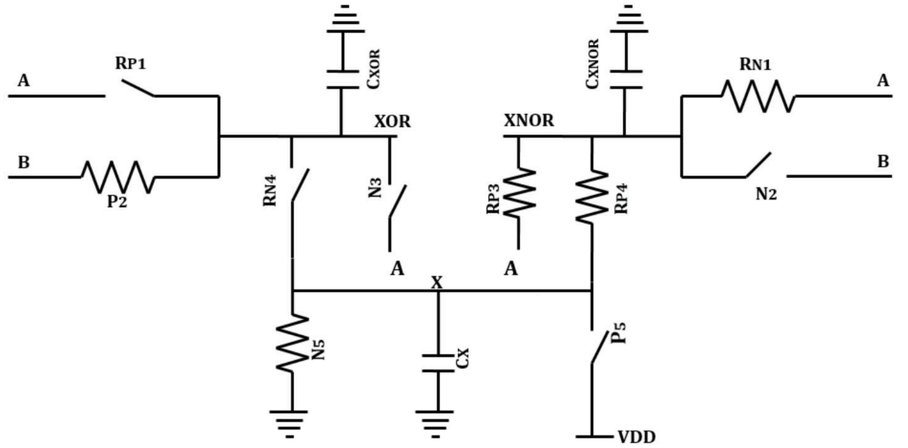


Outputs Obtained :

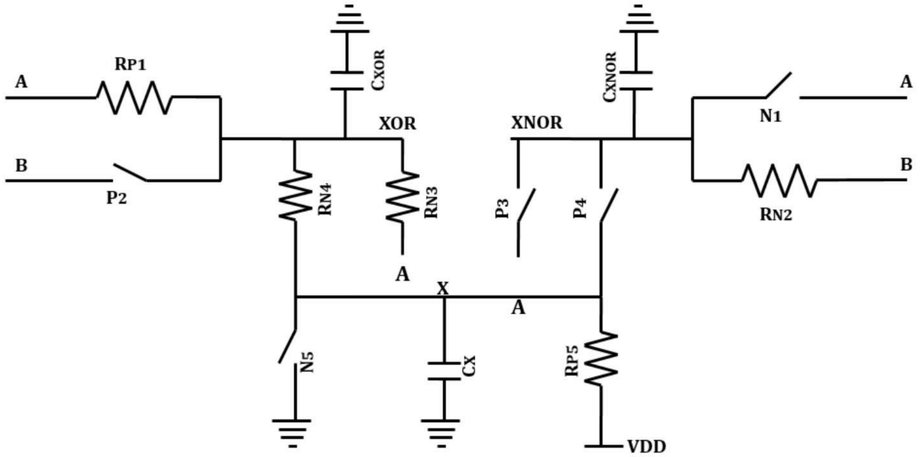




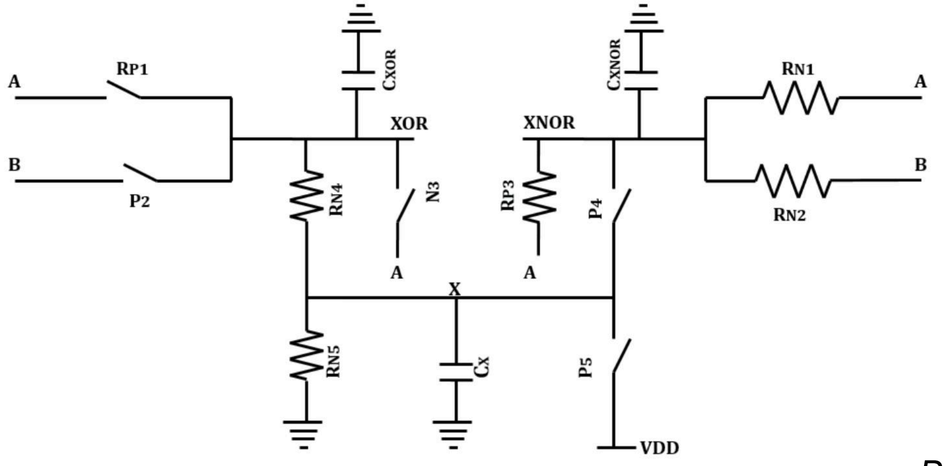
RC delay model for AB : 00



RC delay model for AB : 01

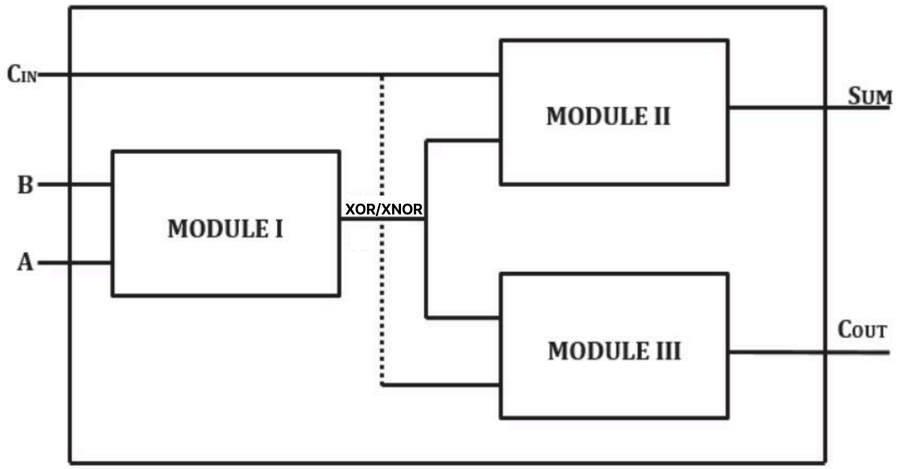


RC delay model for AB : 10



RC delay model for AB : 11

Proposed Top Level Schematic:



Module 1:
Proposed XOR-XNOR Cell

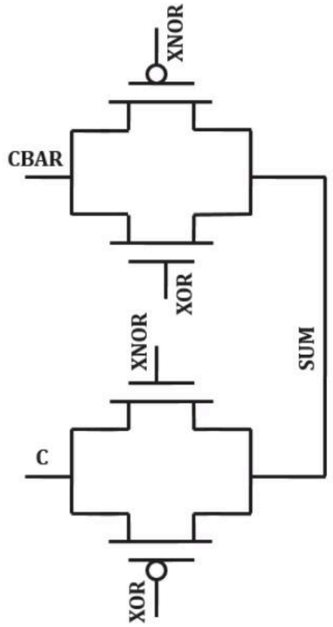
Module 2:
Sum Circuit

$$\mathrm{SUM} = (A \oplus B) \oplus C'_{\mathrm{IN}} + (A \oplus B)' \oplus C_{\mathrm{IN}}.$$

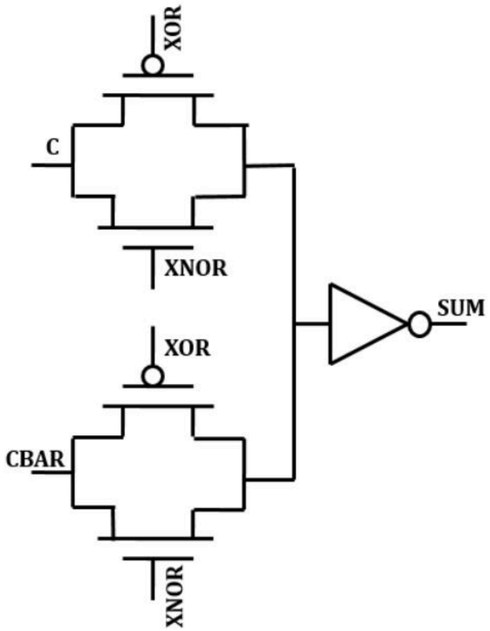
Module 3:
Carry-out Circuit

$$C_{\mathrm{OUT}} = (A \oplus B)'A + (A \oplus B)C_{\mathrm{IN}}.$$

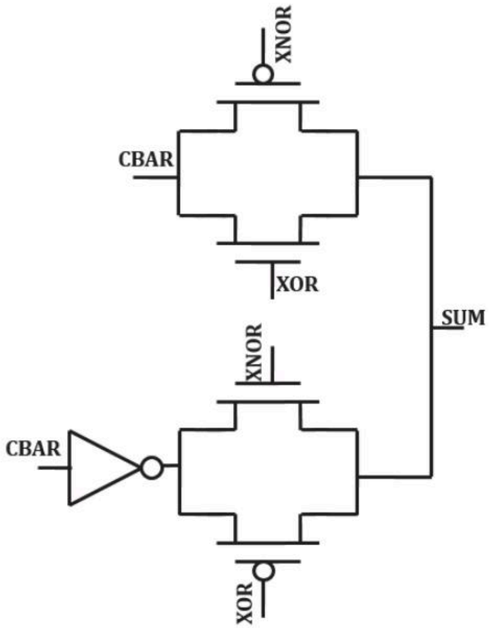
Proposed Module II Designs: (Sum Circuit)



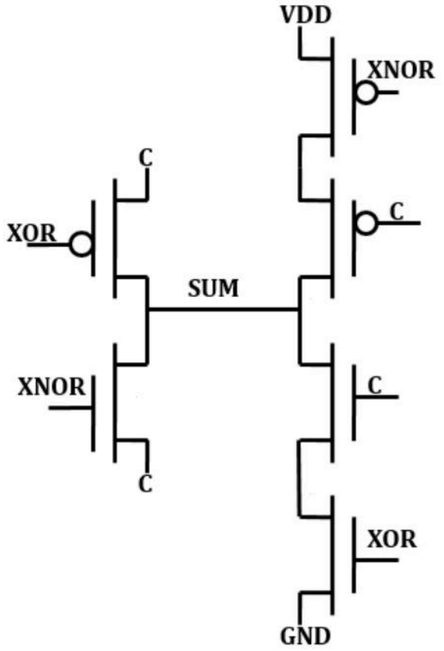
Design 1
Using Transmission Gate (TG)



Design 2*
Using TG with Inverter design 1

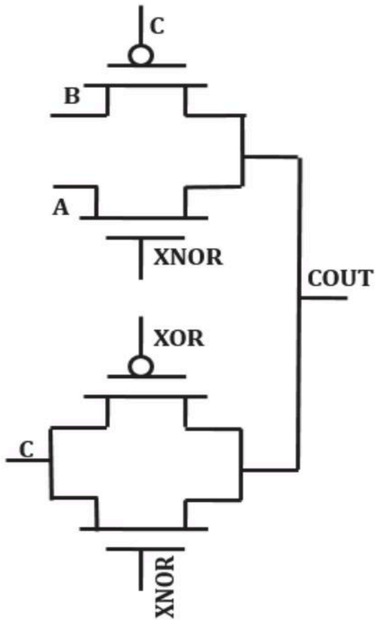


Design 3
Using TG with Inverter design 2

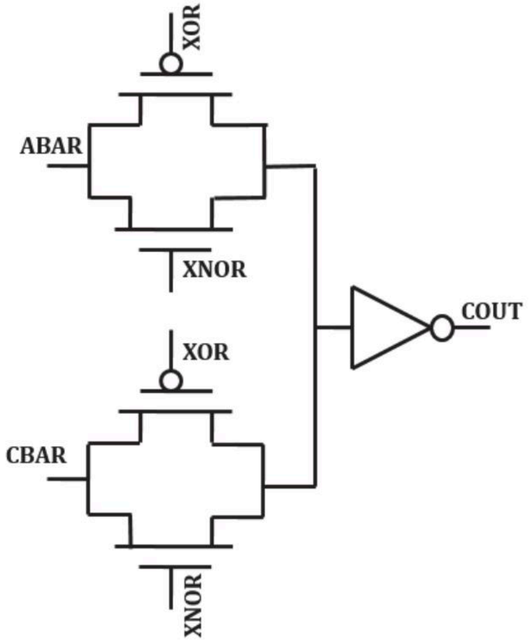


Design 4
Using CMOS

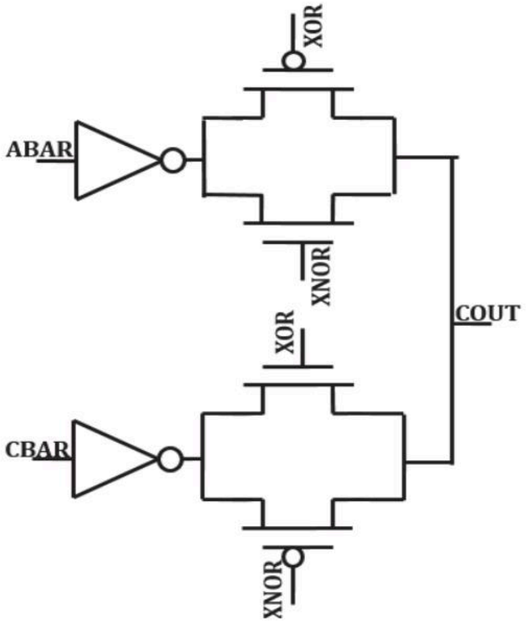
Proposed Module III Designs: (Carry-out Circuit)



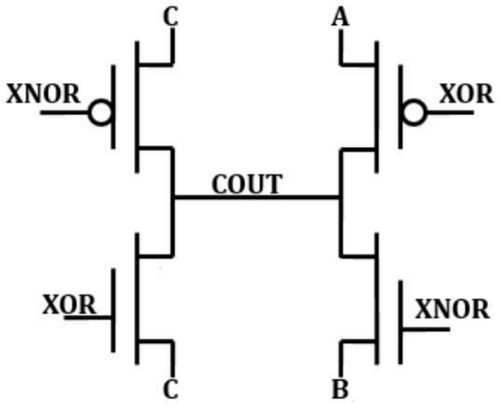
Design 1*
Using Transmission Gate (TG)



Design 2*
Using TG with Inverter design 1

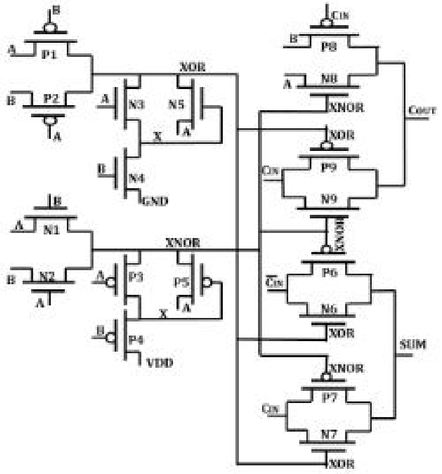


Design 3
Using TG with Inverter design 2

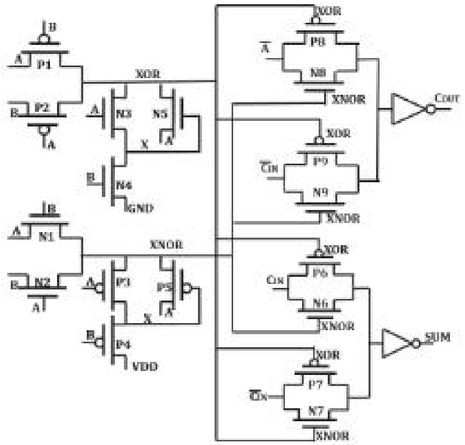


Design 4
Using CMOS

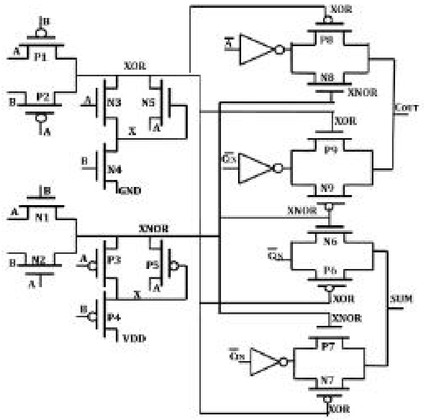
Proposed Full Adder Designs



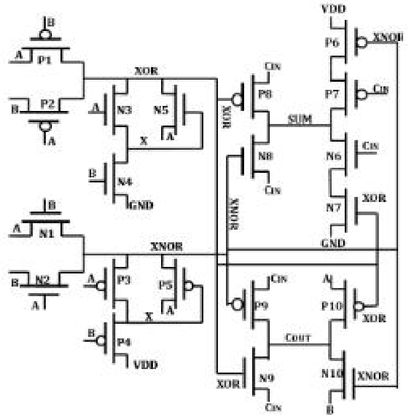
FA - 1



FA - 2

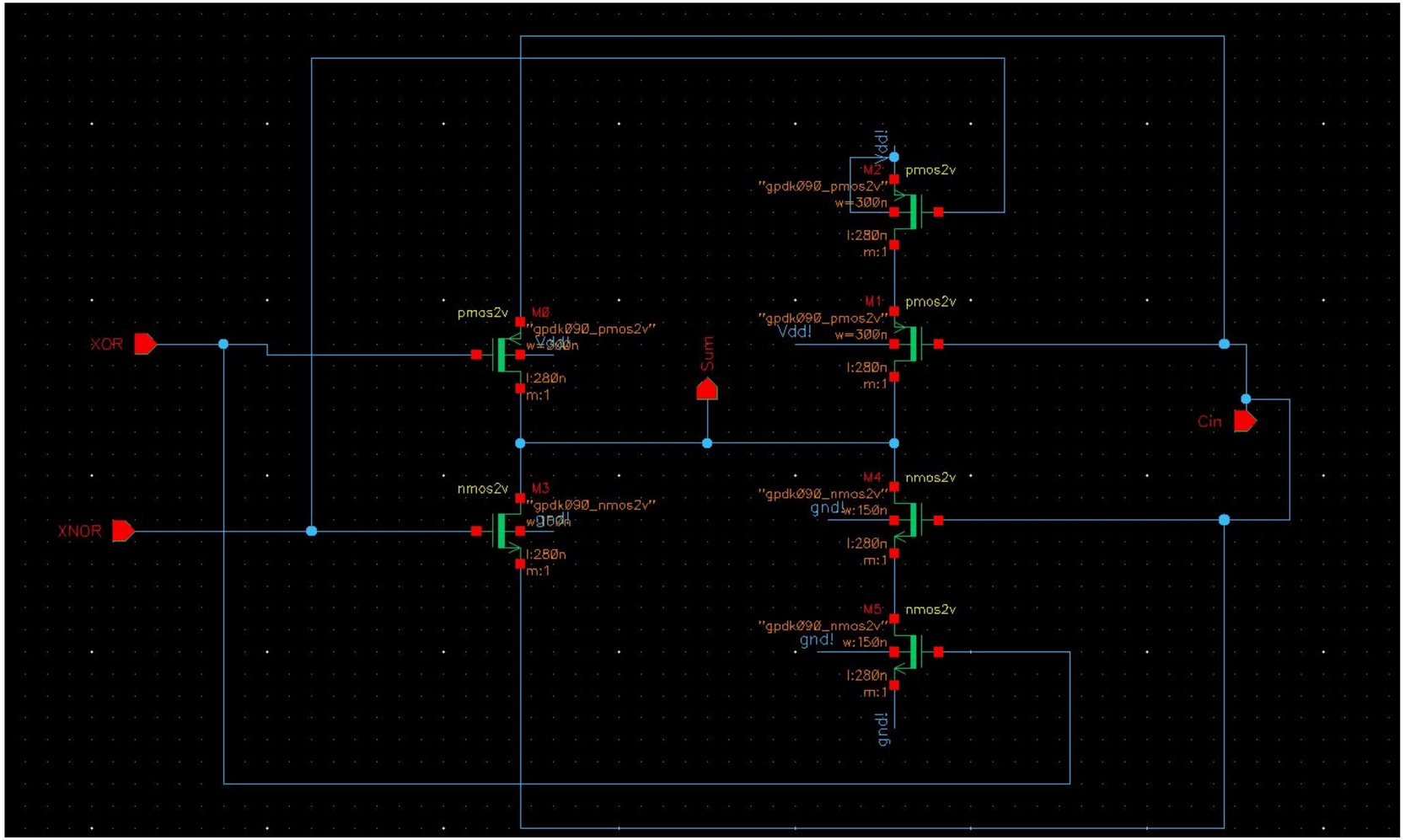


FA - 3

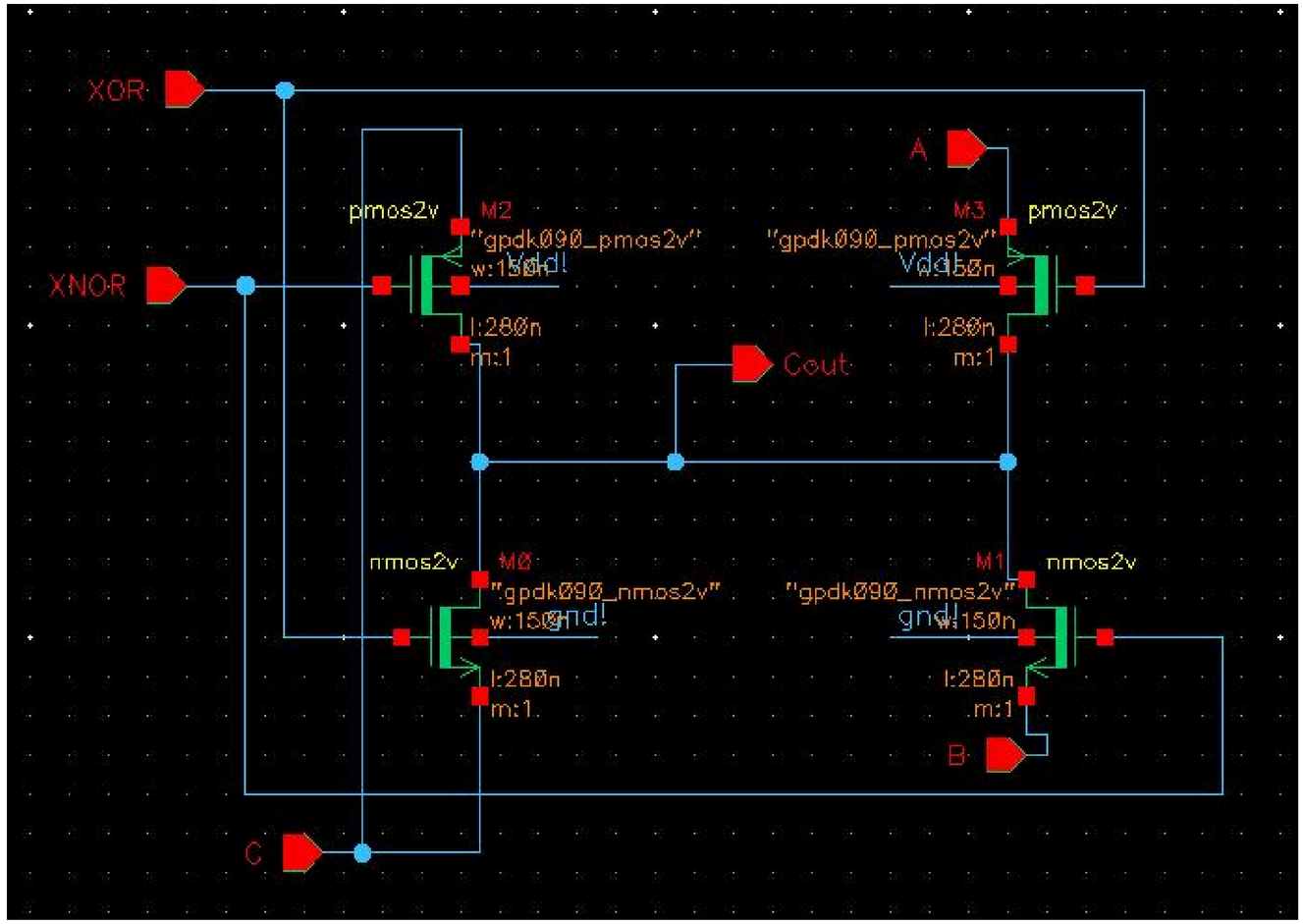


FA - 4

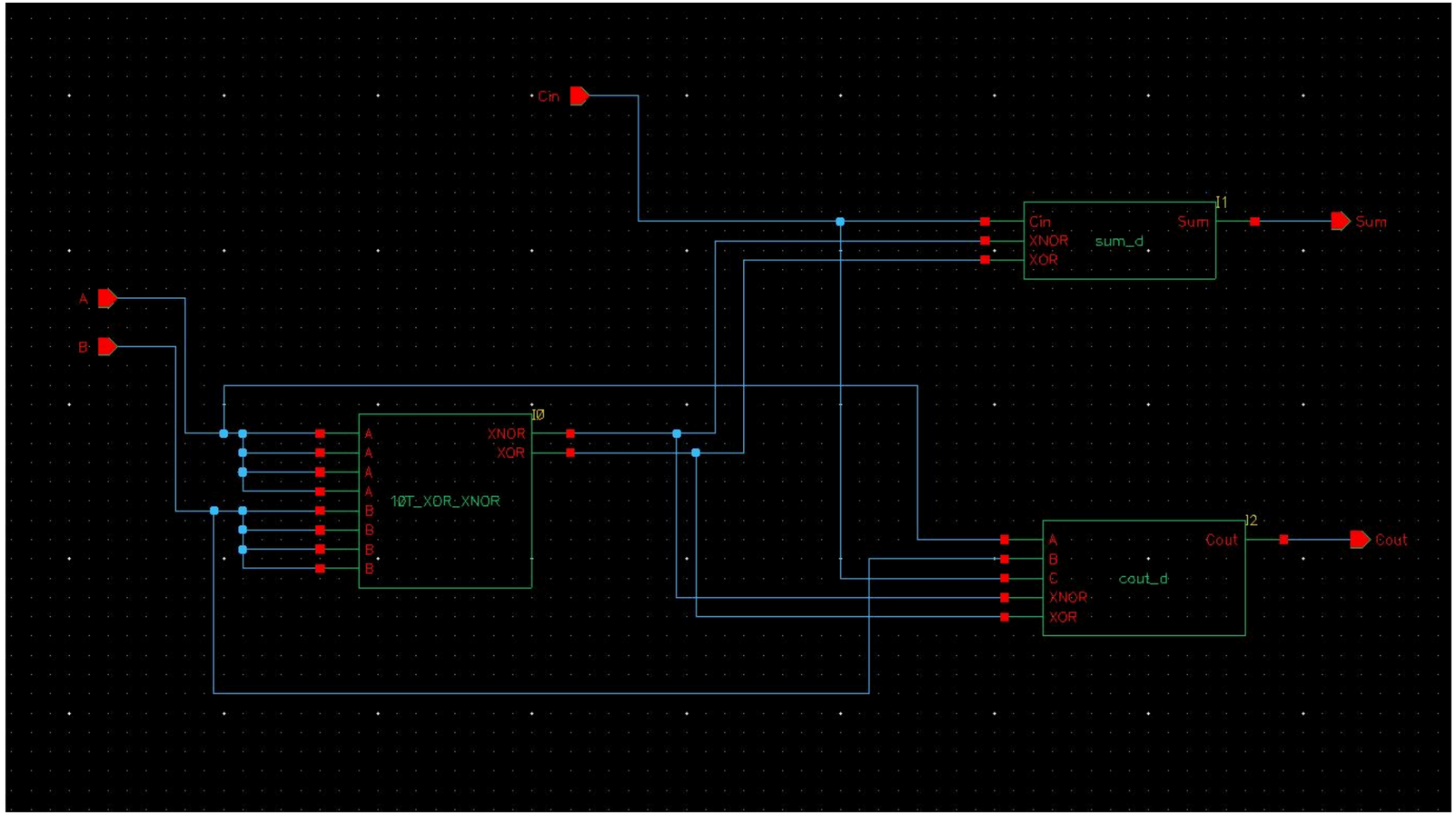
Full Adder-4 design : Sum Module



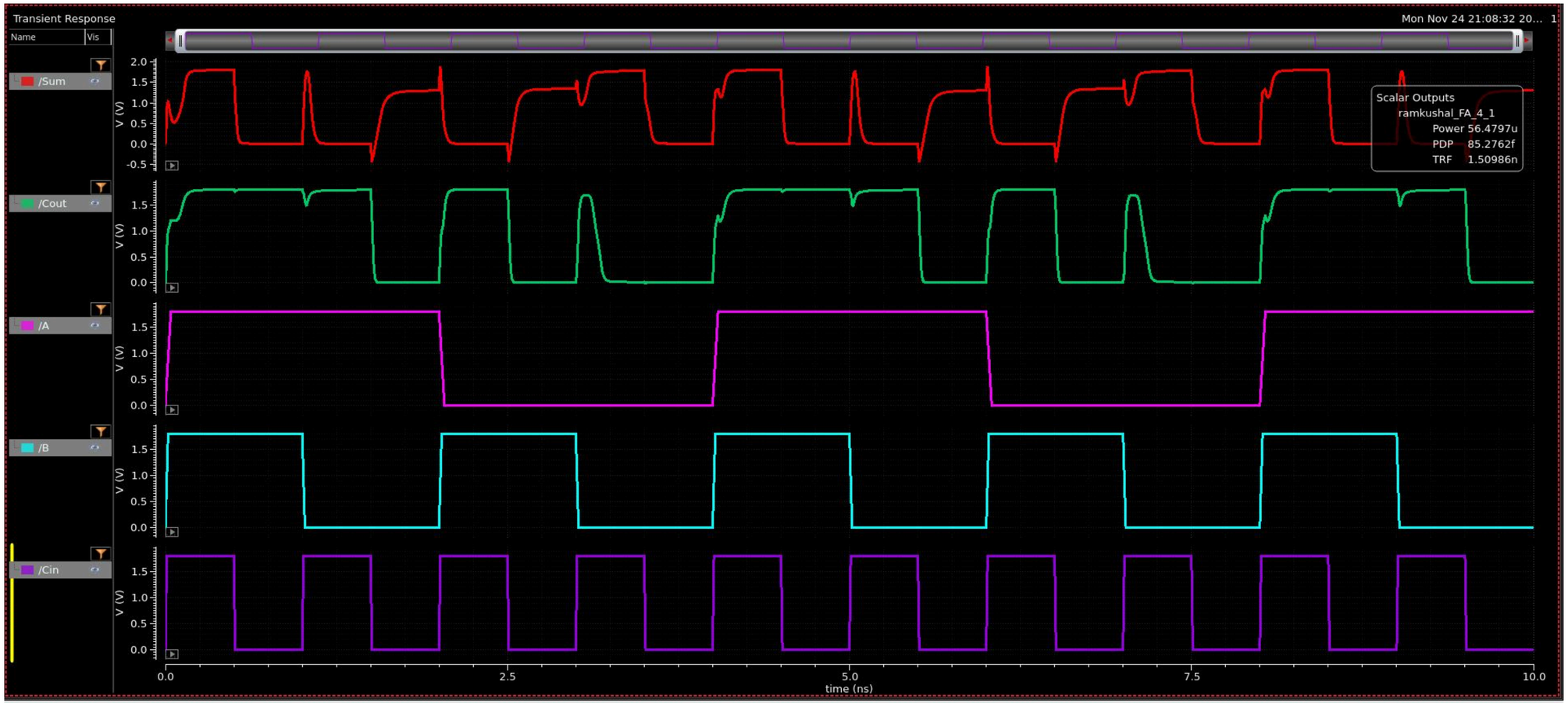
Full Adder-4 design : Cout Module



Full Adder-4 design : Integrating the XOR-XNOR cell and the Sum,Cout modules



Full Adder-4 Output Waveforms



Power Delay Product analysis of adders (NN)

Full adder circuits	Number of Transistors	Delay (ns)	Power (µW)	PDP (f)
FA Design-1	20	1.509	70.046	105.729
FA Design-2	26	1.590	69.522	110.523
FA Design-3	26	1.629	74.642	121.584
FA Design-4	20	1.510	56.480	85.276

A supply voltage(Vdd) of 1.8V was used for the analysis

Power Delay Product analysis of adders (SS)

Full adder circuits	Number of Transistors	Delay (ns)	Power (µW)	PDP (f)
FA Design-1	20	1.515	63.736	96.567
FA Design-2	26	1.676	67.904	113.779
FA Design-3	26	1.737	72.630	126.15
FA Design-4	20	1.515	53.416	80.916

A supply voltage(Vdd) of 1.8V was used for the analysis

Power Delay Product analysis of adders (SF)

Full adder circuits	Number of Transistors	Delay (ns)	Power (µW)	PDP (f)
FA Design-1	20	1.510	71.738	108.354
FA Design-2	26	1.589	70.851	112.581
FA Design-3	26	1.639	76.457	125.282
FA Design-4	20	1.511	60.645	91.662

A supply voltage(Vdd) of 1.8V was used for the analysis

Power Delay Product analysis of adders (FS)

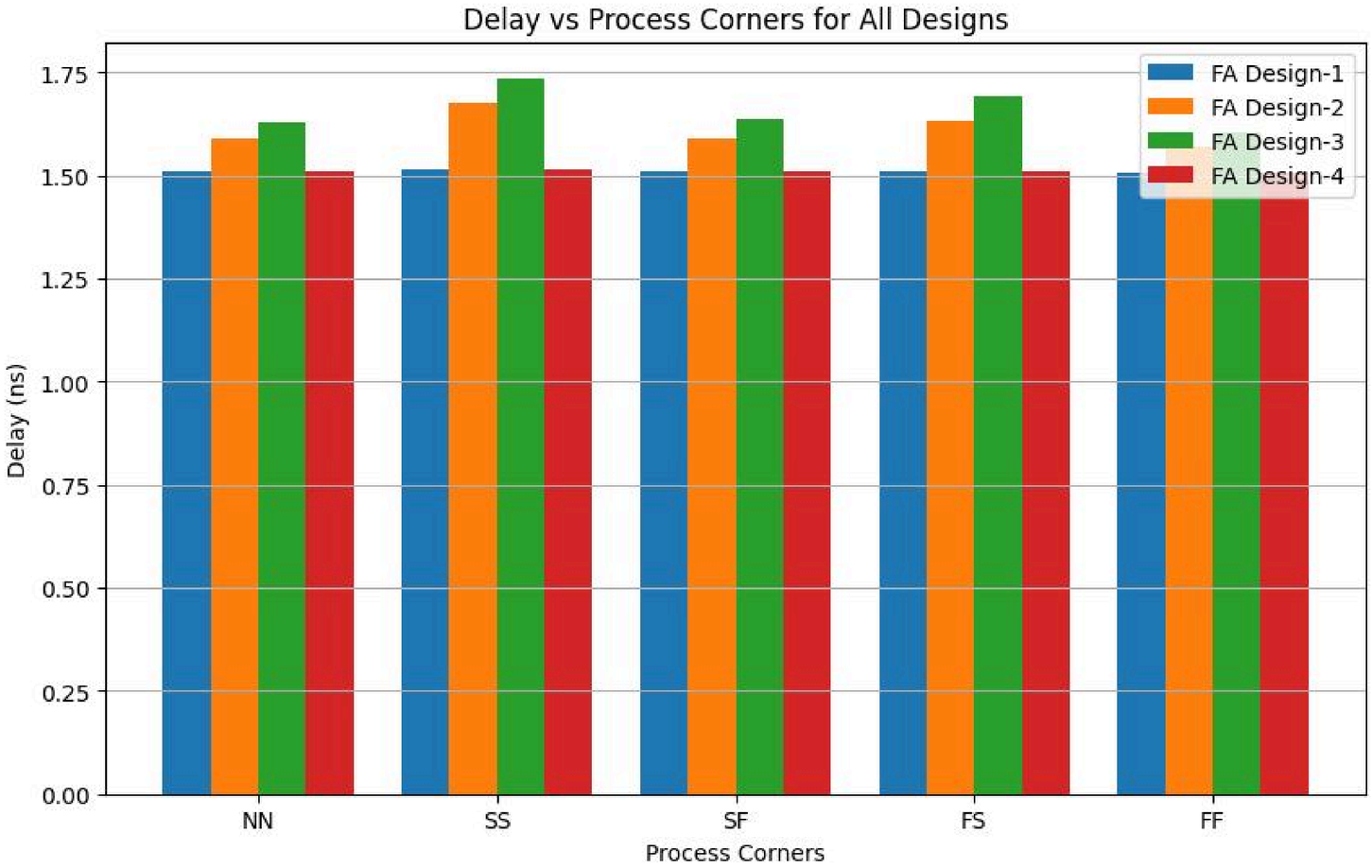
Full adder circuits	Number of Transistors	Delay (ns)	Power (µW)	PDP (f)
FA Design-1	20	1.510	65.301	98.601
FA Design-2	26	1.634	69.601	113.755
FA Design-3	26	1.694	74.231	125.719
FA Design-4	20	1.510	52.62	79.455

A supply voltage(Vdd) of 1.8V was used for the analysis

Power Delay Product analysis of adders (FF)

Full adder circuits	Number of Transistors	Delay (ns)	Power (µW)	PDP (f)
FA Design-1	20	1.507	75.314	113.534
FA Design-2	26	1.572	72.517	113.998
FA Design-3	26	1.605	78.011	125.239
FA Design-4	20	1.508	60.731	91.585

A supply voltage(Vdd) of 1.8V was used for the analysis



A supply voltage(Vdd) of 1.8V was used for the analysis

Conclusion

- Using the proposed XNOR-XOR circuit four new full adder cells based on hybrid logic design styles were proposed.
- The performance of the proposed circuit and FA cells were tested by simulating them in Cadence virtuoso using GPDK 90nm CMOS technology.
- The proposed 10-T XNOR-XOR circuit eliminates external inverters, reducing PDP compared to existing designs.
- Proposed FA-4 design achieves the lowest PDP amongst all the tested architectures.
- The proposed FA designs, due to its optimal parameters are suitable for cascaded designs.

Thank-You!