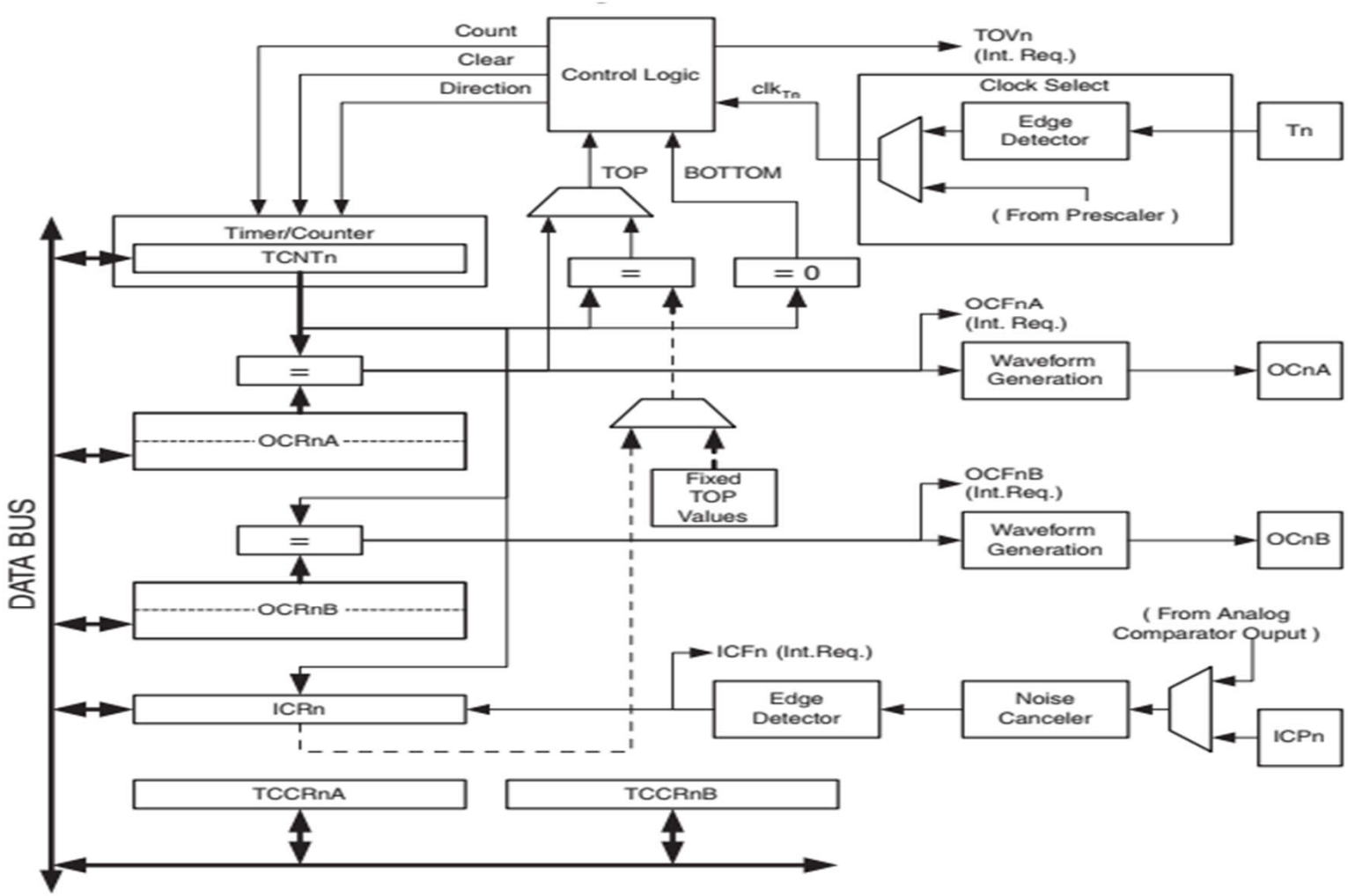
16 bit Timer/Counter1

- The 16-bit Timer/Counter unit allows accurate program execution timing (event management), wave generation, and signal timing measurement .
- **Main Features:**
  - **True 16-bit Design (that is, allows 16-bit PWM)**
    - **Two Independent Output Compare Units**
    - **Double Buffered Output Compare Registers**
    - **One Input Capture Unit**
    - **Input Capture Noise Canceler**
    - **Clear Timer on Compare Match (Auto Reload)**
    - **Glitch-free, Phase Correct Pulse Width Modulator (PWM)**
    - **Variable PWM Period**
    - **Frequency Generator**
    - **External Event Counter**
    - **Four Independent Interrupt Sources (TOV1, OCF1A, OCF1B, and ICF1)**

16-bit Timer/Counter1 Block diagram



Definition of terms used in Block Diagram

TCNT1	Timer/Counter1 (16 bit Register)
OCR1A/B	Output compare register (16 bit Registers)
ICR1	Input Capture Register (16-bit Register)
TCCR1A/B	Timer/ Counter Control Register (8-bit Register)

Block Diagram description of 16 bit Timer/Counter1

- Can be clocked internally, via the prescaler, or by an external clock source on the T1 pin.

- The Clock Select logic block controls which clock source and edge the Timer/Counter uses to increment (or decrement) its value.

- The Timer/Counter is inactive when no clock source is selected. The output from the clock select logic is referred to as the timer clock(clkT1).

Continued …

- The double buffered Output Compare Registers (OCR1A/B) are compared with the Timer/Counter value at all time.
- The result of the compare can be used by the waveform generator to generate a PWM or variable frequency output on the Output Compare Pin (OC1A/B).
- The Compare Match event will also set the Compare Match Flag (OCF1A/B) which can be used to generate an Output Compare interrupt request.

Continued …

- The Input Capture Register can capture the Timer/Counter value at a given external (edge triggered) event on either the Input Capture Pin (ICP1) or on the Analog Comparator pins .

- The Input Capture unit includes a digital filtering unit (Noise Canceler) for reducing the chance of capturing noise spikes.

Continued …

- **Terms used in 16-bit Timer/Counter1:**

BOTTOM	The counter reaches the BOTTOM when it becomes 0x0000
MAX	The counter reaches its MAXimum when it becomes 0xFFFF (decimal 65535)
TOP	The counter reaches the TOP when it becomes equal to the highest value in the count sequence
	The TOP value can be assigned to be one of the fixed values: i) 0x00FF (decimal equivalent 255) ii) 0x01FF (decimal equivalent 511) iii) 0x03FF (decimal equivalent 1023) iv) the value stored in the OCR1A or ICR1 Register. The assignment is dependent of the mode of operation.

Continued …

- The TOP value, or maximum Timer/Counter value, can in some modes of operation be defined by either the OCR1A Register, the ICR1 Register, or by a set of fixed values.
- When using OCR1A as TOP value in a PWM mode, the OCR1A Register can not be used for generating a PWM output.

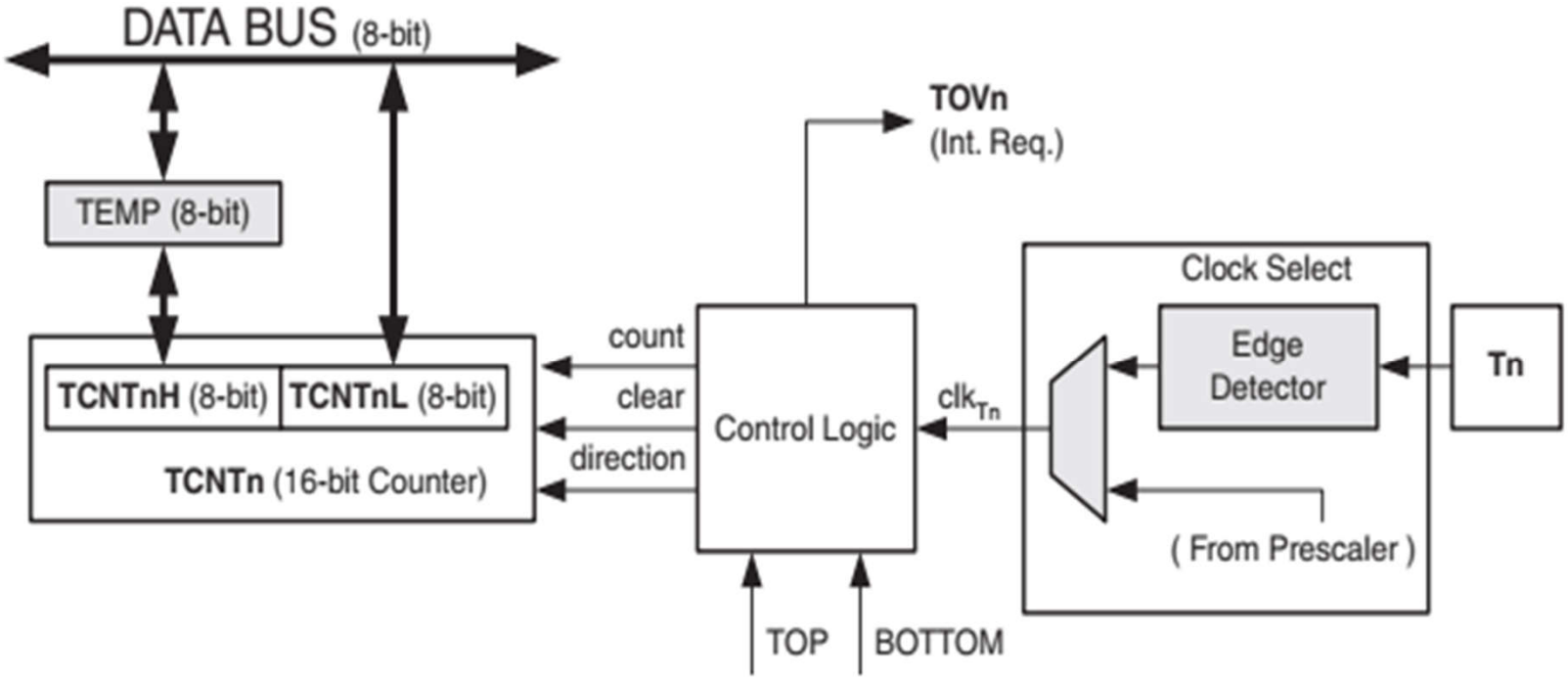
- If a fixed TOP value is required, the ICR1 Register can be used as an alternative, freeing the OCR1A to be used as PWM output.

Timer/ counter1 Clock Sources

- The Timer/Counter can be clocked by an internal or an external clock source. The clock source is selected by the clock select logic which is controlled by the *clock select* (CS1,2:0) bits located in the *Timer/Counter Control Register B* (TCCR1B)

Counter Unit Block diagram

- 16-bit Timer/Counter is the programmable 16-bit bi-directional counter unit



Counter Unit Signal Description

Signal	Description
Count	Increment or decrement TCNT1 by 1
Direction	Select between increment and decrement
clear	Clear TCNT1 (set all bits to zero)
clkT1	Timer/Counter clock
TOP	Signalize that TCNT1 has reached maximum value
BOTTOM	Signalize that TCNT1 has reached minimum value (zero)

Working of TCNT1 (READ/WRITE) value

- The 16-bit counter is mapped into two 8-bit I/O memory locations: *counter high* (TCNT1H) containing the upper eight bits of the counter, and *Counter Low* (TCNT1L) containing the lower eight bits.

- The TCNT1H Register can only be indirectly accessed by the CPU.

- When the CPU does an access to the TCNT1H I/O location, the CPU accesses the High byte temporary register (TEMP).

Continued…

- The temporary register is updated with the TCNT1H value when the TCNT1L is read, and TCNT1H is updated with the temporary register value when TCNT1L is written.

- This allows the CPU to read or write the entire 16-bit counter value within one clock cycle via the 8-bit data bus.

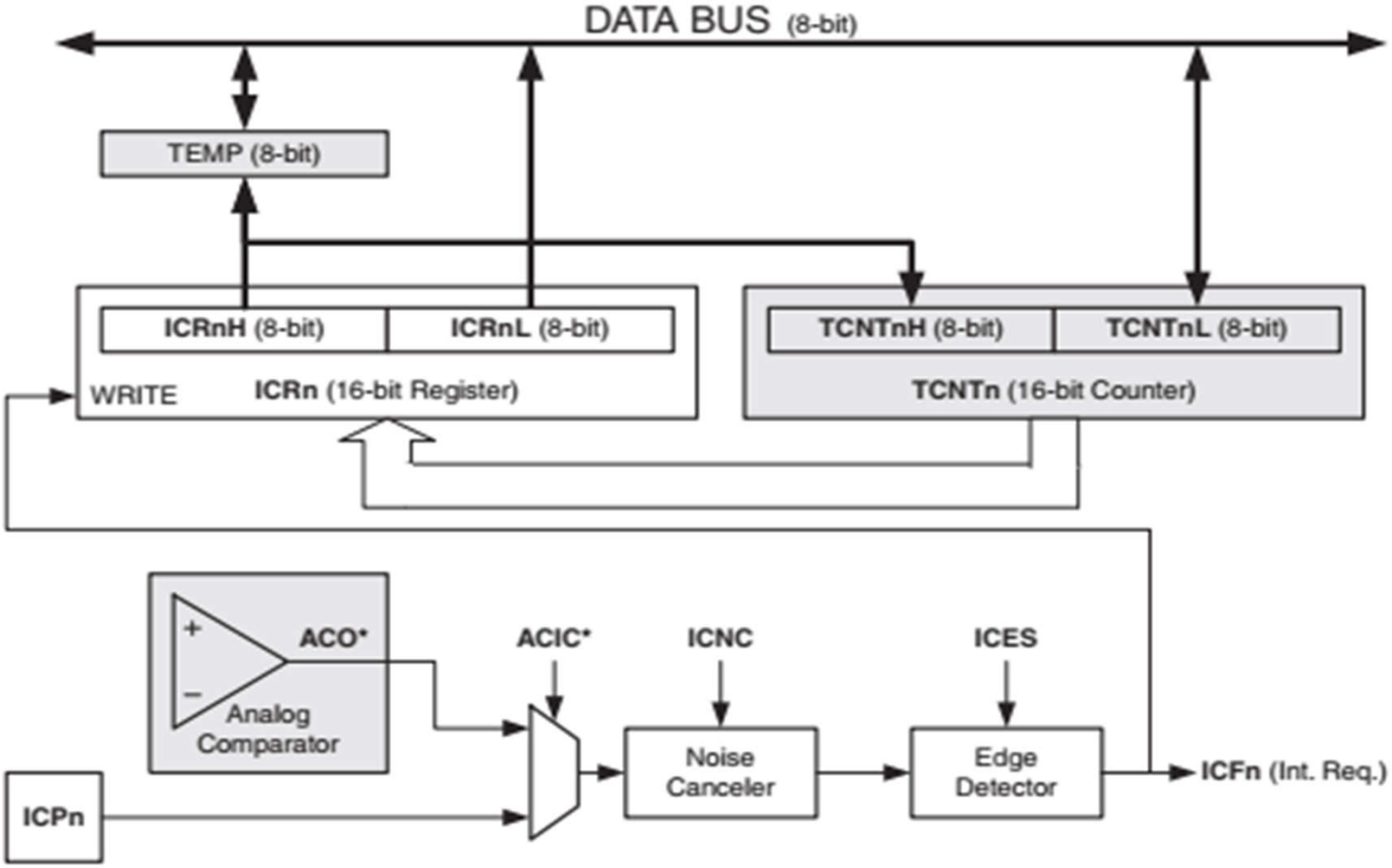
Continued…

- The counting sequence is determined by the setting of the Waveform Generation mode bits WGM1(3:0) located in the Timer/Counter Control Registers A and B (TCCR1A and TCCR1B)

- The *Timer/Counter Overflow* (TOV1) flag is set according to the mode of operation selected by the WGM1(3:0) bits.

- TOV1 can be used for generating a CPU interrupt.

Input Capture unit block diagram



ICP working

- Input Capture unit can capture external events through (ICP1 pin) and give them a time-stamp indicating time of occurrence.

- The time-stamps can then be used to calculate frequency, duty-cycle, and other features of the signal applied.

- The small “n” in register and bit names indicates the Timer/Counter number.

ICP working (continued…)

- When a change of the logic level (an event) occurs on the Input Capture Pin (ICP1)/on the Analog Comparator Output (ACO), and this change confirms to the setting of the edge detector, a capture will be triggered.
- When a capture is triggered, the 16-bit value of the counter (TCNT1) is written to the *Input Capture Register* (ICR1).
- The *Input Capture Flag* (ICF1) is set at the same system clock as the TCNT1 value is copied into ICR1 Register.
- If enabled (TICIE1 =1), the Input Capture Flag generates an Input Capture interrupt.

ICP working (continued…)

- The ICF1 Flag is automatically cleared when the interrupt is executed. Alternatively the ICF1 Flag can be cleared by software by writing a logical one to its I/O bit location.

- Reading the 16-bit value in the *Input Capture Register* (ICR1) is done by first reading the Low byte (ICR1L) and then the High byte (ICR1H).

- When the Low byte is read the High byte is copied into the High byte temporary register (TEMP). When the CPU reads the ICR1H I/O location it will access the TEMP Register.

ICP working (continued…)

- The ICR1 Register can only be written when using a Waveform Generation mode that utilizes the ICR1 Register for defining the counter's TOP value.

- *Waveform Generation mode* WGM1,(3:0) bits must be set before the TOP value can be written to the ICR1 Register.

- When writing the ICR1 Register the High byte must be written to the ICR1H I/O location before the Low byte is written to ICR1L.

- **Input capture pin source:**

  i) Timer/counter1

  ii) Analog comparator output (ACO)

- **The Analog Comparator selection:**

  Set Analog Comparator Input Capture (ACIC) bit = '1' in the *Analog Comparator Control and Status Register* (ACSR).

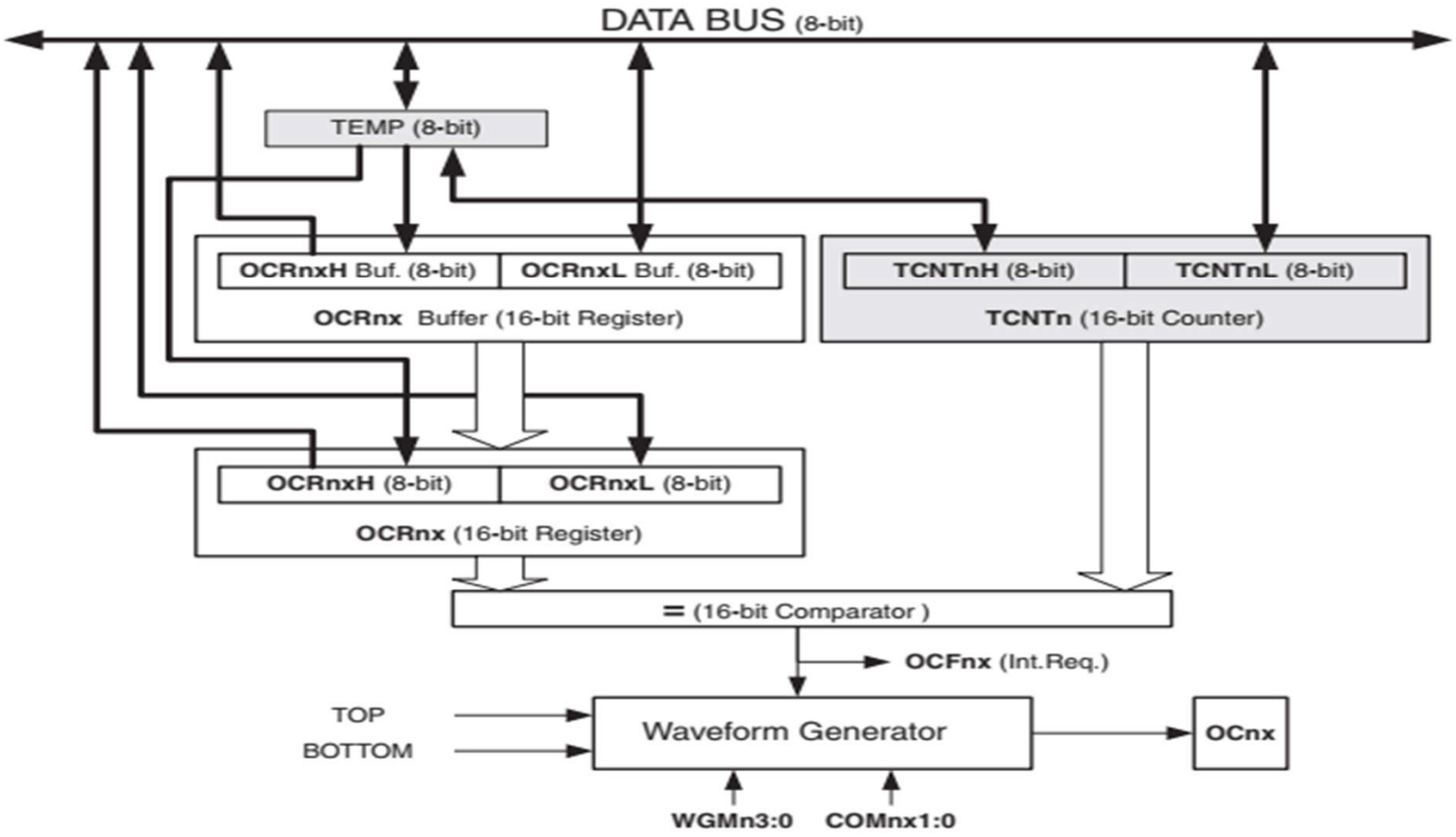
- The Input Capture Flag must therefore be cleared after the change.

- **Noise canceler:**

✓ The noise canceler improves noise immunity by using a simple digital filtering scheme. The noise canceler input is monitored over four samples, and all four must be equal for changing the output that in turn is used by the edge detector.

✓ The noise canceler is enabled by setting the *Input Capture Noise Canceler* (ICNC1) bit in *Timer/Counter Control Register B* (TCCR1B).

Output Compare Unit



Working of output compare unit

- The 16-bit comparator continuously compares TCNT1 with the *Output Compare Register* (OCR1x).
- If TCNT equals OCR1x the comparator signals a match. A match will set the *Output Compare Flag* (OCF1x) at the next timer clock cycle.
- If enabled (OCIE1x = 1), the Output Compare Flag generates an Output Compare interrupt. The OCF1x Flag is automatically cleared when the interrupt is executed.
- The waveform generator uses the match signal to generate an output according to operating mode set by the *Waveform Generation mode* WGM1,(3:0) bits and *Compare Output mode* (COM1x1:0) bits.

Modes of Operation

- The mode of operation is defined by the combination of the *Waveform Generation mode* (WGM1,3:0) and *Compare Output mode* (COM1x1:0) bits.
- The Compare Output mode bits do not affect the counting sequence, while the Waveform Generation mode bits do.
- The COM1x1:0 bits control whether the PWM output generated should be inverted or not (inverted or non-inverted PWM).
- For non-PWM modes the COM1x1:0 bits control whether the output should be set, cleared or toggle at a Compare Match.

Modes of Operation(continued..)

- **Normal mode:**
  - *Normal* mode (WGM1,3:0 = 0).
  - Counting direction is always up (incrementing), and no counter clear is performed.
  - Counter overruns when it passes its maximum 16-bit value (MAX = 0xFFFF) and then restarts from the BOTTOM (0x0000).
  - Timer/Counter Overflow Flag (TOV1) will be set in the same timer clock cycle as the TCNT1 becomes zero.
  - combined with the timer overflow interrupt that automatically clears the TOV1 Flag, the timer resolution can be increased by software.

Modes of Operation(continued..)

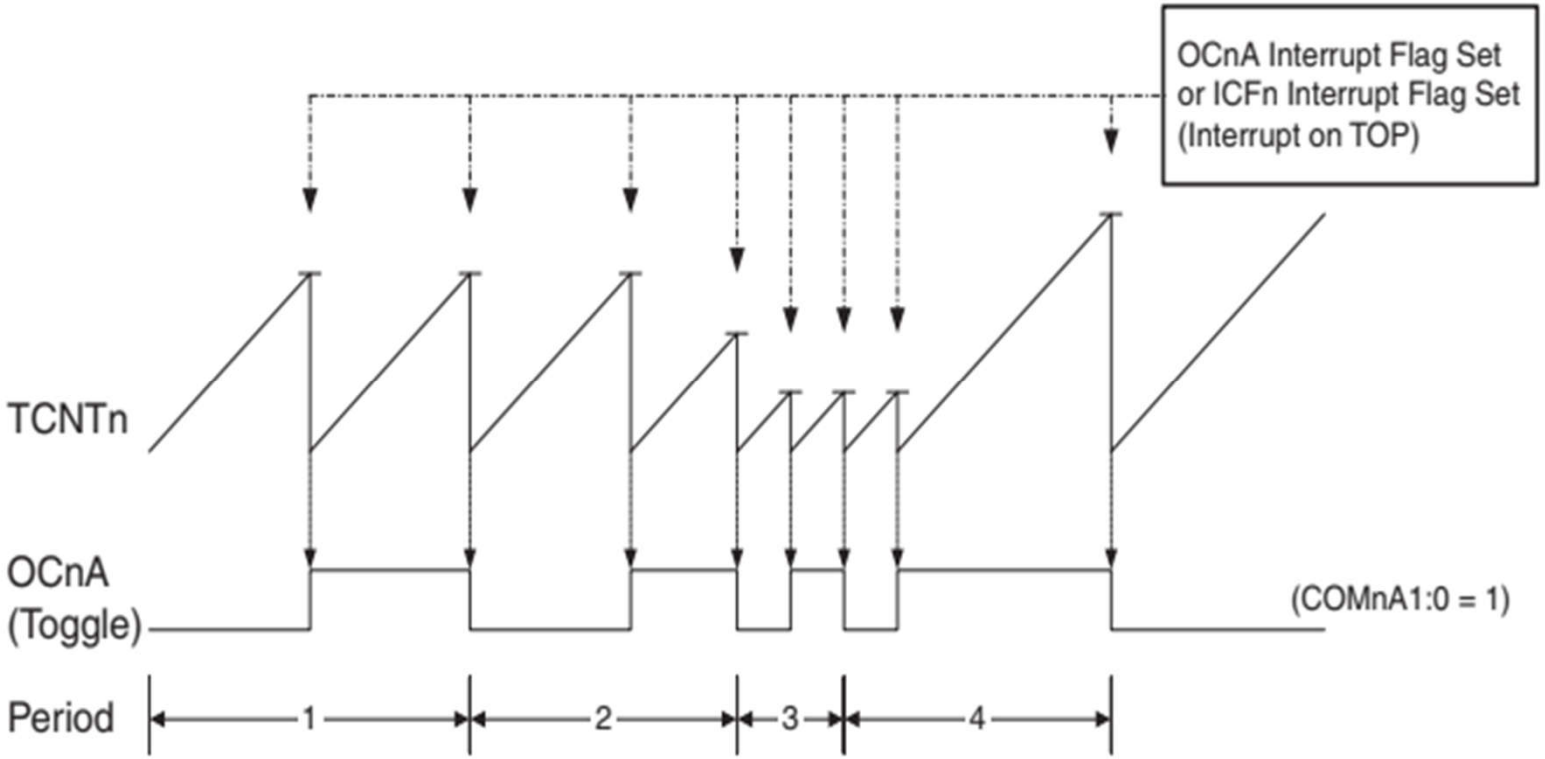
- Using the Output Compare to generate waveforms in Normal mode is not recommended, since this will occupy too much of the CPU time.

Modes of Operation(continued..)

- **Clear timer on Compare Match (CTC) Mode:**

- **CTC mode (WGM1,3:0 = 4 or 12)**
- **OCR1A or ICR1 Register are used to manipulate the counter resolution.**
- **counter is cleared to zero when the counter value (TCNT1) matches either the OCR1A (WGM1,3:0 = 4) or the ICR1 (WGM1,3:0 =12).**
- **This mode allows greater control of the Compare Match output frequency. It also simplifies the operation of counting external events.**

Modes of Operation (continued..)



CTC mode , Timing diagram

Modes of Operation(continued..)

- The counter value (TCNT1) increases until a Compare Match occurs with either OCR1A or ICR1, and then counter (TCNT1) is cleared.
- For generating a waveform output in CTC mode, the OC1A output can be set to toggle its logical level on each Compare Match by setting the Compare Output mode bits to toggle mode (COM1A1:0 = 1).