mm:30 BE(ECE) VLSI Design Time: 1½ hr.

Section-2 Minor-I

Q1. Calculate the threshold voltage of MOSFET with $\phi_{GC} = -0.8V$, $t_{ox} = 200\text{Å}$, $N_A = 1.5 \times 10^{16} cm^{-3}$, $Q_{ox} = 3.2 \times 10^{-9} C/cm^2$, $T = 300K$, $\varepsilon_{ox} = 3.97\varepsilon_0$, $\varepsilon_{Si} = 11.7\varepsilon_0$. ϕ_{GC} or ϕ_{ms} is the work function difference between gate & channel region. (6)

Q2. What are MOSFET level 1 SPICE parameters? Discuss effect of variation of these parameters on MOSFET drain characteristics (5)

Q3. Which short channel Effect is the work effect? What is remedy to overcome it? (3)

Q4. Draw various inverter configurations. List advantages & disadvantages of each type. Which configuration has best Noise Margin? (4)

Q5. Draw the CMOS and nmos logic circuit for following

a) $\overline{A + B(C+D)}$

b) $(A + \bar{B})C + \bar{A}D$ (6)

Q6. The CMOS fabrication parameters are $\mu_n C_{ox} = 120\mu A/V^2$, $\mu_p C_{ox} = 60\mu A/V^2$, $L = 0.6\mu m$ (for both nmos & pmos), $V_{thn} = 0.8V$, $V_{thp} = -1V$, Calculate the W of transistors for $\tau_{PHL} \leq 0.2ns$ & $\tau_{PLH} \leq 0.15ns$. Use average current method. (6)