VLSI Design Flow: RTL To GDS (NPTEL Course)

Tutorial 8

Objective: To understand how delay calculation and Static Timing Analysis (STA) are impacted by Technology Library and Constraints with the help of open-source tool OpenSTA

Requirements:

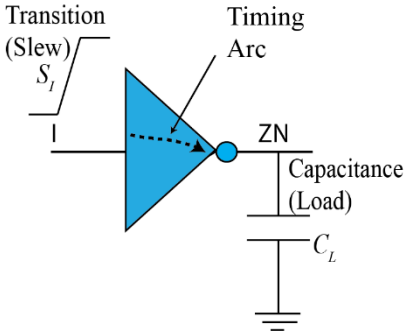
- **OpenSTA**: The installation and how to run OpenSTA is described in Tutorial 7. Please refer to it if you do not have OpenSTA installed on your machine.
- **Files:**
  - Design file: test.v
  - OpenSTA script file: test.tcl
  - SDC file: test.sdc
  - Technology library: toy.lib

  All the above files are available on the NPTEL website as study material for Week 8

Concepts:

From Lecture 21 (Library):

Non-linear Delay Model (NLDM)



NLDM

$T(i,j)$	$C_{L,1}$	$C_{L,2}$			$C_{L,N}$
$S_{I,1}$					
$S_{I,2}$					
$S_{I,M}$					

From Lecture 25, 26 (Constraints):

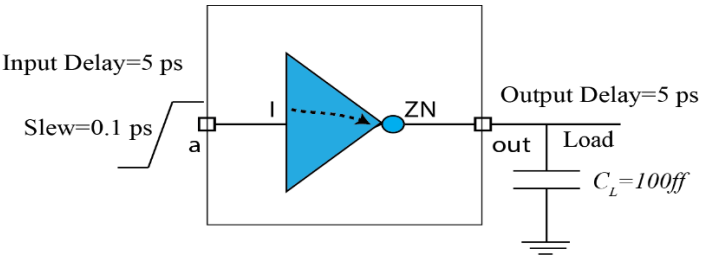
- create_clock: to create a clock reference for timing analysis
- set_input_delay: to specify the delay in input before reaching the given circuit
- set_output_delay: to model change in required time due to external circuit elements
- set_input_transition: to specify transition/slew at the input port
- set_load: to specify load capacitance at the output port
- set_clock_uncertainty: to add pessimism to timing analysis

Experiment: Run OpenSTA and study the impact of library, delay, and constraints on STA

From toy.lib:

	C=0.1ff	C=100ff
Tr=0.1ps	1	80
Tr=100ps	4	200

From small.v and small.sdc:



Expected Delay: 80 ps