Week 1 Embedded system design

1. An embedded system is always programmable.
    a. True
    b. False

Ans – b. False

Explanation – Apart from Embedded systems being programmable an Embedded system can also be hardwired.

2. There can be multiple embedded systems present in a larger system.
    a. True
    b. False

Ans – a. True

Explanation –Take for example an car (larger system) can have multiple embedded systems present in it for example - Antilock Braking System(ABS), Engine Control Unit (ECU), Traction Control System etc.

3. An Embedded System differs from General Purpose system in which of the following factor(s)
    I. Lower Power Consumption
    II. Lower Cost
    III. Portable
    IV. Multipurpose

a) I
b) I,III
c) III,IV
d) I,II,III
e) I,II,III,IV

Ans –d)I,II,III

Explanation- An Embedded system is used for single purpose whereas a General Purpose System is used for General purpose. Embedded system is tightly constrained in terms of low cost, low power consumption, portable and sometimes it must be realtime.

4. Boiler of a Thermal Power Plant is equipped with embedded systems which control and maintain the temperature and pressure inside the boiler. The Embedded systems must be
    a. Soft realtime systems
    b. Hard realtime systems

Ans – b. Hard realtime systems

Explanation – Overshooting deadline to complete a task of controlling temperature and pressure can lead to major catastrophe, that's why stringent time constraints are present and embedded systems in the above case must be Hard Realtime embedded system

5. The design activity where operations are mapped to hardware or software is
    a. Compilation
    b. Scheduling
    c. Processor Design
    d. Hardware-Software Co-Design
    e. None of the above

Ans – d. Hardware-Software Co-Design

Explanation – The hardware/software Co-Design is the activity which is in charge of mapping operations to the software or to the hardware

6.

If a component is implemented in software then

a. It will be faster
b. It will be Slower
c. It will be Costly
d. None of the above

Ans – b. It will be Slower

Explanation – Designing any component in software leads to the system to be slower as the system has to process it separately by allocating separate CPU time but on the other hand it leads to the system to be more flexible as it would able to perform more functions on the programmer's side.

7.

If a component is implemented in hardware then

a. It will be flexible
b. It will be faster
c. It will be cheaper
d. None of the above

Ans – b. It will be faster

Explanation – Designing a specific component in hardware helps in making that component fast but leads to more time consumed in designing the hardware parts and hence the increase in cost related to it, and makes the system less flexible too on programmer's side.

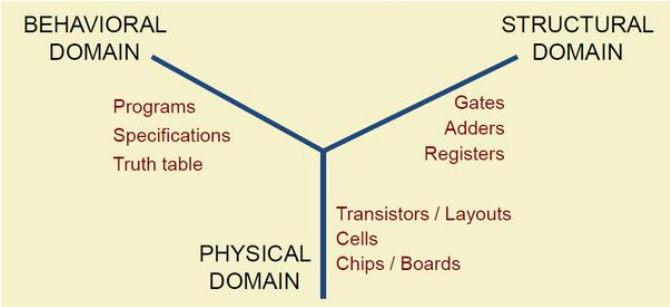
8.

Placement and Routing task comes under which design step

a. Structural Design
b. Geometrical Design
c. Behavioral Design
d. None of the above

Ans – b. Geometrical Design

Hint – Gajski's Ychart



Explanation – Placement and Routing task is a part of Geometrical design step as we need to place and route the structure of circuit obtained in structural design step.

9.

There is no distinction in between data memory and program memory in Harvard Architecture

a. True
b. False

Ans – b. False

Explanation - There is no distinction in between data memory and program memory in Von-Neumann Architecture but in Harvard architecture they are separate.

10.

A Timer is set to zero and at every clock pulse it counts up and at any point of time we can find out the time elapsed.

a. True
b. False

Ans – b. False

Explanation - A Counter is set to zero and at every clock pulse it counts up and at any point of time we can find out the time elapsed.

1. The possible ways to optimize a single-purpose processor is:
   a. To optimize the original program of the processor.
   b. To optimize FSMD by merging the stages in FSMD.
   c. Make sure for parallel execution of similar operations.
   d. All of the above.
   e. Option a and b both.

   Ans. e (Option a and b both)

   Justification: One can optimize single purpose processor by optimizing the original program, optimizing the FSMD by eliminating or merging the states. But parallel execution of similar operations is not possible because it will need more hardware support which is not optimal.

2. Optimization of data path can be done with:
   a. By merging the control bus and data bus.
   b. Reducing one to one mapping and effectively using the hardware.
   c. By making sure the similar type of tasks is executed parallelly in same time slot.
   d. Opting to use high level processors.

   Ans. b (Reducing one to one mapping and effectively using the hardware.)

   Justification: One to one mapping is not necessary. If similar operations take place in different stages, they can share same functional unit.

3. States can only be merged if they are equivalent states. Equivalent states are:
   a. States that perform similar type of operation.
   b. Time needed to execute the states are same so they can be merged together.
   c. For all possible input combinations states generate the same output and transitions to the same next state.
   d. None of the above.

   Ans. C (For all possible input combinations states generate the same output and transitions to the same next state.)

   Justification: States can only be merged if, for all possible input combinations states generate the same output and transitions to the same next state. These states are called equivalent states.

4. State the false statement.
   a. The embedded systems using GPPS takes relatively less time to market.
   b. The embedded system using single purpose processors are more versatile.
   c. The embedded system using FPGA are the fastest.
   d. The embedded system using ASIP are faster than embedded system using general purpose processor.

   Ans. b (The embedded system using single purpose processors are more versatile.)

   Justification: The embedded systems using general purpose processors are more versatile. Single purpose processors are designed considering a single type of tasks.

5. Field programmable gate arrays (FPGA) consists of:
   a. Configurable logic blocks.
   b. Single purpose processor.
   c. Programmable logic devices.
   d. Application specific instruction set processors.

   Ans. a (Configurable logic blocks.)

   Justification: FPGAs consists of an array of Configurable logic blocks (CLB).

6. State which is true among the statements about antifuse connection.
   a. The resistance is very high for antifuse.
   b. A capacitor is used for antifuse.
   c. It provides more flexibility than SRAM connection.
   d. It is permanent and hence can not be used further.

   Ans. d (It is permanent and hence can not be used further)

Justification: Antifuse connections are permanent and hence can not be further used. Antifuse connections are permanent and once it is done, it can not be redone.

7. Combinational logic can be implemented by
   a. Encoder and a look up table.
   b. Decoder and a look up table.
   c. Multiplexer.
   d. All of the above.
   e. b and c both.

   Ans. e (b and c both)

   Justification: Combinational logic can be implemented either by using a multiplexer or a decoder and a look-up table.

8. In SRAM connection:
   a. A pass transistor is used.
   b. An insulator is used that becomes conductor after a certain voltage.
   c. A capacitor is used that allows AC current to pass.
   d. An inductor is used.

   Ans. a (A pass transistor is used).

   Justification: In SRAM a pass transistor is used. It can be programmed and when the value is 1 it conducts and creates the connection and when value is 0 the connection is off.

9. The D flipflop is used in configurable logic block because
   a. To store all the results of the CLB.
   b. To use the previous state result from look-up table.
   c. It works as encoder.
   d. To halt the function of CLB.

   Ans. b (To use the previous state result from look-up table)

   Justification: In configurable logic block a d flipflop is used so that the value of look-up table can be used in next state so that a delay can be induced.

10. For a 2*2 control logic block based system, the number of switch box required is:
    a. 4
    b. 5
    c. 6
    d. 7

    Ans. b (5)

    Justification: For a 2*2 CLB based system, 5 switch box is required.

Week 3 Embedded system design

1. Behavioral Description of a system include(s)
    a. Operations
    b. Functions
    c. Processes
    d. None of the above

Ans - a. Operations, b. Functions, c. Processes
Explanation - Behavioral description of a system includes Operations, Function, Processes etc that are required to convert input to output.

2. A system designed in VHDL consists of modules
    a. True
    b. False

Ans – b. False
Explanation – A system designed in verilog consists of module where as a system designed in VHDL is composed of entities each of which can have multiple architecture and a configuration chooses what architecture is used for a given instance of an entity.

3. Given 2 statements
    i. Functional Design is also Known as Back-End Design
    ii. Physical Design is also known as Front-End Design

    a. Both i. & ii. are False
    b. Both i. & ii. are True
    c. i. is True & ii. is False
    d. i. is False & ii. is True

Ans - a. Both i & ii are false
Explanation –
Functional Design is also Known as Front-End Design whereas Physical Design is also known as Back-End Design

4. Single line comments in verilog start with #
    a. True
    b. False

Ans – b. False
Explanation – Single line comments in verilog starts with //

5. We can design a memory element using Dataflow model
    a. True
    b. False

Ans – b. False
Explanation – We cannot design a memory element using a data flow model because in dataflow model outputs are defined in terms of input signal transformation i.e. only combinational elements can be deigned.

6. Given below a code of an module

```
module unknown(
        output a,b,c,d,
        input e,f);
            wire ne,nf;
            not inv1(nf,f);
            not inv2(ne,e);
            and A1(a,ne,nf);
            and A2(b,ne,f);
            and A3(c,e,nf);
```

and A4(d,e,f);
endmodule

the above module represents

a. Encoder
b. Decoder
c. Multiplexer
d. None of the Above

Ans – b. Decoder
Explanation- the module takes ‘e’ and ‘f’ as input and produces all 4 combinations of them.

7. Assign statement in dataflow modeling are executed parallely
   a. True
   b. False

Ans – a. True
Explanation – assign statements are concurrent in nature and thus are executed when there is an change in a variable on the right hand side of statement.

8. Parameters are compile time constants
   a. True
   b. False

Ans – b. False
Explanation – Parameters are runtime constants, are declared within a module, their scope lies within a module, can be overwritten during component instantiation and are used to make code scalable.

9.

The default value of variable is

a. X
b. 1
c. Z
d. 0

Ans – a. X
Explanation – By default variable have the value as ‘x’

10.

The default value of net is

a. X
b. 1
c. Z
d. 0

Ans – c. Z
Explanation - Net’s default value is ‘z’ i.e. high impedance

11.

Which type of device FPGA are?

a. SLD
b. SROM
c. EPROM
d. PLD

Ans – d. PLD
Explanation - Field-Programmable Gate Arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors that you find in your PC, programming an FPGA rewires the chip itself to implement your functionality rather than run a software application. Thus, FPGAs are PLD devices.

Assignment 4

MCQ:

1. The bit rate of a signal generated from an 8-bit generator is 3200 bps. Calculate the Baud rate of the signal.

A. 400 Baud/sec
B. 25600 Baud/sec
C. 200 Baud/sec
D. None of the above

Solution: Option A. 400 Baud/sec

Explanation: Using the relation, bit rate = no. of bits per signal unit * Baud rate; bit rate = 3200; no. of bits per signal unit = 8. Therefore, the Baud rate = 3200/8 = 400 Baud/sec.

2. I am building a device that takes in digital signals but restricts the input higher than a certain frequency limit. What kind of filter should I use on the device?

A. High pass filter
B. Low pass filter
C. Both A and B
D. None of the above

Solution: Option A. High pass filter

Explanation: High pass filters allow the passage of signals above a set frequency.

3. An operational amplifier has

A. Very low input impedance and infinite output impedance
B. Infinite input impedance and infinite output impedance
C. Infinite input impedance and very low output impedance
D. Very low input impedance and very low output impedance

Solution: Option C. Infinite input impedance and very low output impedance

Explanation: This is a property of operational amplifiers which makes them voltage-gain devices.

4. The number of comparators needed in a flash A/D convertor for a 3-bit conversion is

A. 3
B. 7
C. 8
D. 31

Solution: Option B. 7

Explanation: The number of convertors needed for a flash A/D converter for n-bit conversion is 2^n -1. For n=3, the number of convertors is 8-1=7.

5. Calculate the resolution(in mV) for a 4-bit A/D convertor over a voltage range of 15V.

A. 0.001
B. 1000
C. 0.1
D. None of the above

Solution: Option B. 1000

Explanation: Res(Q) for n-bit convertor = V/(2^n -1).
Putting n=4, V=15, Res(Q) = 15/((2^4 -1) = 1V = 1000mV

6. The frequency of a circuit is *f*. In order to reconstruct the original signal, the incoming signal should be

A. *=f*
B. <f/2
C. >f/2
D. =f/2

Solution: Option B. *<f/2*
Explanation: This can be observed from the Nyquist theorem.

7. Why is the power consumption of a CMOS sensor more than a CCD sensor?

A. CMOS sensors have embedded logic in them.
B. CCD sensors have a higher number of DSPs.
C. Both A and B
D. None of the above

Solution: Option A. CMOS sensors have embedded logic in them.
Explanation: We can put logic on the chip in CMOS sensors which increases the power consumption of the system. On the other hand, CCD sensors do not have logic embedded in them.

8. Which of the following properties of the Nyquist criteria are true?

A. Sampling frequency must be at least twice that of the highest frequency in the signal
B. Frequency spectrum gets divided into an infinite number of Nyquist zones each having a width of half the sampling frequency.
C. Both A and B
D. None of the above

Solution: Option C. Both A and B
Explanation: Option A is the definition of Nyquist criteria. Option B says about the Nyquist bandwidth which is equal to half the sampling frequency.

9. How does delta-sigma modulation take place in A/D convertors?

A. Iteratively
B. Recursively
C. Both A and B can be implemented.
D. None of the above

Solution: Option A. Iteratively
Explanation: Fact. Also, recursive implementation is avoided in hardware implementations.

10. Quantization is irreversible.

A. True
B. False

Solution: Option A. True

Week 5

1.

In a pulse width modulated system avg. voltage is changed by

a. Changing the analog signal into digital signal.
b. Changing the duty cycle
c. Changing the sampling rate of the signal.
d. Changing the clock rate of the signal

Ans. b (Changing the duty cycle)
Justification: In pulse width modulated system the analog signals are represented into digital signal by varying the time duration of high and low (0, 1) voltage. Changing the duty cycle the avg. voltage of the system is changed.

2.

The receiver gets informed about the serial incoming message from the transmitter by:

a. A start bit denoted by 1 bit of 0 and end bit is denoted by 2 bits of 0.
b. A start bit is denoted by 1 bit of 1 and end bit is denoted by 2 bits of 1.
c. A start bit is denoted by 1 bit of 0 and end bit is denoted by 1 bit of 1.
d. A start bit is denoted by 1 bit of 1 and end bit is denoted by 2 bits of 0.

Ans. a (A start bit denoted by 1 bit of 0 and end bit is denoted by 2 bits of 0.)
Justification: Data is transmitted from sender to receiver through a TTL line which is in high level in default state. The start bit is denoted by 1 bit of 0 and stop bit is 2 bit of 0.

3.

The value of the key pressed is parsed in Arduino by which command

a. Serial. read
b. Serial.parse
c. Serial.scan
d. Serial.parseInt

Ans. d (Serial.parseInt)
Justification: Serial.parseInt command is used to perse the value when a key press event occurs.

4.

The components of interrupt function (attachInterrupt) in Arduino are

a. Interrupt mode and function of interrupt
b. Interrupt mode, Interrupt return and Function of interrupt
c. Interrupt pin, interrupt function and interrupt mode
d. Interrupt function, reason of interrupt and interrupt mode

Ans. C (Interrupt pin, interrupt function and interrupt mode)
Justification: The interrupt function contains three components which are Interrupt pin, interrupt function and interrupt mode. Example: attachInterrupt (0, deEncode, FALLING). Here 0 is the pin number, deEncode is the function and FALLING is the mode of interrupt that means interrupt will work on falling edge.

5.

The keyword used in Arduino to execute a periodic function is:

a. Period
b. Eventperiod
c. Onperiod
d. Every

Ans. d (every)
Justification: The keyword used to execute a periodic function in Arduino is every
Example: int every (long period, p)

6.

In oscillating pulse function (int oscillate ()) the advantage of using 'repeatCount' parameter is:

a. It will determine how many times the oscillation will repeat else the oscillation will continue forever
b. It will help to repeat the oscillation else the oscillation will stop
c. It changes the duty cycle accordingly
d. It helps to clear the noise in the pulse

Ans. a (It will determine how many times the oscillation will repeat else the oscillation will continue forever)
Justification: The 'repeatCount' parameter gives the count of oscillation as input so it does not continue oscillating forever.

7.

The function that is used to get the analog signal in Arduino is:

a. scanAnalog
b. readAnalog
c. analogRead
d. analogCheck

Ans. c (analogRead)
Justification: The function 'analogRead' reads the value from the specified analog pin. Arduino boards contain a multichannel, 10-bit analog to digital converter. This means that it will map input voltages between 0 and the operating voltage (5V or 3.3V) into integer values between 0 and 1023.

8.

In proportional control, the target value can never be achieved due to an error called:

a. Proportional error
b. Projection error
c. Rogue error
d. Steady-state error

Ans. d (steady-state error)
Justification: In proportional control, the error is known as steady-state error. The magnitude of the error depends on the system gain and will be never zero.

9.

Arduino ATmega328 uses the following hardware architecture:

a. RISC architecture
b. CISC architecture
c. MISC architecture
d. HISC architecture

Ans. a (RISC architecture)
Justification: Arduino ATmega328 uses 8-bit RISC architecture

10.

An Arduino ATmega328 has:

a. 14 digital I/O pins of which 8 provide PWM output
b. 14 digital I/O l pins of which 6 provide PWM output
c. 16 digital I/O pins of which 8 provide PWM output
d. 12 digital I/O pins of which 6 provide PWM output

Ans. b (14 digital I/O pins of which 6 provide PWM output)
Justification: An Arduino ATmega328 has 14 digital I/O pins of which 6 provide PWM output.

Week 6 Embedded system design

1. Processor using a single supply voltage V completes a task T just at its deadline , then V is the unique supply voltage that maximizes power consumption of T
   a. True
   b. False

Ans – b. False
Explanation – According to lemma given by Ishihara and Yasuura. Processor using a single supply voltage V completes a task T just at its deadline , then V is the unique supply voltage that minimizes power consumption of T.

2. Considering tighter time constraints, Energy Consumption
   a. Increases
   b. Decreases
   c. Remains Same
   d. Cannot be predicted

Ans – a. Increases
Explanation – If the time constraint is tight more energy is consumed because we need to push more cycles at higher voltage which leads to increased energy consumption

3. Power consumption depend(s) on
   a. Voltage
   b. Switching
   c. Load Capacitance
   d. All of the above

Ans – d. All of the above
Explanation – Power consumption depends on Supply Voltage, Lower Capacitance and Switching (of bits)

4. Decision in voltage scheduling in Static Voltage Scheduling is carried out
   a. At Runtime
   b. At Compile time
   c. Dynamically
   d. None of the Above

Ans – b. At Compile time
Explanation – The Voltage scheduling in Static Scheduling algorithm is taken at compile time, where deadline of each task is known and linear Programming problem is formulated and thus voltage levels are scheduled.

5.

Accessing registers uses less power than accessing primary memory

a. True
b. False

Ans - True
Explanation - Accessing registers consumes less power than accessing primary memory, that's why various measures are taken to reduce access to primary memory.

6.

In VLIW (Very Long Instruction Word) four independent instructions are clubbed together to form an Instruction word, the task of finding out Independent Instruction is carried out by

a. Programmer
b. Operating System
c. Compiler
d. Assembler

Ans- c. Compiler
Explanation- the four independent instructions clubbed together in VLIW (Very Long Instruction Word) is performed by the compiler.

7.

In EPIC (Explicitly Parallel Instruction Code) Architecture which bit position is used to encode the end of parallel execution?

a. MSB (Most Significant Bit)
b. LSB (Leas Significant Bit)

Ans – b. LSB (Least Significant Bit)
Explanation – as In EPIC (Explicitly Parallel Instruction Code) Architecture LSB (Least Significant Bit) bit position is used to encode the end of parallel execution.

8.

How many bit instructions are used in thumb mode of operation in ARM

a. 8
b. 10
c. 16
d. 32

Ans – c. 16
Explanation – In Thumb Mode operation processor works with 16bit instructions whereas in normally in expanded mode ARM can work with 32 bit instructions.

9.

Dictionary approach to attain code efficiency is based on the use of some kind of dictionary that contains parts of input sequence that frequently appears.

a. True
b. False

Ans – a. True
Explanation – Dictionary approach or two level control store approach helps in attaining code efficiency which is based on the use of dictionary that contains parts of input sequence that frequently appears.

10.

The factors achieved in VLIW (Very Long Instruction Word) is/are

a. Reduces the number of accesses to memory
b. Increases Parallelism
c. Pushing some overhead to compiler
d. None of the above

Ans – a. Reduces the number of accesses to memory, b. Increases Parallelism, c. Pushing some overhead to compiler

Explanation - VLIW reduces the total number of accesses to memory for fetching instructions, increases parallelism and pushes overhead to compiler for clubbing together four independent instructions.

Week 7

1. In saturation arithmetic if the result is restricted to unsigned 8 bits in binary, then which of the following is correct
    a. 17*17=289
    b. 17*18=256
    c. 17*17=255
    d. 17*18=306

Ans – c. 17*17=255

Explanation

17*17 gives 289 which is 0001 0010 0001 in binary and since it is 8 bit saturation arithmetic and the output is greater than 8 bits therefore the maximum value represented by 8 bits in binary i.e. 1111 1111 which is 255 in decimal, which is the output

2. DSP (Digital Signal processor) has/have
    a. Specific hardware for performing multiplication and addition operations in same cycle
    b. Saturation Arithmetic
    c. Zero Loop Overheard (hardware /Software)
    d. All of the above

Ans – d. All of the Above

Explanation – DSP follows Saturation arithmetic and has special memory architectures that can fetch multiple data or instruction at the same time to reduce the overall execution time and has special hardware for performing multiplication and addition operation in same cycle and has zero loop overhead, thus all these together helps to make DSPs more efficient.

3. Reuse of components helps in reducing time to market and can only be done in Hardware.
    a. True
    b. False

Ans – b. False

Explanation - Reuse of components helps in reducing time to market and can only be both done in Hardware as well as Software.

4. Which of the following data structure falls under the category of Static Data Structure
    a. Arrays
    b. Linked Lists
    c. Trees
    d. Graphs

Ans – a. Arrays

Explanation: Array is classified under static data structure whereas linked list, trees and graphs falls under dynamic data structure.

5. In Standard operating system Application layer can access device drivers
    a. True
    b. False

Ans – b. False

Explanation – In Standard operating system Application Layer has to access device drivers via Operating system whereas in RTOS (Real Time Operating System) supports direct access of device drivers from application layer.

6. RTOS requires files to be contiguous because
    a. Helps in predictable head movements
    b. Helps to manage task scheduling
    c. Helps in disabling interrupt

d. All of the above

Ans – a. it makes system predictable

Explanation – RTOS requires files to be contiguous. If a file is not contiguous it may lead to varying access times due to unpredictable head movements.

7. Total number of semaphore variable required for an unit resource to be accessed in a mutually exclusive fashion by N number of processes
    a. N
    b. 1
    c. N-1
    d. 2

Ans – b. 1

Explanation - Only one Binary Semaphore is sufficient to guarantee mutually exclusive access to a unit resource.

Every process need to follow the following sequence to access resource R

Let the semaphore be named S

1. P(S)
2. Resource
3. V(S)

Where P() and V() are atomic in nature.

8. When several processes access and manipulate same data concurrently and the outcome doesn't depend on the particular order in which access has taken place is known as race condition.
    a. True
    b. False

Ans – b. False

Explanation –Race condition is when multiple processes access and manipulates data concurrently and the output depends on the particular order in which access has taken place.

9. A cyclic dependency of resources among processes will always lead to deadlock.
    a. True
    b. False

Ans – b. False

Explanation – A cyclic dependency of resources may not always lead to deadlock as there may me multiple resources of the same type.

10. Rate Monotonic Scheduling uses which of the following approach(es)
    a. Tasks with shorter period are assigned last
    b. Preemptive
    c. first come first served
    d. last come first served

Ans – b. preemptive

Explanation – rate monotonic scheduling algorithm schedules periodic tasks using static priority along with preemption i.e. it gives higher priority to tasks with smaller time period.

1.

The output value of mealy state machine depends upon

a. The current state.
b. The input values.
c. The input value and the current state.
d. The input value, the current state and the previous state.

Ans. c (The input value and the current state)
Justification: The output value in mealy state machine depends upon the current state and the input value.

2.

The disadvantages of finite state machine are:

a. The finite state machines seldom show inconsistency.
b. The lack of ability to display the temporal behaviour of the system explicitly.
c. Not suitable for control dominated system.
d. Lack of hierarchy and concurrency.
e.

Ans. d (Lack of hierarchy and concurrency)
Justification: The finite state machines are suitable for displaying temporal behaviour explicitly and for control dominated systems. But when it tries to represent complex systems, lack of hierarchy and concurrency becomes the disadvantage of finite state machine as number of states and arcs increases greatly.

3.

In a super state, whenever super state is entered the default state to enter is called:

a. Default state
b. Sub state
c. Prior state
d. None of the above

Ans. a (Default state)
Justification: In a super state, unless specified otherwise, the default state to enter is called default state or entry state.

4.

Statement 1: A history node indicates the last active sub-state of a superstate.
Statement 2: A history node can not be combined with default entry node.

a. Statement 1 and 2 both are true.
b. Statement 1 is true but 2 is false.
c. Statement 2 is true but 1 is false.
d. Statement 1 and 2 both are false.

Ans. b (Statement 1 is true but 2 is false)
Justification: A history node keeps track of the last active substate from which superstate was exited so that when entering into the superstate the system can enter into the state from which it exited. A history node can be combined with the default entry node.

5.

In an AND-Super state:

a. One of the substate runs at a time.
b. The substates executes the same work parallelly.
c. All the substates run concurrently.
d. None of the above

Ans. c (All the substates run concurrently.)
Justification: In an AND-Super state all the substates works concurrently and executes different functions.

6.

Timer in in a state chart representation does the following:

a. When an input is given to a timer state it waits for a certain time and then the next state will be entered.
b. When a timer state is entered, other states are entered according to input value and if no input received within the certain time a predefined state is entered.
c. When a time state is entered, irrespective of the input, a predefined next state will be entered after the certain time.
d. If a timer state is entered after a certain time the timeout will take place and the process will be terminated.

Ans. B
Justification: When a timer state is entered, upon receiving input the control goes to respective states and if no input value is received within certain time, it enters to a predefined state.

7.

Statement 1: An event exists until next evaluation of the model.
Statement 2: A condition consist of a variable whose value can be reassigned.

a. Statement 1 and 2 both are true
b. Statement 1 is true but 2 is false
c. Statement 2 is true but 1 is false
d. Statement 1 and 2 both are false

Ans. a (Statement 1 and 2 both are true)
Justification: An event exist only until the model is revaluated.
A condition consists of variable which can be reassigned and until reassignment occurs the variables keep their value.

8.

The phases of evaluation of edge models are:

a. Evaluation of the effect, checking of condition and execution
b. Checking of condition, execution
c. Evaluation of the effect and effective transition with variables gaining new values
d. Evaluation of effect of external change on event and condition, computation of transitions and changing of values of variables

Ans. d (Evaluation of effect of external change on event and condition, computation of transitions and changing of values of variables)
Justification: The three phases of evaluation of an edge of the model is:
i) Effect of external changes on events and condition is evaluated.

ii) The set of transitions to be made in current state and right-hand sides of assignment are computed

iii) The transition becomes effective and variables obtain new values.

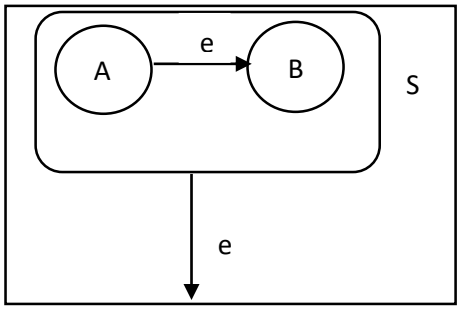
9.

In state chart the mode of communication used is:

a. Asynchronous message passing
b. Synchronous message passing
c. Broadcast
d. Semaphore

Ans. c (Broadcast)

Justification: In state chart broadcast mode of communication is used. It means if from a state an action generates an event, that event is visible to all other states.



In the following figure when event e occurs in state A the following will take place:

a. The control will go state B
b. The control will move from the super state S and will go to next state.
c. A conflict scenario will be generated
d. None of the above

Ans. c (A conflict scenario will be generated)

Justification: When the event shows in the picture occurs, a conflict scenario arises and a deterministic overcome is not possible in this case

1. The property of dynamic scheduling that makes it different from static scheduling is
   a. It is faster than the static scheduling
   b. It reschedules every time when a new process enters the queue
   c. For it the task with shorter deadline starve
   d. For it the tasks with longer deadline starve

   Ans. b (It reschedules every time when a new process enters the queue)

   Justification: Dynamic scheduling reschedules the task every time a new task enters the queue and, in this process, it may pre-empt a task.

2. Suppose 3 repetitive tasks be (4,1), (6,3), (9,3) (Consider period and deadline is same for these tasks) following earliest deadline first. All of them start at timestamp 0. When the timestamp 4 ends the following will take place
   a. Task 3 will start executing.
   b. Task 2 will continue being executed
   c. Task 1 will start executing
   d. Task 1 will be stopped and task 3 will execute.

   Ans. c (Task 1 will start executing)

   Justification: At time stamp 0 task 1 will start executing and will carry on for 1 unit. At time stamp 2 task 2 will start executing and will continue for 3 unit. Now after end of timestamp 4, task 1 reappears and its deadline is 4. The new deadline of task 3 is 5. So, task 1 will be assigned to be executed as its deadline is the earliest.

3. Schedulability check condition in earliest deadline first rule is
   a. Both sufficient and necessary condition to check whether tasks can be scheduled.
   b. Sufficient but not necessary condition to check schedulability.
   c. Necessary but not sufficient condition to check schedulability.
   d. Fails to check schedulability of the tasks in some cases. So, neither necessary nor sufficient.

   Ans. a (Both sufficient and necessary condition to check whether tasks can be scheduled)

   Justification: Schedulability check in earliest deadline first scheduling is both necessary and sufficient condition.

4. Suppose 3 task be (3,1), (5,3), (7,3). Can they be scheduled using earliest deadline first rule? (Period and deadline are same for these tasks)
   a. Yes
   b. No
   c. Can not be decided

   Ans. b (no)

   Justification: According to schedulability check ((1/3) + (3/5) + (3/7)) > 1. The condition is sufficient and necessary for tasks to be schedulable. As the condition fails, these tasks can not be scheduled.

5. Suppose two task T1 and T2 where the priority of T1 is greater than T2, have critical section for same resource starts executing at different time. T2 starts executing first and enters critical section and then the T1 enters the queue. The following will take place:
   a. T1 will start executing and when critical section of T2 comes, T2 will stop and T1 will start executing till its critical section ends.
   b. T1 will start executing and when the critical section comes, it will also keep executing as the critical section of T2 is halted.
   c. T2 will keep on being executed as it is performing critical section.
   d. The outcome can not be predicted.

   Ans. a (T1 will start executing and when critical section of T2 comes, T2 will stop and T1 will start executing till its critical section ends.)

Justification: When T1 enters the queue the critical section of T2 will stop and T1 will execute till its critical section arrives. Then T1 will be halted and T2 will be executed till its critical section is completed executing and next T1 will be executed.

6. Statement 1: For three or more than three processes having critical section for same resources, the blocking time of a process may even exceed the time required to compute critical section.
   Statement 2: If the scheduling test fails for RMS scheduling, no scheduling will be possible.
   a. Statement 1 and 2 both are true.
   b. Statement 1 is true but statement 2 is false.
   c. Statement 2 is true but statement 1 is false.
   d. Statement and 2 both are false.
   Ans. b (Statement 1 is true but statement 2 is false.)
   Justification: For three or more than processes having critical section for same resources, the blocking time of a process may even exceed the time required to compute critical section.
   In case of RMS the condition for schedulability was sufficient but not necessary, i.e. if the test fails, it does not make sure that no scheduling is possible.
7. The disadvantage of priority inversion protocol is:
   a. The process that does not need the critical section, starves.
   b. The process that appears later starves irrespective of its priority
   c. The process with longest critical section may starve
   d. When there are more than two process, the higher priority process which needs to access the critical section may starve.
   Ans. d (When there are more than two process, the higher priority process which needs to access the critical section may starve.)
   Justification: In priority inversion protocol the priority changes when some higher priority process asks for shared resource that is being accessed by lower priority process. So, one process may take long time due to access of critical section by other lower priority process which will hamper the real time system.
8. The disadvantages of priority inversion protocol can efficiently be overcome by
   a. Non pre-emption of process.
   b. RMS protocol
   c. Priority inheritance protocol
   d. Earliest deadline first protocol
   Ans. c (Priority inheritance protocol)
   Justification: Priority inheritance protocol is used to overcome the disadvantages of priority inversion protocol.
9. Statement 1: Disallowing pre-emption may cause starvation of higher priority process without critical section.
   Statement 2: In priority inversion protocol the priority changes when some higher priority process asks for shared resource that is being accessed by lower priority process.
   a. Statement 1 and 2 both are true.
   b. Statement 1 is true but 2 is false
   c. Statement 1 is false but 2 is true
   d. Statement 1 and 2 both are false.
   Ans. a (Statement 1 and 2 both are true.)
   Justification: Disallowing pre-emption may cause starvation of higher priority process without critical section. As in that case when a lower priority process enters into critical section, higher priority process without even need of the critical section waits for lower priority process to finish its critical section.

In priority inversion protocol the priority changes when some higher priority process asks for shared resource that is being accessed by lower priority process. Only after critical section finished being executed, the higher priority process starts executing.

10.

Suppose 3 tasks are following priority inheritance protocol and Pr(T1)> Pr(T2) > Pr(T3). Now T3 starts executing and enters critical section. Then T2 enters and pre-empts T1 and next T1 enters and pre-empts T2. Now when the T1 will require critical section following will take place:

a. T1 will start executing and after completion of task T1, T2 will start executing.
b. T3 will inherit the priority of T1 and it will execute its critical section and then T2 will start execution
c. T3 will inherit the priority of T1 and it will execute its critical section and then T1 will start execution
d. The tasks will enter into a deadlock situation as the critical section is hold by T3 and T1 is highest priority process.

Ans. c (T3 will inherit the priority of T1 and it will execute its critical section and then T1 will start execution)

Justification: In this case priority inheritance protocol will be followed and T3 will inherit the priority of T1 as priority inheritance is transitive property. After T3 completes execution of critical section, T1 will start executing the critical section.

1.

In SDL the mode of communication used is:

a. Asynchronous message passing
b. Synchronous message passing
c. Broadcast
d. Semaphore

Ans. a (Asynchronous message passing)
Justification: In state chart Asynchronous message passing is use for communication.

2.

The advantage of SDL over state chart is:

a. Exception handling is absent in state chart
b. State chart is not suitable for distributed systems
c. State chart is non-hierarchical
d. One of the above

Ans. b (State chart is not suitable for distributed systems)
Justification: As SDL follows asynchronous message passing for communication, it is more suitable for distributed systems than state charts

3.

The root block in hierarchy of SDL is called:

a. Block
b. Root
c. Header
d. System

Ans. d (System)
Justification: The root block in hierarchy of SDL is called system.

4.

The construct that is used in SDL to fetch current time is:

a. Current
b. Live
c. Now
d. Real

Ans. c (Now)
Justification: The construct used in SDL to fetch current time is now.
Example: set (now +p, T) will set a timer t that is the current time + p unit

5.

A data flow model consists of:

a. Data model, process and link
b. Process, data store, external entities and data flow
c. Process, interrupts, data link and data store
d. Data model, data queue, data link, data mart

Ans. b (Process, data store, external entities and data flow)
Justification: A data flow model consist of process, data store, external entities and data flow. Process corresponds to activities that transform data. Data flows are routes though which data flows, data stores hold or stores the data.

6.

The tasks in KAHN processing networks communicate between themselves using:

a. Asynchronous message passing
b. Synchronous message passing
c. Blocking
d. FIFO

Ans. d (FIFO)
Justification: In KAHN processing network, the tasks communicate between themselves using FIFO where it is assumed that there will be no overflow. There is one sender and one receiver per FIFO.

7.

In KPN the channels transmit message in:

a. Unpredictable but finite amount of time
b. Predictable and finite amount of tie
c. Unpredictable and uncertain amount of time
d. Infinite amount of time

Ans. a (Unpredictable but finite amount of time)
Justification: In KAHN processing network the transmit messages for unpredictable but finite amount of time. So the execution time becomes unknown.

8.

The disadvantage of KPN is

a. The number of processes is static
b. It is difficult to analyze
c. All of the above
d. None of the above

Ans. c (All of the above)
Justification: The disadvantages of KPN is that the number of processes is static so whenever new tasks arrives it can not be handles by KPN. Also, it's also difficult to analyze because of buffering and accumulation of tokens

9.

In synchronous data flow the mode of message passing is:

a. Asynchronous message passing
b. Synchronous message passing
c. Shared memory
d. LIFO

Ans. a (Asynchronous message passing)
Justification: In synchronous data flow, the mode of message passing is asynchronous message passing. In this case the tasks do not have wait for the output to be accepted.

10.

In synchronous data flow the global clock is used for:

a. At clock ticks the message passing takes place
b. The nodes are fired at the clock tick
c. All of the above
d. None of the above

Ans. b (The nodes are fired at the clock tick)
Justification: In SDF (synchronous data flow) the global clock is used and at the tick of the clock the nodes are fired

Week 11

1.

Register Sharing helps in reducing cost.

a. True
b. False

Ans – a. True
Explanation - Since all registers are not being used in same state, therefore connectivity costs can be reduced by combining the registers together.

2.

In connection merging, we can merge two connections if they are active at the same time.

a. True
b. False

Ans – b. False
Explanation – We cannot merge two connections if they are active at the same time because a connection cannot carry 2 separate data value at the same time.

3.

In Resource Constrained Scheduling given the time, we need to minimize the resources used.

a. True
b. False

Ans – b. False
Explanation – In Resource Constrained Scheduling we have resources specified to us and we need to minimize metrics like time, power etc.

4.

Windowing is a technique for image analysis.

a. True
b. False

Ans – b. False
Explanation - Windowing is a technique used to concentrate the processing in a desired part of image and also ignoring the non-desired part or non-interested part of the image. In this, an electronic mask is created around a small area of an image.

5.

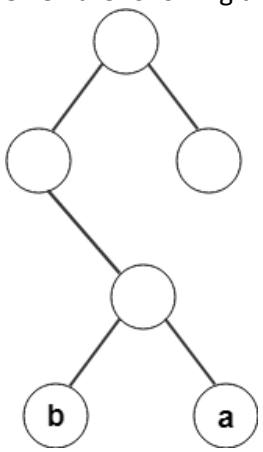
In Huffman Coding, we traverse the tree from root to leaf to obtain binary code of leaf's value, we append 1 for left traversal and 0 for right traversal.

a. True
b. False

Ans – b. False
Explanation - In Huffman Coding, we traverse the tree from root to leaf to obtain binary code of leaf's value, we append 0 for left traversal and 1 for right traversal.

6.

Given the following tree:



What is the codeword for ‘a’

a. 011
b. 010
c. 100
d. 101

Ans- a. 011
Explanation - recording the path of the node from root to leaf, the code word for character ‘a’ is found to be 011.

7.

CCD (Charge Coupled Devices) is an example of dynamic memory

a. True
b. False

Ans – a. True
Explanation – CCD is an example of dynamic memory because contents of it changes with time.

8.

Zero Bias Adjustment falls under Post Processing.

a. True
b. False

Ans – b. False
Explanation – Zero Bias Adjustment falls under pre-processing, it is done due to the reason that no manufacturing process is perfect so a pixel in CCD sensor being black may give a non zero value reading, thus to take corrective measure for the image captured Zero Bias Adjustment is performed.

9.

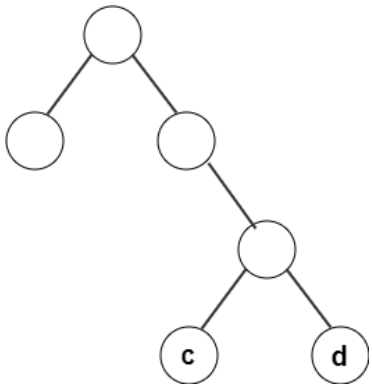
No of bits required for standard encoding if the size of character set is N is

a. N
b. 2N
c. $Log_2(N)$
d. N^2

Ans – c. $Log_2(N)$
Explanation – we need to satisfy the equation $2^x>=N$ where value of x is smallest. As each bit in binary has 2 values thus x bits can produce 2^x discrete combination.

10.

What is the codeword for ‘c’



a. 111
b. 101
c. 110
d. 011

Ans – c. 110
Explanation - recording the path of the node from root to leaf, the code word for character ‘a’ is found to be 110.

Assignment 12

MCQ:

1. A complete hardware implementation of a system leads to
   A. Fast working of the system.
   B. Increased cost.
   C. Increased power consumption.
   D. All of the above.

Solution: Option D. All of the above.

Explanation: This is the reason a hardware software co-design is preferred as the hardware aspect increases speed and the software aspect reduces cost and power consumption.

2. Which of the following operations help in optimization of the design of a system?
   A. Merging tasks
   B. Splitting tasks
   C. Both A and B
   D. None of the above

Solution: Option C. Both A and B

Explanation: Merging tasks with the same resources help to reduce cost and complexity of code. Splitting tasks having critical sections prone to deadlock, avoid priority inversion and makes the system free from delay.

3. Which facts about splitting tasks are true?
   A. Removes blocking of resources.
   B. Leads to less flexible scheduling
   C. Decreases overall efficiency
   D. All of the above

Solution: Option A. Removes blocking of resources.

Explanation: Splitting tasks increases flexibility of scheduling and possibly makes the system more efficient.

4. A system design can be validated using
   A. Simulation softwares
   B. Petri Nets
   C. State Machines
   D. All of the above

Solution: Option D. All of the above

Explanation: Fact.

5. Match the following:

Language	Storing multidimensional arrays
1. C	a. Column-major order
2. FORTRAN	b. Row-major order
3. Python	c. Table of tables
4. MATLAB	d. List of lists

A. 1-a;2-b;3-c;4-d
B. 1-d;2-b;3-c;4-c
C. 1-b;2-a;3d;4-a
D. None of the above

Solution: Option C. 1-b;2-a;3d;4-a
Explanation: Multidimensional arrays are stored in row or column major form to store the matrix form of data in a linear storage space like RAM. The spatiality locality of reference is exploited by the cache memory which prompts the usage of such techniques.

6. “The looping in DSPs is hardwired.”

A. True
B. False
C. Cannot be determined

Solution: Option A. True
Explanation: DSPs have hardwired looping units in order to reduce the overheads and ensure a fast and smooth computation.

7. Statement 1: “Simulation is very slow.”
Statement 2: “The complex circuits have a huge test bench that requires a lot of test runs making the simulation slow.”

A. Statement 1 is true and Statement 2 is the correct explanation of Statement 1.
B. Statement 1 is true and Statement 2 is not the correct explanation of Statement 1.
C. Both statements are false.

Solution: Option A. Statement 1 is true and Statement 2 is the correct explanation of Statement1.
Explanation: Fact

8. Suppose I build a calculator but the operations, addition and subtraction are swapped by mistake. Which of the following are correct?

A. The device does not pass verification.
B. The device does not pass validation.
C. The device passes verification but not validation.
D. None of the above.

Solution: Option A. The device does not pass verification.
Explanation: Verification checks if the product works according to specifications. Validation checks if the product to be built would complete the task at hand. The calculator performs the calculation hence the device is validated but the output is wrong and therefore the device does not pass verification.

9. Which of the following are parts of a DSP?

A. Address Generating Unit
B. Virtual memory
C. Both A and B
D. None of the above.

Solution: Option A. Address Generating Unit
Explanation: Virtual memory is absent in DSP since it increases the time of context switching and it affects performance.

10. “Two FSMs are equivalent when they take in the same input and for the same input, they produce the same output.”

A. True
B. False
C. Cannot be determined

Solution: Option A. True
Explanation: Fact

Short-Answer type(Alphanumeric answers only):

11. Optimize the following piece of code:
a = 2^k (^ refers to the exponent operator)

Solution: a = 1 << k
Explanation: << is the left shift operator and has a faster execution time than the ^ operator.

12. Optimize the following piece of code:

```
i = 12
if(i>13){
        i = i-1;
}
```

Solution: i = 12

Explanation: The if-block is a piece of dead code, which does not get executed since the value of i = 12 which is less than 13.