1. The possible ways to optimize a single-purpose processor is:
   a. To optimize the original program of the processor.
   b. To optimize FSMD by merging the stages in FSMD.
   c. Make sure for parallel execution of similar operations.
   d. All of the above.
   e. Option a and b both.

   Ans. e (Option a and b both)

   Justification: One can optimize single purpose processor by optimizing the original program, optimizing the FSMD by eliminating or merging the states. But parallel execution of similar operations is not possible because it will need more hardware support which is not optimal.

2. Optimization of data path can be done with:
   a. By merging the control bus and data bus.
   b. Reducing one to one mapping and effectively using the hardware.
   c. By making sure the similar type of tasks is executed parallelly in same time slot.
   d. Opting to use high level processors.

   Ans. b (Reducing one to one mapping and effectively using the hardware.)

   Justification: One to one mapping is not necessary. If similar operations take place in different stages, they can share same functional unit.

3. States can only be merged if they are equivalent states. Equivalent states are:
   a. States that perform similar type of operation.
   b. Time needed to execute the states are same so they can be merged together.
   c. For all possible input combinations states generate the same output and transitions to the same next state.
   d. None of the above.

   Ans. C (For all possible input combinations states generate the same output and transitions to the same next state.)

   Justification: States can only be merged if, for all possible input combinations states generate the same output and transitions to the same next state. These states are called equivalent states.

4. State the false statement.
   a. The embedded systems using GPPS takes relatively less time to market.
   b. The embedded system using single purpose processors are more versatile.
   c. The embedded system using FPGA are the fastest.
   d. The embedded system using ASIP are faster than embedded system using general purpose processor.

   Ans. b (The embedded system using single purpose processors are more versatile.)

   Justification: The embedded systems using general purpose processors are more versatile. Single purpose processors are designed considering a single type of tasks.

5. Field programmable gate arrays (FPGA) consists of:
   a. Configurable logic blocks.
   b. Single purpose processor.
   c. Programmable logic devices.
   d. Application specific instruction set processors.

   Ans. a (Configurable logic blocks.)

   Justification: FPGAs consists of an array of Configurable logic blocks (CLB).

6. State which is true among the statements about antifuse connection.
   a. The resistance is very high for antifuse.
   b. A capacitor is used for antifuse.
   c. It provides more flexibility than SRAM connection.
   d. It is permanent and hence can not be used further.

   Ans. d (It is permanent and hence can not be used further)

Justification: Antifuse connections are permanent and hence can not be further used. Antifuse connections are permanent and once it is done, it can not be redone.

7. Combinational logic can be implemented by
   a. Encoder and a look up table.
   b. Decoder and a look up table.
   c. Multiplexer.
   d. All of the above.
   e. b and c both.

   Ans. e (b and c both)

   Justification: Combinational logic can be implemented either by using a multiplexer or a decoder and a look-up table.

8. In SRAM connection:
   a. A pass transistor is used.
   b. An insulator is used that becomes conductor after a certain voltage.
   c. A capacitor is used that allows AC current to pass.
   d. An inductor is used.

   Ans. a (A pass transistor is used).

   Justification: In SRAM a pass transistor is used. It can be programmed and when the value is 1 it conducts and creates the connection and when value is 0 the connection is off.

9. The D flipflop is used in configurable logic block because
   a. To store all the results of the CLB.
   b. To use the previous state result from look-up table.
   c. It works as encoder.
   d. To halt the function of CLB.

   Ans. b (To use the previous state result from look-up table)

   Justification: In configurable logic block a d flipflop is used so that the value of look-up table can be used in next state so that a delay can be induced.

10. For a 2*2 control logic block based system, the number of switch box required is:
    a. 4
    b. 5
    c. 6
    d. 7

    Ans. b (5)

    Justification: For a 2*2 CLB based system, 5 switch box is required.