Question 1:

The schematic shown Fig. a represents a power BJT, Q_p, carrying collector current, I_o, of 15 A. A totem pole arrangement is used for driving Q_p. The base emitter drop of the power transistor, Q_p, and the drive transistors Q_{s1} and Q_{s2} are 0.8 V and 0.7 V respectively. The saturation current gain of all the BJTs is $\beta_{sat} = 10$. The gating signals are as shown in Fig. b.

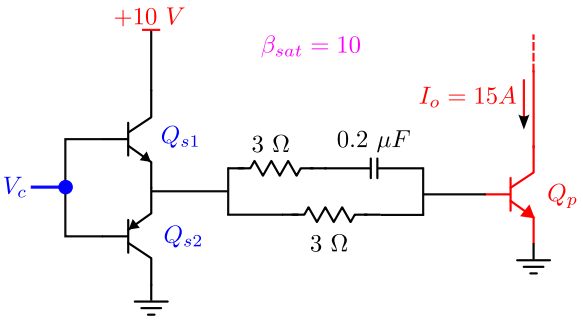


Fig. *a*

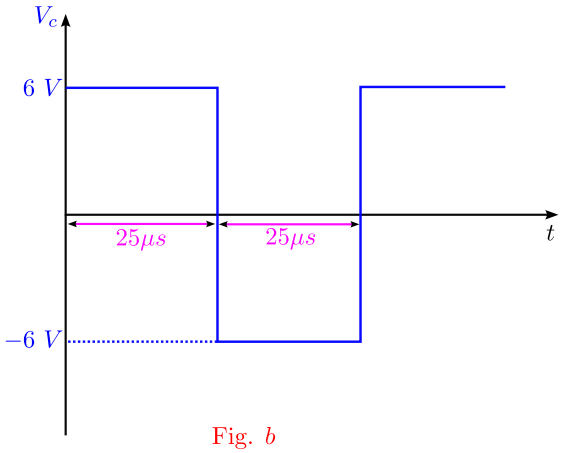


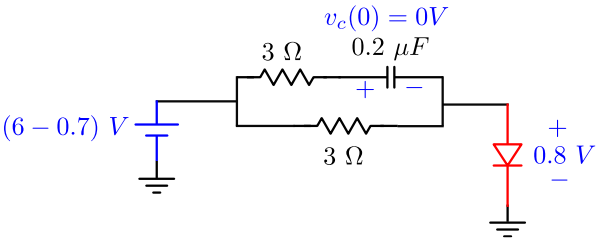
Fig. *b*

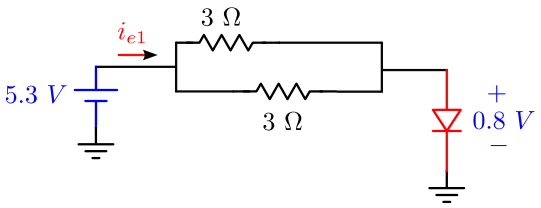
What will be the source and sink current of control input V_c. Assume the drive transistors to be in deep saturation.

(a) 500 mA, 500mA
(b) 500 mA, 928 mA
(c) 928 mA, 500 mA
(d) 928 mA, 928 mA

Solution: Correct option is (b)

To find the source current capability of the control input V_c we need to draw the equivalent circuit when $V_c = 6V$. During this period Q_{s1} is on. Thus, the equivalent circuit is as shown below





The capacitor is replaced by a short circuit as it is initially relaxed.

Thus, the emitter current of the switch Q_{s1}, represented as i_{e1} can be calculated as

$$i_{e1} = \frac{5.3 - 0.8}{1.5} A = 3 A$$

Now, if the designer chooses the drive transistor to be in deep saturation then

$$i_{e1} = i_{b1} + i_{c1} = i_{c1}\left(\frac{2}{\beta_{sat}} + 1\right) = 1.2 \times i_{c1}$$

Thus, the collector current of the drive switch Q_{s1} is

$$i_{c1} = \frac{i_{e1}}{1.2} = 2.5 A$$

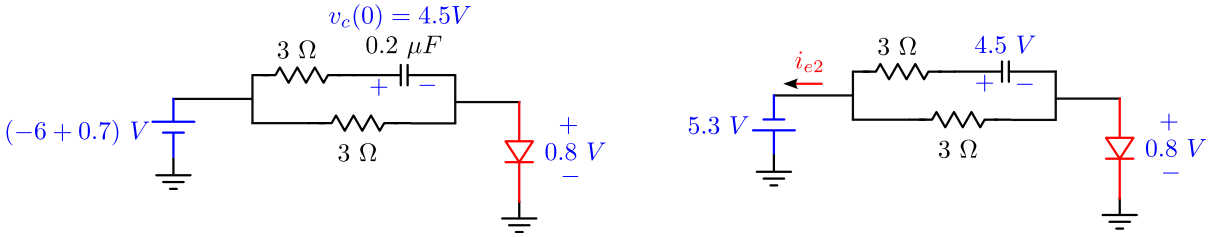
The base current of Q_{s1} is thus calculated as

$$i_{b1} = \frac{2i_{c1}}{\beta_{sat}} = 500\ mA$$

This current must be sourced from the control input V_c.

At the end of the positive half cycle of V_c, the capacitor is charged to a value $v_c = 5.3 - 0.8 = 4.5\ V$.

To find the sink current capability of the control input V_c we need to draw the equivalent circuit when $V_c = -6V$. During this period Q_{s2} is on. Thus, the equivalent circuit is as shown below



The stored charge in the depletion layer of the emitter base junction of the BJT is being removed during this period and hence the equivalent diode in the figure above is shown to carry current in the opposite direction.

Thus, the emitter current of the drive switch Q_{s2}, represented as i_{e2} can be calculated as

$$i_{e2} = \left(\frac{5.3 + 0.8}{3} + \frac{5.3 + 4.5 + 0.8}{3}\right) A = 5.567\ A$$

Thus, the collector current of drive switch Q_{s2} can be calculated as

$$i_{c2} = \frac{i_{e2}}{1.2} = 4.64\ A$$

The base current of Q_{s2} is thus calculated as

$$i_{b2} = \frac{2i_{c2}}{\beta_{sat}} = 928\ mA$$

This current must be sinked into the ground of the control input V_c.

Question 2:

In continuation to Question 1, what will be the source and sink current of the drive power source.

(a) 2.5 A, 2.5 A
(b) 4.64 A, 4.64 A
(c) 4.64 A, 2.5 A
(d) 2.5 A, 4.64 A

Solution: Correct option is (d)

We have already calculated the collector current flowing through the drive switch Q_{s1} during the positive half cycle of the control input V_c as given below

$$i_{c1} = \frac{i_{e1}}{1.2} = 2.5\ A$$

This current is being sourced from the drive power supply. Thus, the source current of the drive power supply is $2.5\ A$.

Similarly, during the negative half cycle of V_c, we have calculated the collector current flowing through the drive Q_{s2} as given below

$$i_{c2} = \frac{i_{e2}}{1.2} = 4.64\ A$$

This current must be sinked into the ground of the drive power supply. Thus, the sink current capability of the drive power supply must be $4.64\ A$.

Question 3:

A drive IC, shown in Fig. b, is capable of sinking and sourcing 1 A and is used to drive a MOSFET switch. The capacitance formed between the three terminals of the MOSFET switch and the threshold voltage is as below

$$C_{GS} = 1000\ pF,\ \ C_{DS} = 200\ pF,\ C_{GD} = 200\ pF,\ V_{th} = 4\ V$$

Find the value of R_g (in Ω) such that V_{GS} on turn-on reaches 10 V within 500 ns.

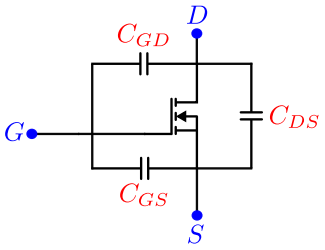


Fig. *a*

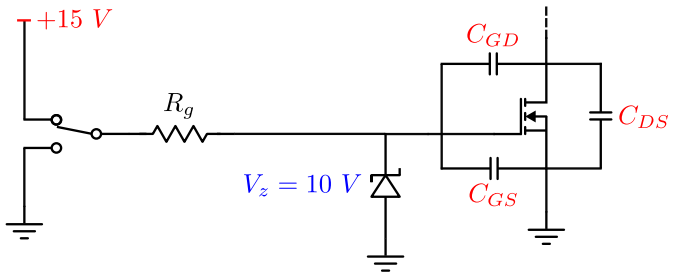
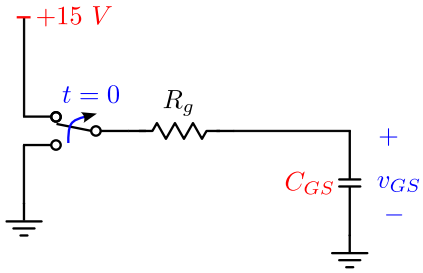


Fig. *b*

Solution: Answer range (454-456)

The equivalent circuit when the gate to source capacitance of the MOSFET is being charged is shown in the figure below



The equation for the voltage across the gate to source capacitance can be written as

$$v_{GS}(t) = 15\left(1 - e^{-\frac{t}{R_g C_{GS}}}\right)$$

v_{GS} reaches 10 V in 500 ns, thus from the above equation we have

$$10 = 15\left(1 - e^{-\frac{500\times10^{-9}}{R_g C_{GS}}}\right)$$

Solving the above equation we have

$$R_g = \frac{500 \times 10^{-9}}{C_{GS} \ln(3)} = 455.12\ \Omega$$

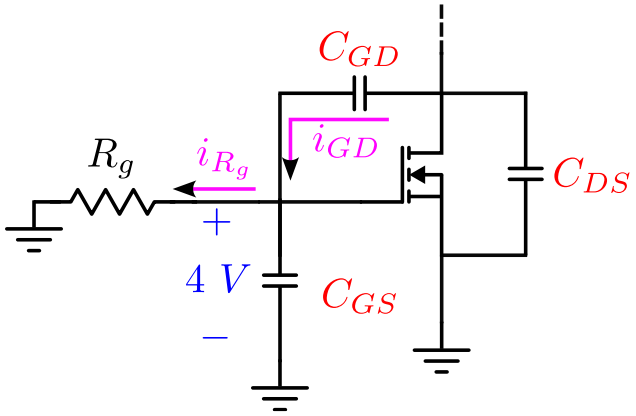
Question 4:

In continuation with Question 3, find the maximum off-time dV_{DS}/dt noise margin (in V/µs) that the MOSFET can withstand with the value of R_g calculated in Question 3.

Solution: Answer range (43-45)

We know that, the MOSFET starts conducting when V_{GS} is $\geq V_{th}$

To find the maximum dV_{DS}/dt, let us consider a limiting condition where the gate to source capacitance is already charged to $V_{th} = 4\,V$ and stays put at V_{th}. The equivalent circuit will then appear as shown in the figure below



As we are considering a condition where the gate to source voltage, v_{GS}, is fixed at $4\,V$, no current will be flowing through the capacitor C_{GS} as $\frac{dv_{GS}}{dt} = 0$.

Thus, applying KCL we can write,

$$C_{GD}\frac{dv_{GD}}{dt} = \frac{4}{R_g}$$

Where, v_{GD} is the gate to drain voltage. Now, as we have considered a case where v_{GS} stays put at $4\,V$

$$\frac{dv_{GD}}{dt} = \frac{dv_{DS}}{dt}$$

Since $v_{DS} = v_{GD} + v_{GS}$,

Thus, the maximum value of dV_{DS}/dt that the MOSFET can withstand during its off-time is

$$\frac{dv_{DS}}{dt} = \frac{4}{R_g C_{GD}} = 43.94\,V/\mu s$$

Question 5:

The drive circuit shown in Fig. a is used to control the power transistor switch Q_p. The device Q_p requires appropriate continuous positive base current during ON time and transient negative base current of at least 1.5 A for at least 2 μs during OFF time. The nature of base current during off time is shown in Fig. b. Evaluate the value of R_1 $(in\ \Omega)$. (Assume the power transistor to be in deep saturation and $V_{BE,sat} = 0V$).

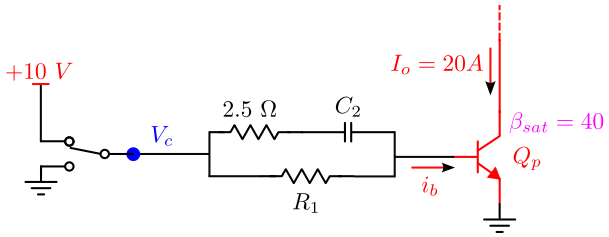


Fig. *a*

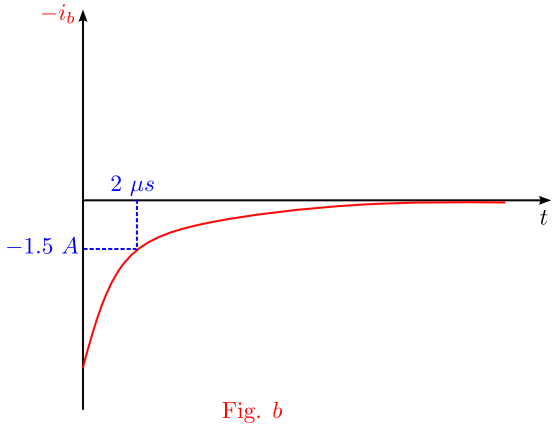


Fig. *b*

Solution: Answer range (10-12)

The transistor is carrying a collector current, $I_c = 20\ A$

As the power transistor is in deep saturation the base current can be calculated as

$$I_b = \frac{2 \times I_c}{\beta_{sat}} = 1\ A$$

This is the least value of base current that must always be supplied to the base of Q_p.

Once the capacitor C_2 is fully charged no current flows through 2.5 Ω. Thus, 1 A current will be flowing through R_1. Thus, the value of R_1 can be calculated as

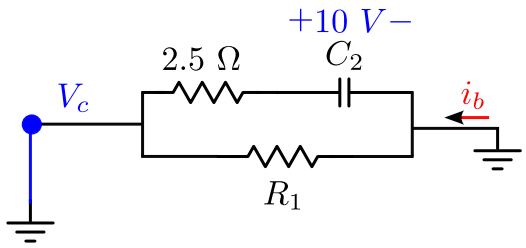
$$R_1 = \frac{V_c}{I_b} = 10\ \Omega$$

Question 6

In continuation with Question 5, evaluate the value of C_2 (in μF).

Solution: Answer range (0.8-0.9)

At the start of the off period the capacitor is charged to $10\ V$. Thus, the equivalent circuit can be drawn as



The direction of the base current i_b during off period is as indicated in the figure above. The equation for i_b can then be written as

$$i_b(t) = \frac{10}{2.5} e^{-\frac{t}{2.5 \times C_2}}$$

As mentioned in *Question 5*, $i_b(t)$ should be at least $1.5\ A$ for $2\ \mu s$, thus the waveform of $i_b(t)$ should be as shown in Fig. b of *Question 5*. Thus, equating the values we get

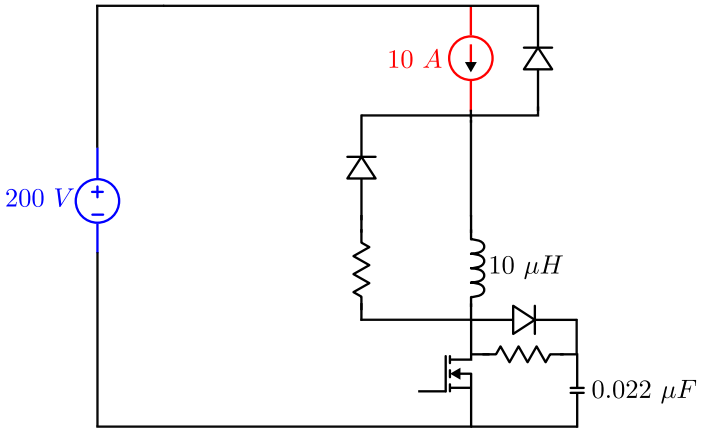
$$1.5 = \frac{10}{2.5} e^{-\frac{2 \times 10^{-6}}{2.5 \times C_2}}$$

Thus, the value of C_2 can be calculated as

$$C_2 = \frac{2 \times 10^{-6}}{2.5 \times \ln \frac{4}{1.5}} = 0.8156\ \mu F$$

Question 7:

The circuit shown below is a chopper operating at 10 kHz. Evaluate the switching losses in the snubber of the circuit (in Watts).



Solution: Answer range : (9.3-9.5)

Turn on snubber:

Energy stored in the inductor of turn on snubber circuit is

$$E_{on-snub} = \frac{1}{2} \times 10 \times 10^{-6} \times 10^2 = 0.5\ mJ$$

Thus, the power dissipated by the turn-on snubber circuit is

$$P_{on-snub} = E_{on-snub} \times f = 5W$$

This power will be dissipated in the resistor of the turn-on snubber circuit when the MOSFET is turned off.

Turn off snubber:

The voltage across the MOSFET when it is turned off is 200 V.

Energy stored in the capacitor of turn off snubber circuit is

$$E_{off-snub} = \frac{1}{2} \times 0.022 \times 10^{-6} \times 200^2 = 0.44\ mJ$$

Thus, the power dissipated by the turn-off snubber circuit is

$$P_{off-snub} = E_{off-snub} \times f = 4.4\ W$$

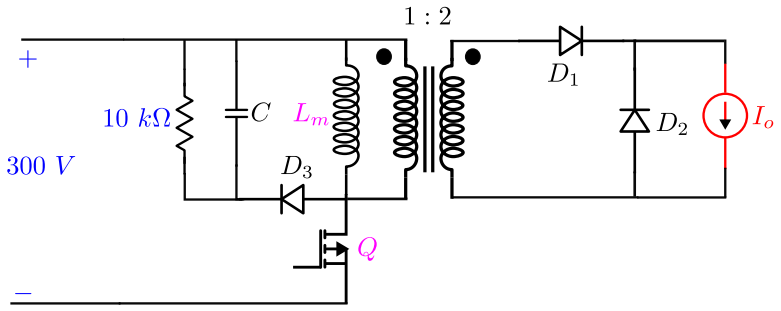
This power will be dissipated in the resistor of the turn-off snubber circuit when the MOSFET is turned on.

Thus, total power loss in the snubber circuit is

$$P_{snub} = P_{on-snub} + P_{off-snub} = 9.4\ W$$

Question 8:

The circuit shown below is a forward converter operating with a duty ratio of 50% *and a switching frequency of* $40\ kHz$*. The magnetizing inductance (*L_m*) of the isolation transformer is found to be* $20\ mH$*. Evaluate the losses in the snubber circuit in watts and rms value of the capacitor voltage.*



(a) 15 W, Not possible to calculate capacitor voltage due to data insufficiency.
(b) 18 W, 300 V
(c) 14.06 W, 300 V
(d) 14.06 W, 374.96 V

Solution: Correct option is (d)

The peak value of the magnetizing current when the MOSFET Q is on can be calculated as

$$I_m = \frac{V_{in}DT}{L_m} = 0.1875\ A$$

Thus, the energy stored in the magnetizing inductor can be calculated as

$$E_m = \frac{1}{2} \times L_m \times {I_m}^2 = 351.56\ \mu J$$

This power needs to be dissipated in the snubber resistor every cycle to reset the flux in the core. Thus, the power dissipated every cycle is

$$P_{snub} = 351.56 \times 10^{-6} \times f = \ 14.06\ W$$

The power is dissipated in the resistor and thus we can write

$$P_{snub} = \frac{V_{C,rms}^2}{R}$$

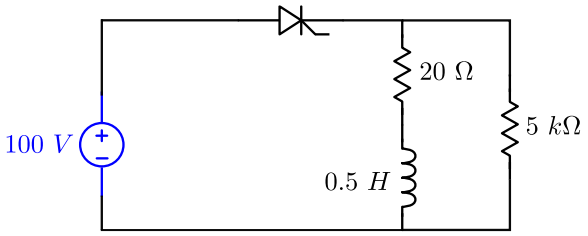
Thus, rms value of the capacitor voltage can be calculated as

$$V_{C,rms} = \sqrt{P_{snub} \times R} = 374.96\ V$$

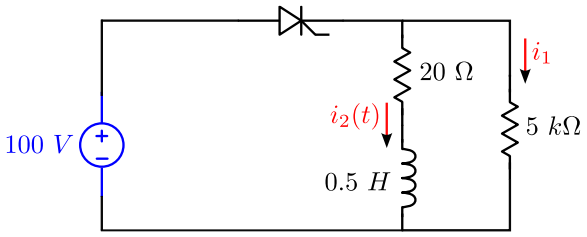
Question 9:

A thyristor having a turn on time of $5\ \mu s$*, latching current of* $50\ mA$ *and a holding current of* $40\ mA$ *is triggered by a short duration pulse and is used in the circuit shown below. The minimum pulse width required to turn the thyristor on will be*

(a) 251 μs
(b) 150 μs
(c) 100 μs
(d) 5 μs



Solution: Correct option is (b).



When positive pulse is applied to the gate of the thyristor, current through the thyristor starts increasing. Now, we can calculate i_1 as

$$i_1 = \frac{100}{5k} = 20\ mA$$

Now, the current through thyristor should reach the value of latching current when positive pulse is applied to the gate of thyristor. Thus, i_2 must reach the value of $30\ mA$ when gating signal is positive. The equation for the current $i_2(t)$ can be written as

$$i_2(t) = 5\left(1 - e^{-\frac{R}{L}t}\right) = 5\left(1 - e^{-\frac{20}{0.5}t}\right) = 5(1 - e^{-40t})$$

Now, the time required for $i_2(t)$ to reach $30\ mA$ can be calculated by solving the following equation

$$30 \times 10^{-3} = 5(1 - e^{-40t})$$

Thus, we can calculate the time required as

$$t = 150\ \mu s$$

Question 10

The circuit schematic given in Fig. a shows a step-down chopper with no snubber circuit connected across the switches. The diode has a stary inductance of $5\ nH$ *and a device capacitance of 100 pF. The diode current waveform is shown in Fig. b. Find the peak voltage that appears across the diode, when the switch* Q *is turned on.*

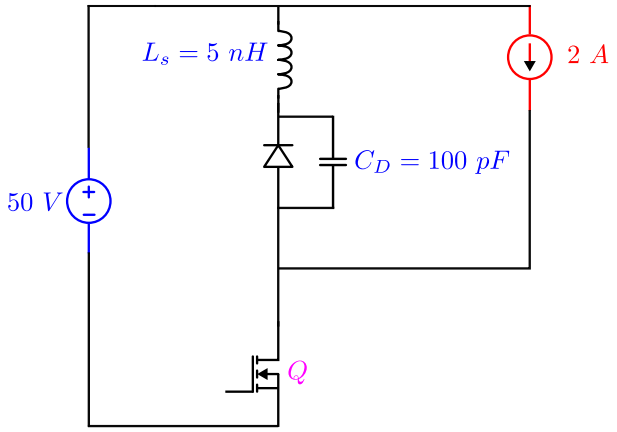


Fig. *a*

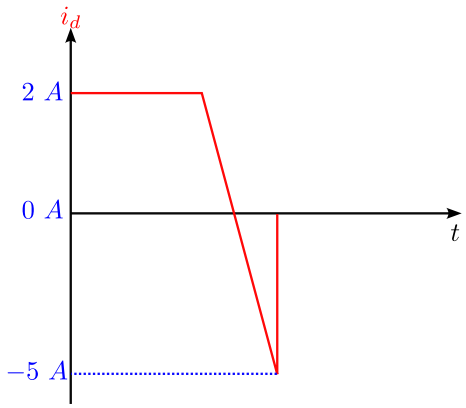


Fig *b*

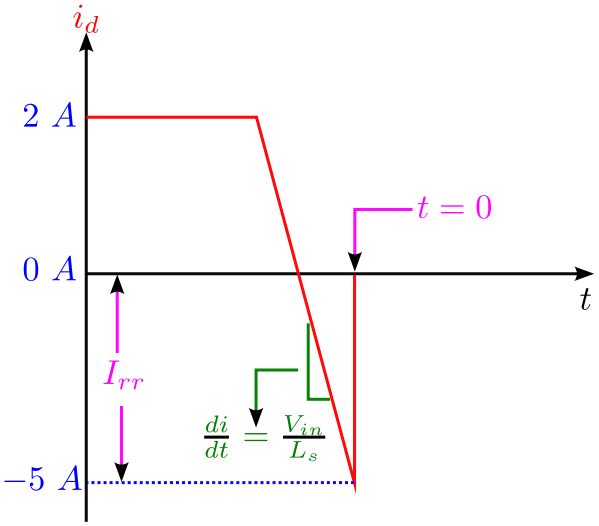
(a) 100.24 V
(b) 151.24 V
(c) 211 V
(d) 111.24 V

Solution: Correct option is (d)

From Fig. b of the question we can conclude that the diode snaps off abruptly when the current through the diode reaches its reverse recovery current

$$I_{rr} = 5A$$

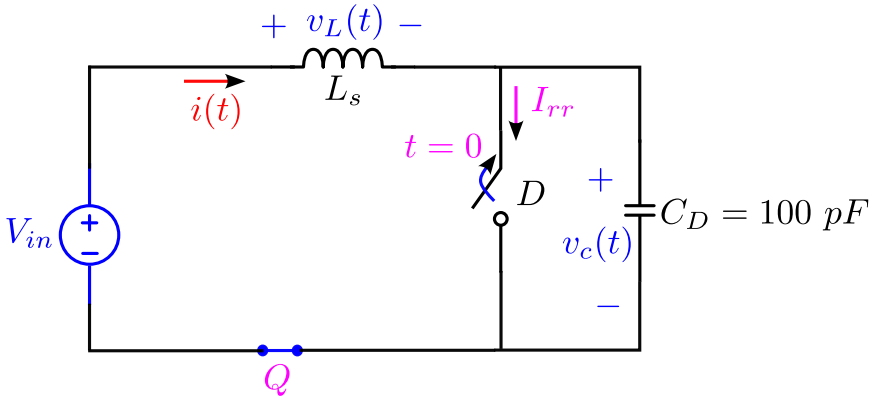
We will consider this instant as our time origin for our subsequent analysis.



Thus, at $t = 0$, the diode snaps off and the MOSFET is conducting. For analysing the circuit for $t > 0$, we thus have the following initial conditions

$$i(t = 0) = I_{rr} \quad and \quad \frac{di}{dt}(t = 0) = \frac{V_{in}}{L}$$

The equivalent circuit for $t \geq 0\ s$ can then be drawn as



The differential equation governing the stray inductor current can be written as

$$L_s \frac{d^2 i}{dt^2} + \frac{i}{C_D} = 0$$

Taking Laplace transform we can write

$$L_s \left(s^2 I(s) - s I_{rr} - \frac{V_{in}}{L_s} \right) + \frac{I(s)}{C_D} = 0$$

Solving for I(s) we get

$$I(s) = I_{rr} \frac{s}{s^2 + \frac{1}{L_s C_D}} + V_{in} \times \sqrt{\frac{C_D}{L_s}} \times \frac{\frac{1}{\sqrt{L_s C_D}}}{s^2 + \frac{1}{L_s C_D}}$$

Taking inverse Laplace transform we can write

$$i(t) = I_{rr} \cos(\omega_o t) + \frac{V_{in}}{Z_o} \sin(\omega_o t)$$

Where,

$$\omega_o = \frac{1}{\sqrt{L_s C_D}} \quad and \quad Z_o = \sqrt{\frac{L_s}{C_D}}$$

Thus, the voltage across the stray inductance can be calculated as

$$v_L(t) = V_{in} \cos(\omega_o t) - I_{rr} \sqrt{\frac{L_s}{C_D}} \sin(\omega_o t)$$

Thus, the equation for voltage across the diode is

$$v_c(t) = V_{in} - V_{in}\cos(\omega_o t) + I_{rr}\sqrt{\frac{L_s}{C_D}}\sin(\omega_o t)$$

Substituting the corresponding values, we can write

$$v_c(t) = 50 - 50\cos(\omega_o t) + 35.35\ \sin(\omega_o t)$$

The maximum value of the above expression is

$$V_{pk} = 50 + \sqrt{50^2 + 35.35^2} = 111.24\,V$$