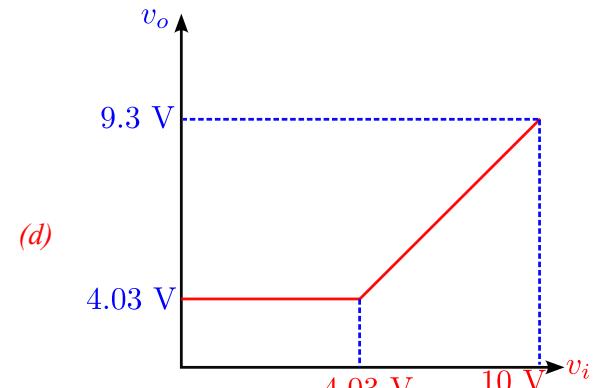
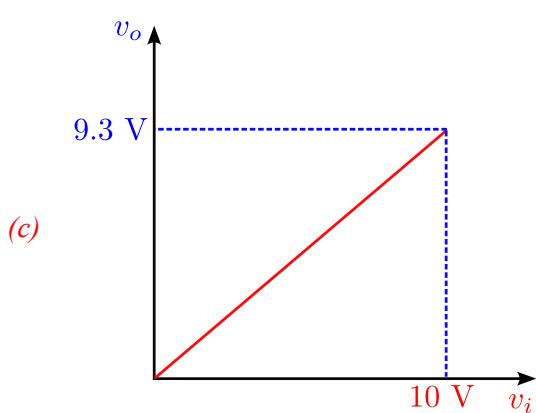
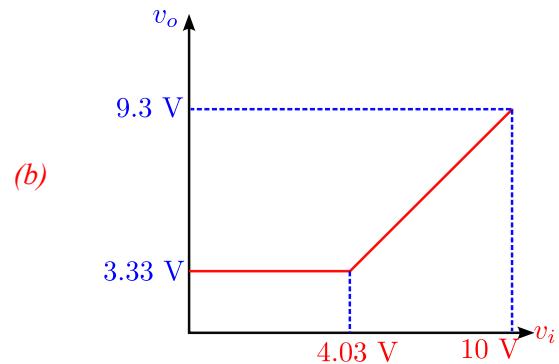
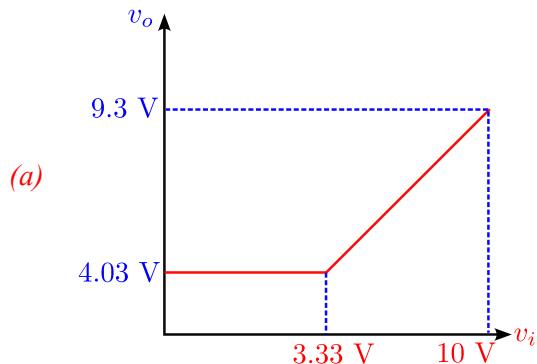
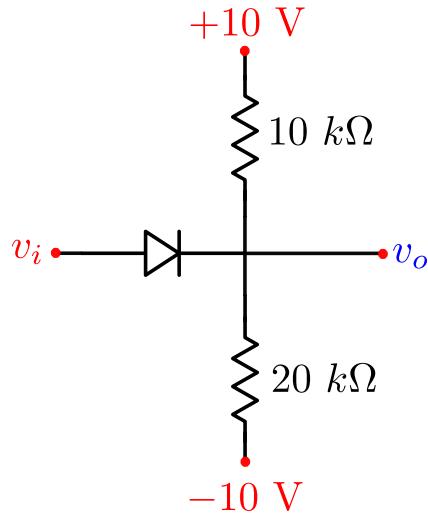


*Question 1:*

The diode in the circuit shown in the figure has a forward voltage drop ( $V_d$ ) of 0.7 V. The input voltage swing is in the range

$$-10 \text{ V} \leq v_i \leq 10 \text{ V}$$

Which of the following plots describes the input-output relation (plot of  $v_o$  versus  $v_i$ ) of the circuit



Solution:

The correct option is (b).

If the diode is not conducting the output voltage,

$$v_o = 10 - i \times 10 \times 10^3$$

When the diode is off, the current,

$$i = \frac{20}{30} \text{ mA}$$

Thus, when the diode is off the output voltage is

$$v_o = 10 - \frac{2}{3} \times 10 = 3.33 \text{ V}$$

The diode will start conducting only when

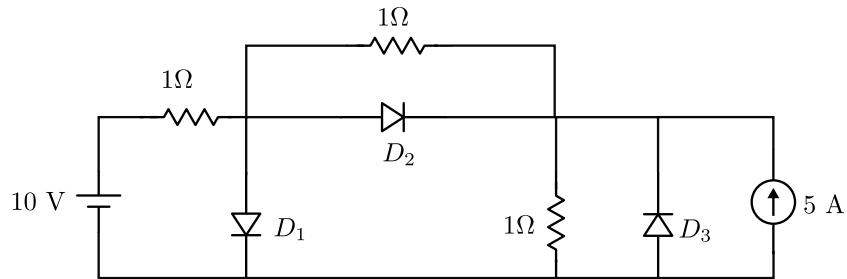
$$v_i \geq 3.33 + v_d, \text{ i.e. } v_i \geq 4.03 \text{ V}$$

Once the diode starts conducting

$$v_o = v_i - v_d = v_i - 0.7$$

*Question 2:*

*What are the states of the three ideal diodes of the circuit shown in the figure?*

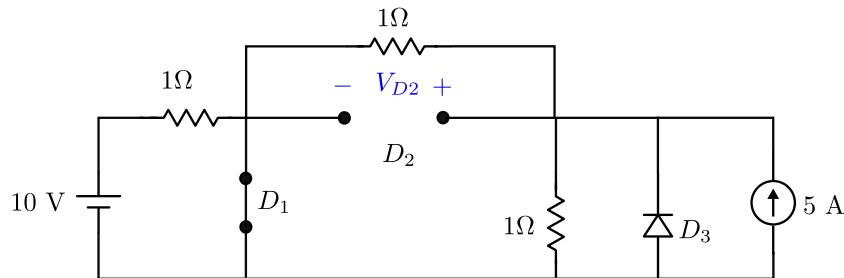


- (a)  $D_1 - OFF, D_2 - ON, D_3 - OFF$
- (b)  $D_1 - ON, D_2 - OFF, D_3 - OFF$
- (c)  $D_1 - ON, D_2 - OFF, D_3 - ON$
- (d)  $D_1 - OFF, D_2 - ON, D_3 - ON$

Solution: The correct option is (b)

Let us assume that  $D_1$  is ON.

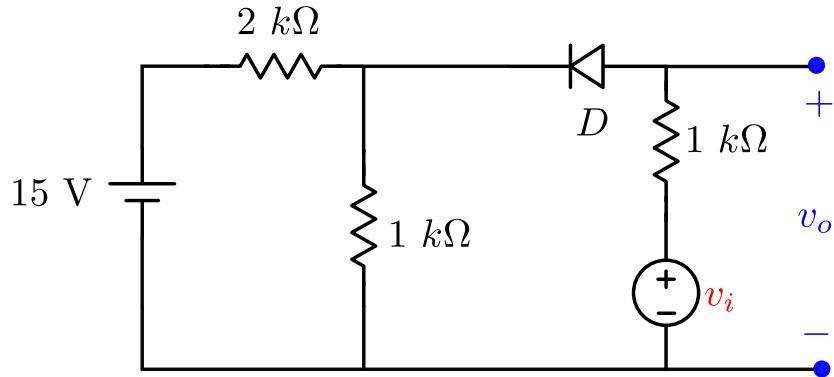
In such a case  $D_2$  will be reverse biased and hence will be OFF. Thus,  $V_{D2}$ , will have a polarity as shown in the figure below.



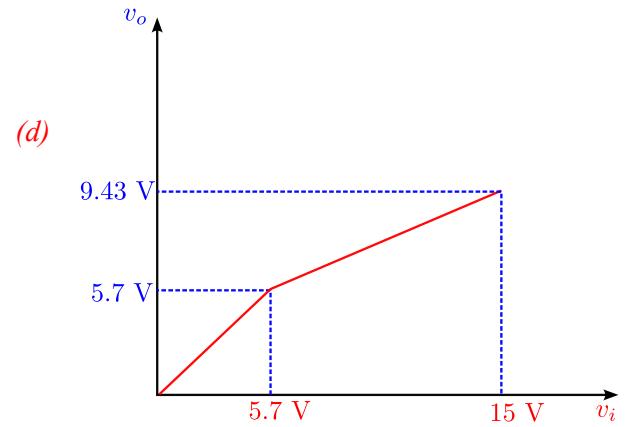
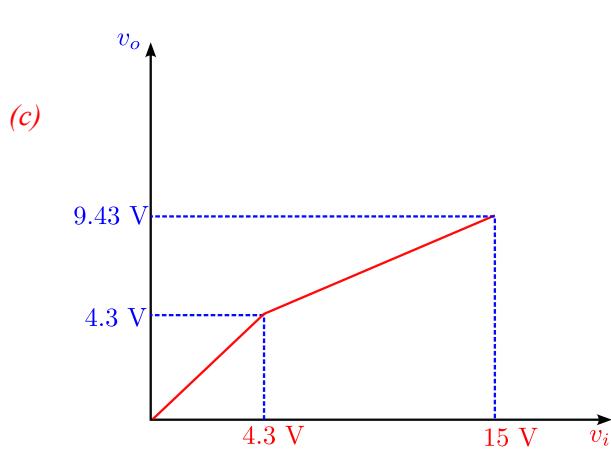
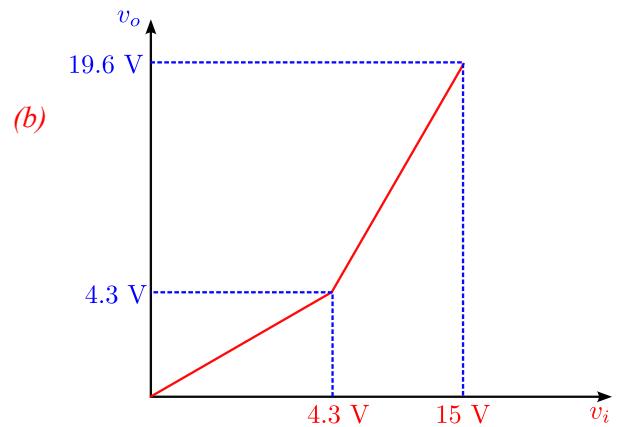
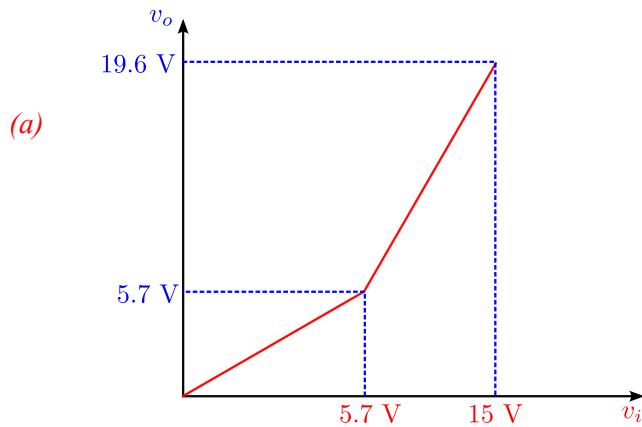
Such polarity of  $V_{D2}$  will reverse bias the diode  $D_3$  and hence  $D_3$  will be OFF. So all our assumptions were correct.

*Question 3:*

*For the circuit shown below the forward voltage drop ( $v_d$ ) is 0.7 V.*



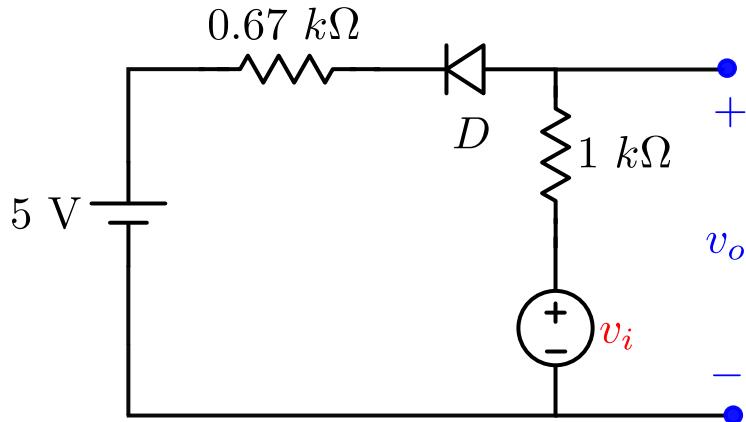
*Which of the  $v_o$  versus  $v_i$  plots best describe the transfer characteristics of the circuit.*



Solution:

The correct option is (d)

By using Thevenin's theorem the circuit can be redrawn as:



From the circuit we can conclude that the diode,  $D$ , will conduct only when

$$v_i > 5.7 \text{ V}$$

Thus, for  $v_i < 5.7 \text{ V}$ , the input output relation is given as

$$v_i = v_o$$

When  $v_i > 5.7 \text{ V}$ , the diode,  $D$ , will start conducting and the input output relation is given as

$$v_o = v_i - \frac{v_i - 0.7 - 5}{1.67} = 0.4 v_i + 3.413$$

**Question 4: Numerical type**

The forward characteristics of a power diode is given as

$$v_D = 0.79 + 0.02 i_D$$

Determine the average power loss (in Watts) for a constant current of 100 A for (2/3) of a cycle.

Solution: Answer range (185.9-186)

The average value of the diode current is

$$i_{D,avg} = 100 \times \frac{2}{3}$$

The rms value of the diode current is

$$i_{D,rms} = 100 \times \sqrt{\frac{2}{3}}$$

The average power loss in the diode is thus given by

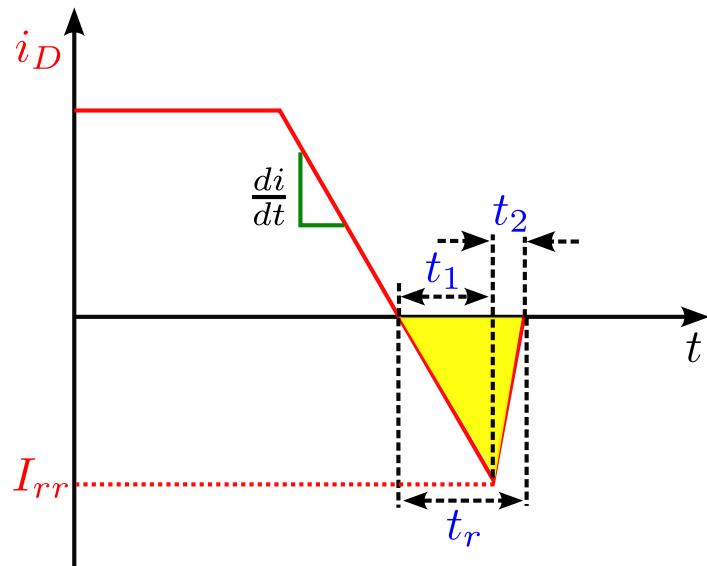
$$P_{loss} = i_{D,avg} \times 0.79 + i_{D,rms}^2 \times 0.02 = 186 W$$

Question 5:

A fast-recovery power diode is in the forward conduction mode and is turning off. The reverse recovery time of the diode is  $t_r$  and the rate of fall of diode current is  $\frac{di}{dt}$ . What is the stored charge in the PN junction of the power diode?

- (a)  $\frac{di}{dt} t_r$
- (b)  $\frac{1}{2} \frac{di}{dt} t_r$
- (c)  $\frac{1}{2} \frac{di}{dt} t_r^2$
- (d)  $\frac{1}{4} \frac{di}{dt} t_r^2$

Solution: Correct answer is (c)



Given that:

For a fast recovery diode  $t_r \approx t_1$

Peak reverse recovery current can be approximated as  $= \frac{di}{dt} t_r$

Stored charge = Area of the triangle shaded with yellow color =  $\frac{1}{2} I_{rr} t_r = \frac{1}{2} \frac{di}{dt} t_r^2$

**Question 6: Numerical type**

A power electronic switch is rated to carry full load current with an allowable case temperature of  $100^{\circ}\text{C}$  for maximum allowable junction temperature of  $125^{\circ}\text{C}$  and thermal resistance between case and ambience is  $0.5^{\circ}\text{C}/\text{W}$ . Find the sink temperature (in  $^{\circ}\text{C}$ ) for an ambient temperature of  $40^{\circ}\text{C}$ . Take thermal resistance between sink and ambient as  $0.4^{\circ}\text{C}/\text{W}$ .

**Solution:** Answer range (87-90)

$$\text{Power that has to be dissipated in the ambience} = \frac{T_{\text{Case}} - T_{\text{ambience}}}{\theta_{\text{case-ambience}}} = \frac{100 - 40}{0.5} \text{ Watts} = 120 \text{ Watts}$$

We want this power to be dissipated in the ambience and we need to find the temperature of the sink which will allow this power to be dissipated in the ambience.

Therefore,

$$120 = \frac{T_{\text{sink}} - T_{\text{ambience}}}{\theta_{\text{sink-ambience}}}$$

Therefore,

$$\begin{aligned} T_{\text{sink}} &= 120 \times \theta_{\text{sink-ambience}} + T_{\text{ambience}} \\ &= 120 \times 0.4 + 40 = 88^{\circ}\text{C} \text{ (Answer)} \end{aligned}$$

Where,

$T_{\text{case}}$  = Temperature of Case

$T_{\text{sink}}$  = Temperature of heat sink

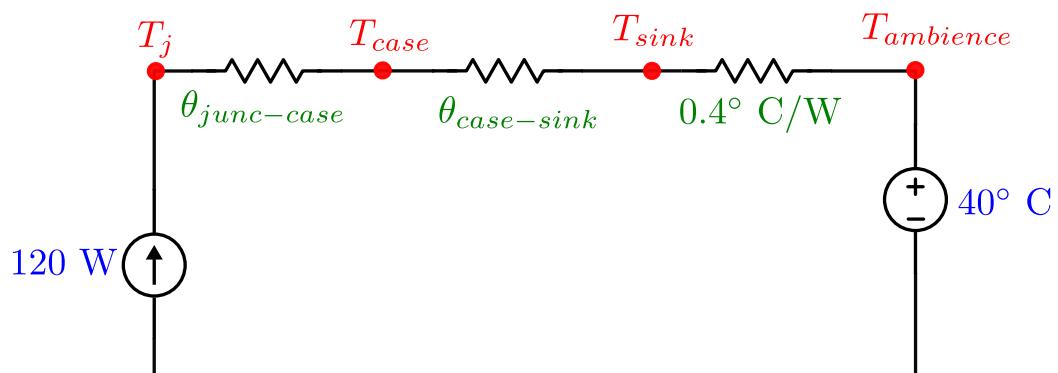
$T_{\text{ambience}}$  = Ambient temperature

$T_j$  = Junction temperature

$\theta_{\text{sink-ambience}}$  = sink to ambience thermal resistance

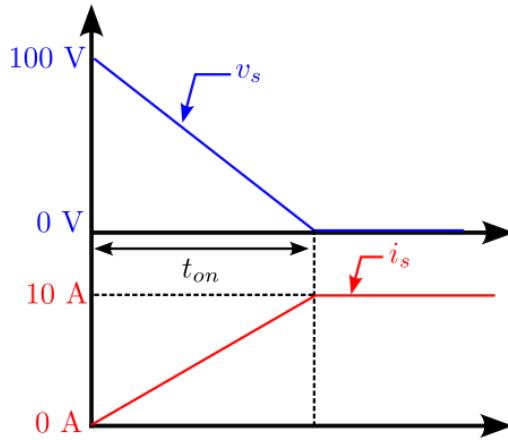
$\theta_{\text{case-ambience}}$  = case to ambience thermal resistance

$\theta_{\text{junc-case}}$  = Junction to case thermal resistance



**Question 7:**

The following figure shows on-transition of a switch. Find the peak instantaneous power loss in watts. Consider the turn on transition time ( $t_{on}$ ) = 5μsec and the total switching time period to be 50μsec.



- (a) 167 Watts
- (b) 500 Watts
- (c) 334 Watts
- (d) 250 Watts

Solution: Correct option is (d).

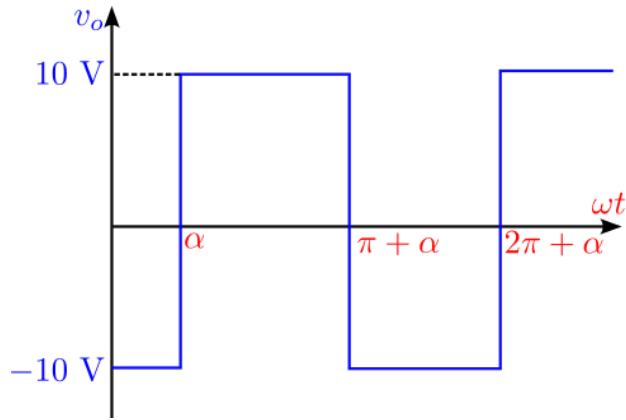
The peak instantaneous power would occur at  $\frac{t_{on}}{2}$ .

Therefore, the peak power is given by

$$P_{max} = v_s \left( t = \frac{t_{on}}{2} \right) \times i_s \left( t = \frac{t_{on}}{2} \right) = \frac{100}{2} \times \frac{10}{2} = 250 W$$

*Question 8:*

The output voltage of a power electronic converter is shown below. The rms value of the fundamental component will be.



(a)  $\frac{40}{\pi} \text{ V}$

(b)  $\frac{4}{\pi} \text{ V}$

(c)  $10 \text{ V}$

(d)  $9 \text{ V}$

Solution:

The correct option is (d).

The fundamental component of the square wave voltage is given by

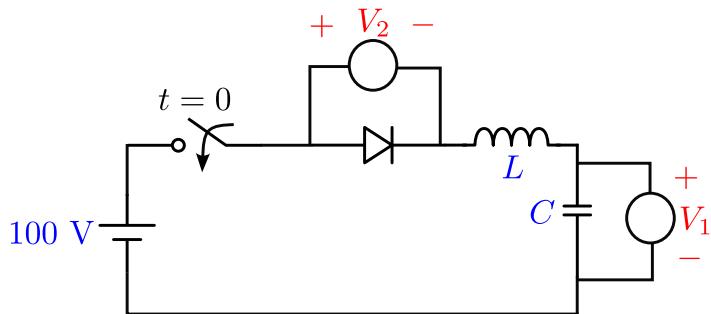
$$V_{o,1} = \frac{40}{\pi} \sin(\omega t - \alpha)$$

Thus, the rms value of the fundamental component will be

$$V_{o,1,rms} = \frac{40}{\pi \times \sqrt{2}} = 9 \text{ V}$$

*Question 9:*

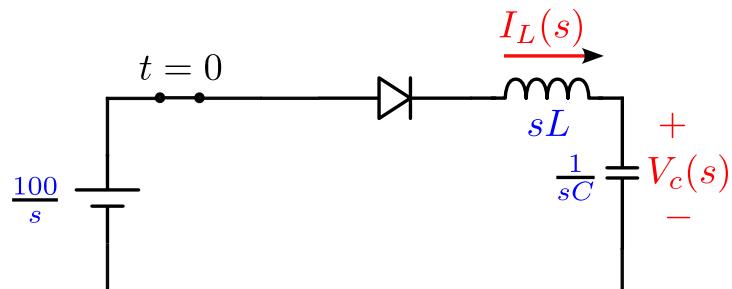
In the circuit shown in the figure  $V_1$ , and  $V_2$  are reading of zero centre PMMC (Permanent Magnet Moving Coil) voltmeters. The circuit is initially relaxed. The switch is closed at  $t=0$ . In steady state what will be the value of  $V_1$ ? (Assume the diode to be ideal)



- (a) 100 V
- (b) -100 V
- (c) 0 V
- (d) 200 V

**Solution:** Correct answer is (d)

At  $t = 0$ , when the switch is closed, the circuit can be redrawn to write the circuit equation in Laplace domain as shown in the figure below:



The KVL equation in s-domain can be written as:

$$\frac{100}{s} = (sL + \frac{1}{sC})I_L(s)$$

As, the circuit was initial conditions are zero i.e.  $i_L(t = 0) = 0 A$  and  $v_c(t = 0) = 0 V$  we can write the transfer function of the inductor current as

$$I_L(s) = 100 \sqrt{\frac{C}{L}} \left( \frac{1}{\frac{\sqrt{LC}}{s^2 + \frac{1}{LC}}} \right)$$

Now, taking inverse Laplace transform we get

$$i_L(t) = 100 \sqrt{\frac{C}{L}} \sin\left(\frac{t}{\sqrt{LC}}\right) = 100 \sqrt{\frac{C}{L}} \sin(\omega_o t)$$

The equation for capacitor voltage ,  $v_c(t)$  will then be given as

$$v_c(t) = \frac{1}{C} \int_0^t i_L(t) dt = 100(1 - \cos(\omega_o t))$$

Now, when  $\omega_o t > \pi$

$$i_L(t) < 0$$

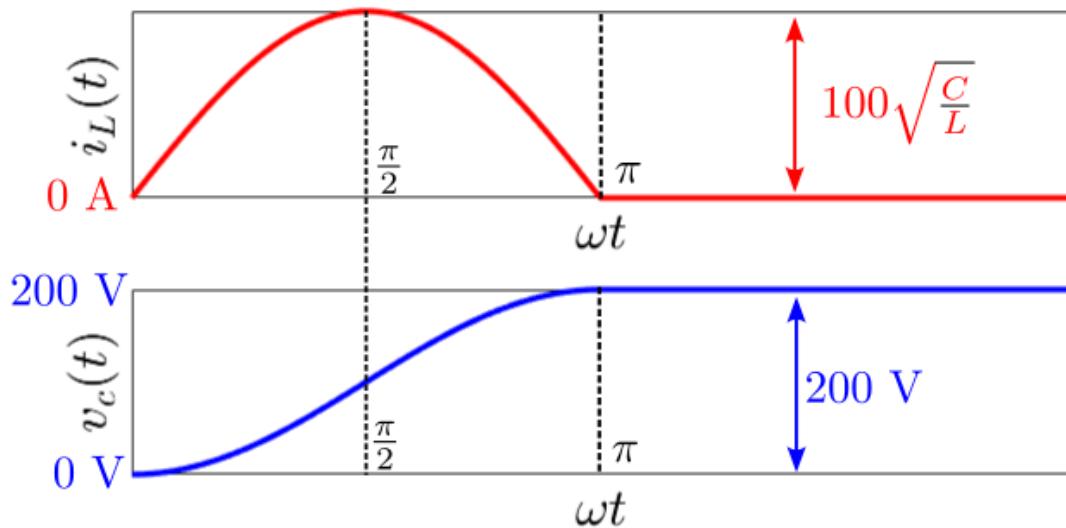
However, the diode will not allow  $i_L(t)$  to go below 0 A. Hence the diode gets turned off at  $\omega_o t = \pi$  and remains off.

The capacitor voltage at  $\omega_o t = \pi$  is given by

$$100(1 - \cos \pi) = 200 V$$

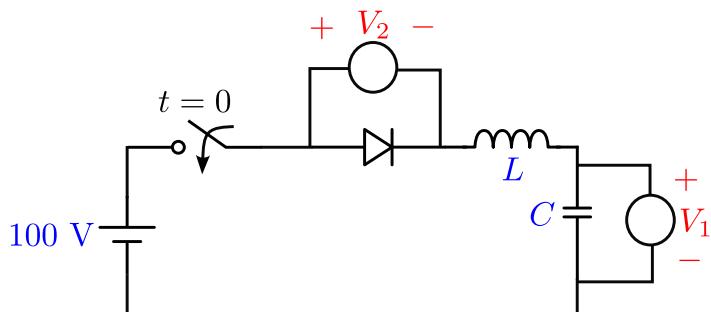
The capacitor voltage stays put at 200 V for  $\omega_o t > \pi$ . Thus the voltmeter reading  $V_1 = 200 V$ .

The waveforms of the inductor current or diode current,  $i_L(t)$ , and the capacitor voltage,  $v_c(t)$ , is shown in the figure below.



*Question 10:*

*In continuation to the previous problem, the circuit shown in the figure  $V_1$ , and  $V_2$  are reading of zero centre PMMC voltmeters. The circuit is initially relaxed. The switch is closed at  $t=0$ . In steady state what will be the value of  $V_2$  ?*



- (a) 100 V
- (b) -100 V
- (c) 0 V
- (d) 200 V

**Solution:** Correct option is (b)

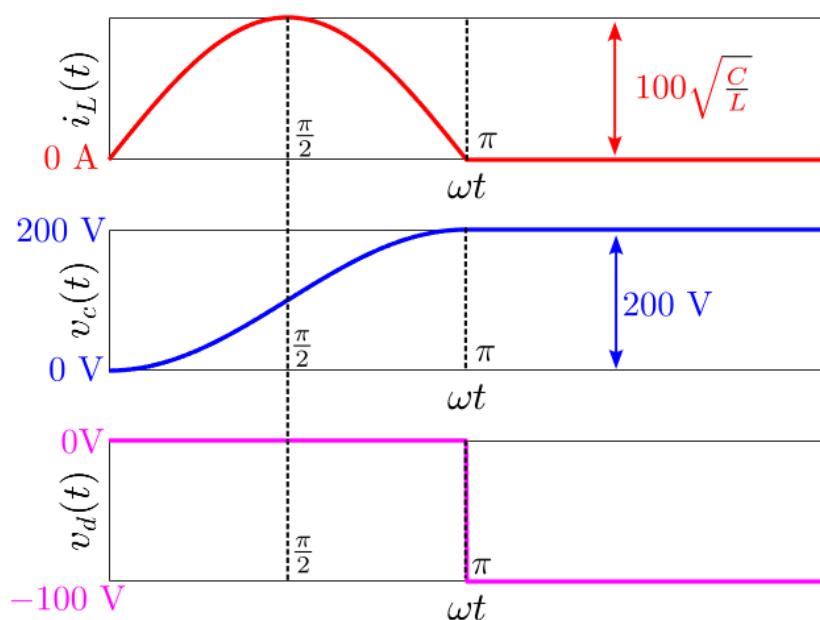
At steady state the voltage across the inductor,  $L = 0V$  as no current flows through it.

The voltage across the capacitor,  $V_1 = 200 V$ .

Therefore, at steady state the voltage across the diode,  $V_2$ , is given by

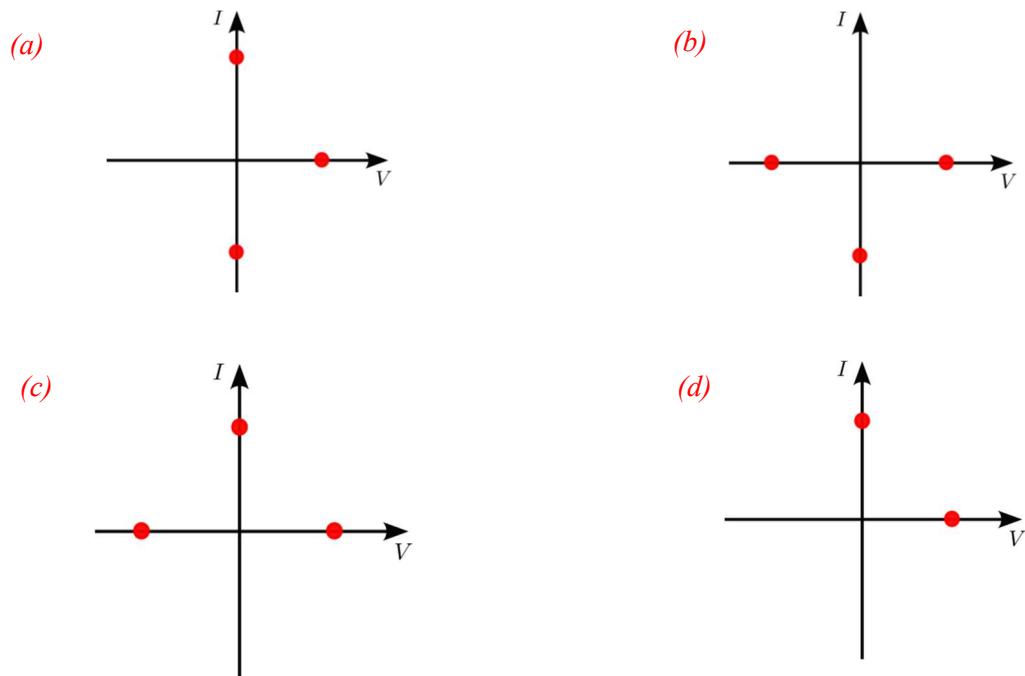
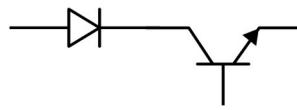
$$V_2 = 100 - V_1 = 100 - 200 = -100 V$$

The waveforms of the voltage across the capacitor,  $v_c(t)$ , the current through the inductor,  $i_L(t)$ , and the voltage across the diode,  $v_d(t)$  is shown in the figure below.



*Question 1:*

*Figure shows a power switching device. Identify the static operating points on V-I plane.*

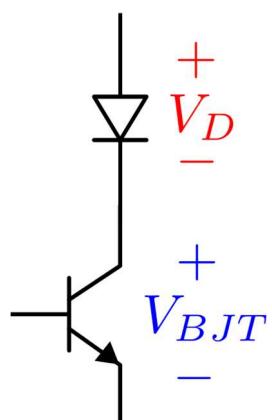


Solution:

The correct option is (c).

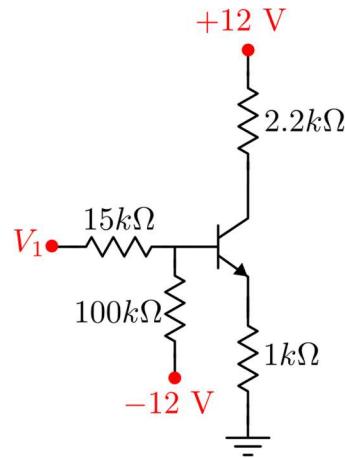
The series diode allows unidirectional flow of current.

BJT can block positive voltage (i.e.  $V_{BJT} > 0$  in blocking state) while the diode can block negative voltage (i.e.  $V_D < 0$  in blocking state or in other words when it is reverse biased) and hence the switching block acts as a bipolar device.

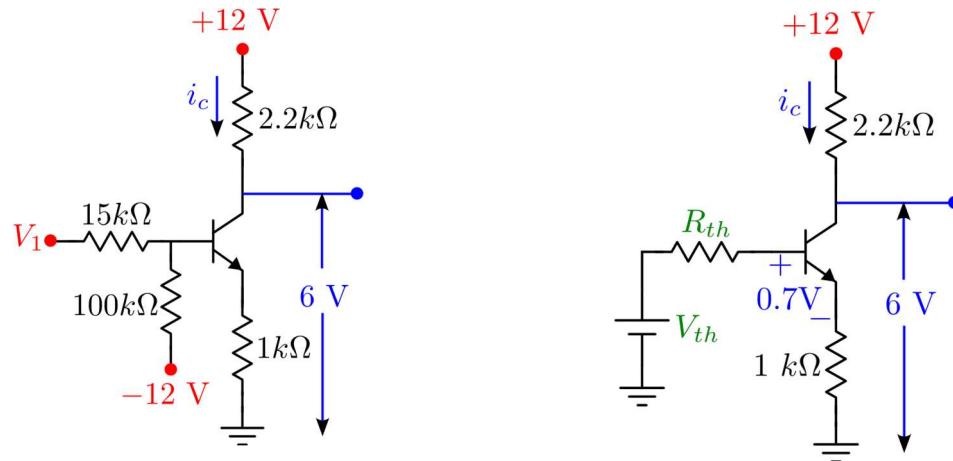


**Question 2: Numerical type**

For the given transistor,  $\beta = 30$  and the collector to emitter voltage  $V_{CE} = 6 V$ . The value of  $V_1$  (in V) is \_\_\_\_\_.



Solution: Range (7-8)



The collector current,  $i_c$ , can be calculated as

$$i_c = \frac{12 - 6}{2.2} \text{ mA} = 2.72 \text{ mA}$$

As  $V_{CE} > 0.3 \text{ V}$ , the transistor is in active region and hence the base current,  $i_b$  can be calculated as

$$i_b = \frac{i_c}{\beta} = \frac{2.72}{30} \text{ mA} = 0.09 \text{ mA}$$

By applying Thevenin's theorem we can calculate the Thevenin's Voltage as seen from the base terminal is

$$V_{th} = \frac{100 V_1 - 180}{115}$$

Similarly, Thevenin's resistance as seen from the base terminals can be calculated as below

$$R_{th} = \frac{15 \times 100}{15 + 100} k\Omega = 13.043 k\Omega$$

By applying KVL we can write

$$V_{th} = i_b R_{th} + 0.7 + (1 + \beta) i_b$$

Thus, we now have

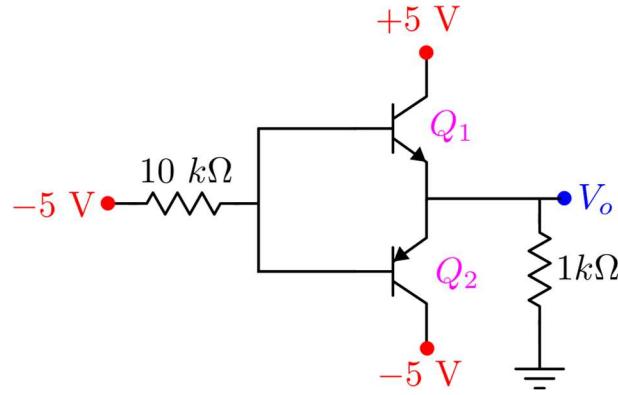
$$\frac{100 V_1 - 180}{115} = 4.66$$

Solving the equation we get:

$$V_1 = 7.16 V$$

*Question 3:*

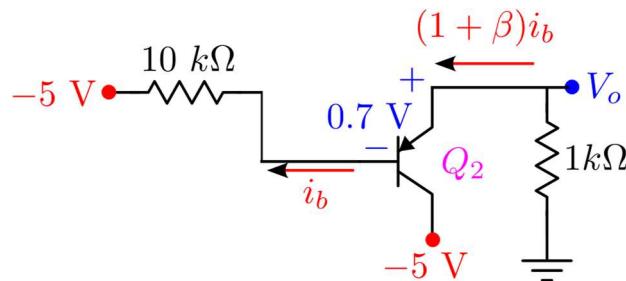
For the circuit shown below  $\beta = 100$ , and the base to emitter or emitter to base voltage ( $|V_{BE}|$ ) is 0.7 V. What is the value of the output voltage  $V_o$ .



- (a) -3.91 V
- (b) -4.8 V
- (c) 3.91 V
- (d) 4.8 V

Solution: Correct option is (a)

The base to emitter junction of  $Q_1$  is reverse biased and hence  $Q_1$  will remain off. Thus, the circuit can be redrawn as shown in the figure below.



Applying KVL we can write

$$(1k \times (1 + \beta)i_b) + 0.7 + (10k \times i_b) - 5 = 0$$

Thus, the value of the base current is given by

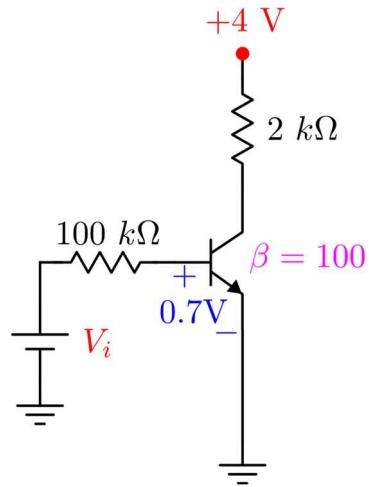
$$i_b = \frac{5 - 0.7}{10k + (1 + \beta) \times 1k} = 0.038 \text{ mA}$$

The value of the output voltage can then be calculated as

$$V_o = -(1 + \beta)i_b \times 1k = -3.91 \text{ V}$$

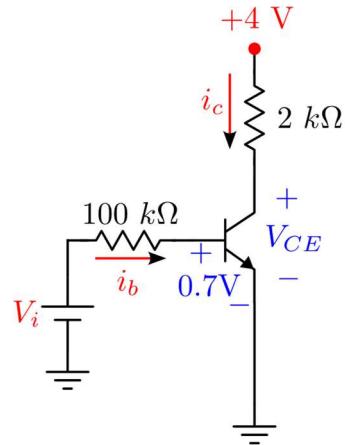
Question 4:

For the transistor circuit shown, the minimum value of  $V_i$  for the transistor to be in saturation region is \_\_\_\_\_ (Assume the collector to emitter voltage under saturation ( $V_{CE}^{sat}$ ) = 0.2 V)



- (a) 1.65 V
- (b) 2.65 V
- (c) 3.65 V
- (d) 3.85 V

Solution: Correct option is (b)



As the transistor is in saturation, the collector current,  $i_c$ , can be calculated as

$$i_c = \frac{4 - (V_{CE})_{sat}}{2} \text{ mA} = 1.9 \text{ mA}$$

The expression for the base current,  $i_b$ , can be obtained as

$$i_b = \frac{V_i - 0.7}{100} \text{ mA}$$

For the transistor to be in saturation it needs to satisfy the following condition

$$i_b > \frac{i_c}{\beta}$$

Therefore, we have the following relation.

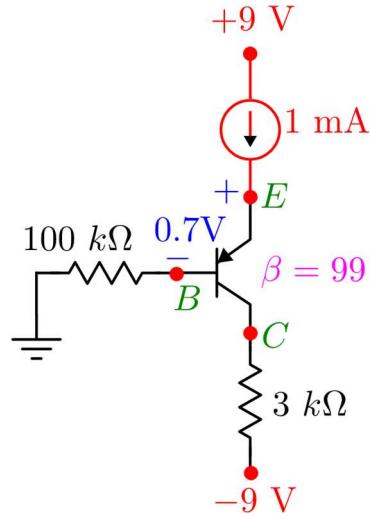
$$\frac{V_i - 0.7}{100} > \frac{1.9}{100}$$

Thus, for the BJT to be in saturation the following condition must hold.

$$V_i > 2.6 V$$

**Question 5: Numerical Type**

Find the conduction losses in the transistor circuit shown in the figure in mW.



Solution: Range (7-8)

The emitter current,  $i_e = 1 \text{ mA}$  as given in the circuit schematic. Thus, the base current,  $i_b$ , can be calculated as

$$i_b = \frac{i_e}{1 + \beta} = \frac{1}{1 + 99} \text{ mA} = 10^{-2} \text{ mA}$$

Thus, the potential at point B w.r.t ground can be written as

$$V_B = 100 \times i_b = 1 \text{ V}$$

Thus, the emitter voltage can now be calculated as

$$V_E = V_B + 0.7 = 1.7 \text{ V}$$

Now, we can calculate the collector current,  $i_c$ , as

$$i_c = \beta i_b = 99 \times 10^{-2} \text{ mA}$$

Now, the potential at point C w.r.t ground can then be calculated as

$$V_C = -9 + 3k \times i_c = -6.03 \text{ V}$$

Thus, the emitter to collector voltage can be calculated as

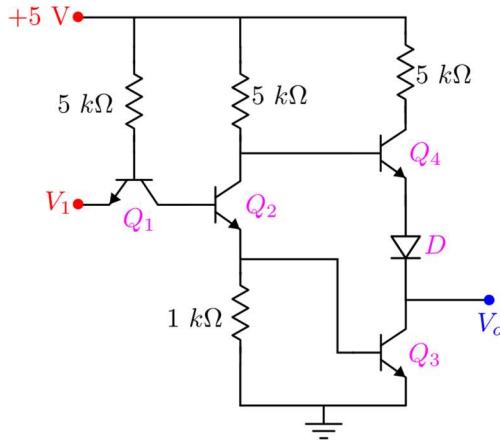
$$V_{EC} = 1.7 + 6.03 = 7.73 \text{ V}$$

The power dissipated can be calculated as

$$P_{loss} = V_{EC} \times i_c = 7.65 \text{ mW}$$

**Question 6:**

$V_1$  is a single input and  $V_o$  is the output. Consider a situation when  $V_1 = 3.3 \text{ V}$  (high), then which of the statements will be correct. Assume all the BJTs are acting as switches. (Assume the collector to emitter voltage under saturation  $(V_{CE})_{sat} = 0.2 \text{ V}$ ,  $(V_{BE})_{sat} = 0.8 \text{ V}$ , and  $\beta \rightarrow \infty$  and Forward diode drop  $V_F = 0.7 \text{ V}$ )



*Statement 1:  $Q_1$  and  $Q_3$  will saturate.*

*Statement 2:  $Q_4$  cut off and diode D does not conduct.*

*Statement 3:  $V_o$  is low*

*Statement 4:  $V_o$  is high*

- (a) 1, 2
- (b) 2,3
- (c) 1,3
- (d) 2,4

**Solution:** Correct option is (b)

Whatever be the value of  $V_1$ ,  $V_1$  will not be able to drive the base of Q2 as bi-directional current flow is not possible in BJT. Therefore, Q1 is OFF and the Base-Collector junction of Q1 will become forward biased and drive the base of Q2. Since  $\beta \rightarrow \infty$ , Base current tends to zero. So Base of Q1 has a voltage of 5V. The voltage at the Base of Q2 will be somewhere between  $4 < V_{B2} < 5$  due to the drop at the base collector junction of Q1.

Assume Q2 to be ON. Since  $\beta \rightarrow \infty$ ,  $I_{C2} = I_{E2}$ , find the current by applying KVL.

$$I_{C2} = \frac{5 - 0.2}{5K + 1K} = 0.8 \text{ mA}$$

Find the voltage at the collector and emitter of Q2.

$$V_{C2} = 5 - (5K \times 0.8 \text{ mA}) = 1 \text{ V}$$

$$V_{E2} = V_{C2} - 0.2 = 0.8 \text{ V}$$

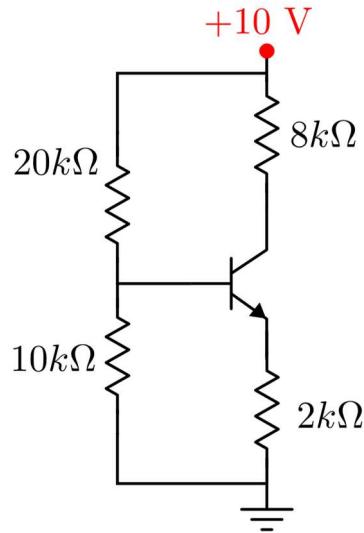
If we compare the voltage,  $V_{B2}, V_{E2}, V_{C2}$  we can see that both Base-Emitter and Base-Collector junctions are forward biased and thus Q2 is in saturation and our assumption is correct.

Now  $V_{C2} = 1V$ , but to drive Q4 and the diode D, we need a voltage greater than their respective forward drops i.e.  $0.8+0.7=1.5V$ . Therefore, Q4 is cut off and the diode does not conduct.

Now  $V_{E2} = 0.8V$ , will drive the base of Q3 and Q3 will go into saturation. Since Q3 is in saturation,  $V_o$  is tied to the ground through Q3 and therefore  $V_o$  is low.

*Question 7:*

For the circuit shown in the figure, the transistor is in \_\_\_\_\_ (take  $\beta = 100$ ).



- (a) Cut off region
- (b) Saturation region
- (c) Active region
- (d) None

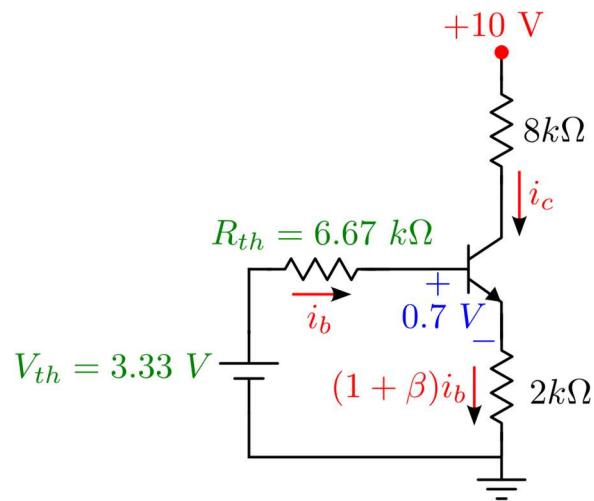
Solution: **Correct option is (b)**

By applying Thevenin's theorem, the Thevenin voltage and Thevenin resistance as seen from the base terminal of the BJT can be calculated as

$$V_{th} = 10 \times \frac{10}{30} = 3.33 \text{ V}$$

$$R_{th} = \frac{20 \times 10}{20 + 10} \text{ k}\Omega = 6.67 \text{ k}\Omega$$

Thus, the given circuit can be redrawn as



The base to emitter junction of the transistor is forward biased and hence it cannot be in cut off region.

Let us assume that the transistor is in active region and hence the following relation holds

$$i_c = \beta i_b$$

Applying KVL we can write

$$3.33 = 6.67i_b + 0.7 + 2(1 + \beta)i_b$$

Therefore, the base current,  $i_b$ , can be calculated as

$$i_b = \frac{3.33 - 0.7}{6.67 + 2(1 + \beta)} = 0.0126 \text{ mA}$$

Thus, the collector current,  $i_c$ , can now be calculated as

$$i_c = \beta i_b = 1.26 \text{ mA}$$

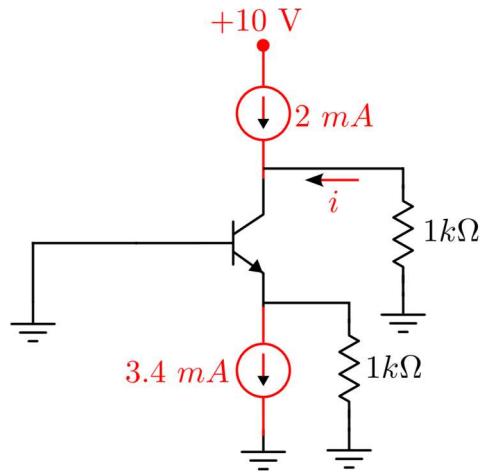
Thus, the collector to emitter voltage can be calculated as

$$V_{CE} = 10 - 8 \times 1.26 - 2 \times 101 \times 0.0126 = -2.62 \text{ V}$$

However,  $V_{CE}$  can not be negative and hence our assumption was incorrect. Thus, the transistor is in saturation mode.

*Question 8:*

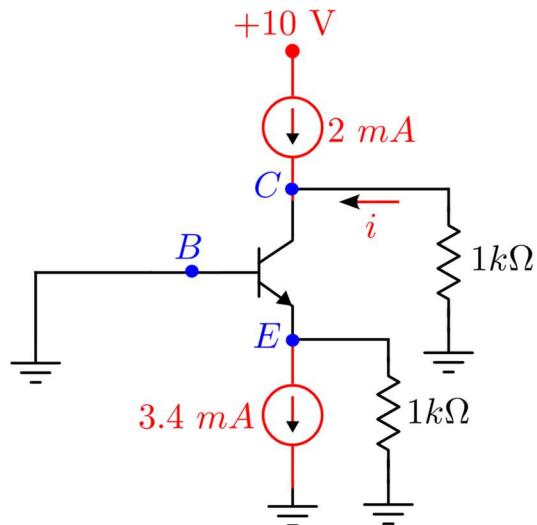
Assume that the transistor shown in the circuit below to be in saturation. Take  $[V_{BE}]_{sat} = 0.8 \text{ V}$ ,  $[V_{CE}]_{sat} = 0.2 \text{ V}$ , and  $\beta = 100$ . What will be the value of the current,  $i$ , in the circuit schematic.



- (a) -0.6 mA
- (b) 0.6 mA
- (c) -0.26 mA
- (d) 0.26 mA

Solution: Correct option is (b)

The base terminal of the BJT shown in the schematic is grounded.



Therefore, the potential at the base terminal,  $V_B = 0 \text{ V}$

As has been mentioned in the question the base to emitter voltage under saturation condition  $[V_{BE}]_{sat} = 0.8 \text{ V}$ . We can now calculate the potential at the emitter terminal,  $V_E$ , as

$$V_E = V_B - 0.8 = -0.8 \text{ V}$$

Again, the collector to emitter voltage under saturation condition is mentioned in the question as  $[V_{CE}]_{sat} = 0.2 \text{ V}$ . Therefore, the potential at the collector terminal can be calculated as

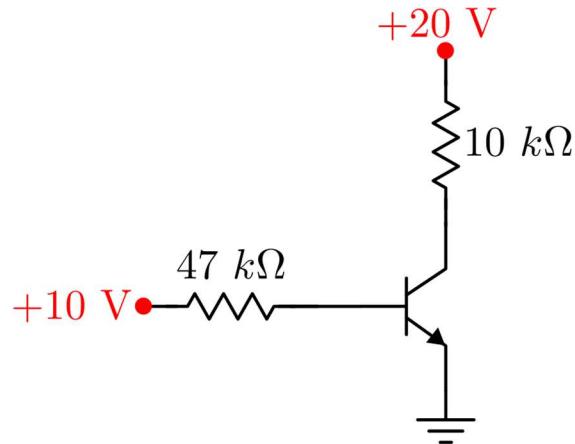
$$V_C = V_E + 0.2 = -0.6 \text{ V}$$

Thus, the value of the current  $i$  can be obtained as

$$i = \frac{-V_C}{1k} = 0.6 \text{ mA.}$$

*Question 9:*

*In the transistor circuit shown below the collector to ground voltage is +20 V. Which of the following is the probable cause of error?*

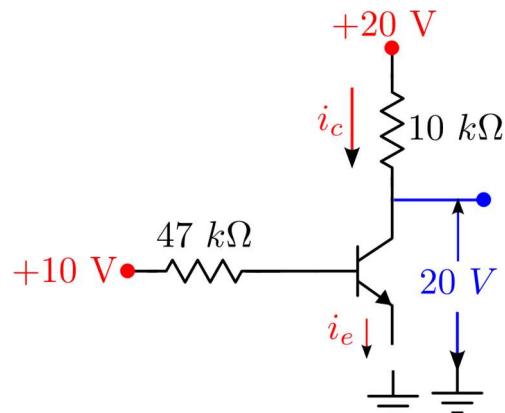


- (a) Collector-Emitter terminals are shorted
- (b) Emitter-ground connection is open
- (c) 10  $k\Omega$  resistor is open.
- (d) Collector- base terminals are shorted

**Solution:** Correct option is (b)

The collector – ground voltage is observed to be +20 V. That means there is no voltage drop across the  $10 \text{ k}\Omega$  resistor. That will essentially mean that

$$i_c \approx i_e = 0 \text{ A}$$



This can only happen if the emitter terminal is open.

*Question 10:*

*A bipolar junction transistor (BJT) is used as a power control switch by biasing it in the cut off region (OFF state) or in saturation region (ON state). In the ON state for the BJT which of the following statements is correct.*

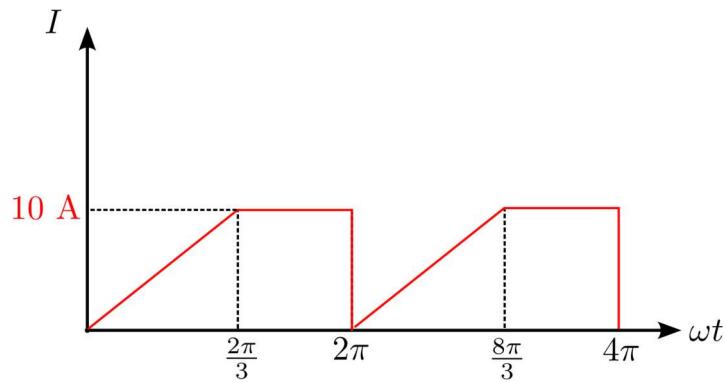
- (a) Both Base-Emitter and Base-Collector junctions are reverse biased
- (b) Base-Emitter junction is reverse biased and Base-Collector junction is forward biased
- (c) Base-Emitter junction is forward biased and Base-Collector junction is reverse biased
- (d) Both Base-Emitter and Base-Collector junctions are forward biased

Solution: **Correct option is (d)**

When BJT is in saturation, both the base-emitter and base-collector junctions will be in forward biased condition.

*Question 1:*

In a power electronic circuit MOSFET is using as a switch. MOSFET has a ON state resistance of  $R_{ds(on)} = 0.5 \Omega$ . What is the conduction loss in the device if the following current waveform is flowing through it during its ON state.



- (a) 35.26 W
- (b) 45.27 W
- (c) 38.89 W
- (d) None

Solution: Correct option is (c)

The mean square value of the current flowing through the MOSFET is given by:

$$I_{rms}^2 = \frac{1}{T} \left[ \int_0^{T/3} \frac{30^2}{T^2} t^2 dt + \int_{T/3}^T 100. dt \right] = 77.78 A^2$$

The conduction power loss is given by:

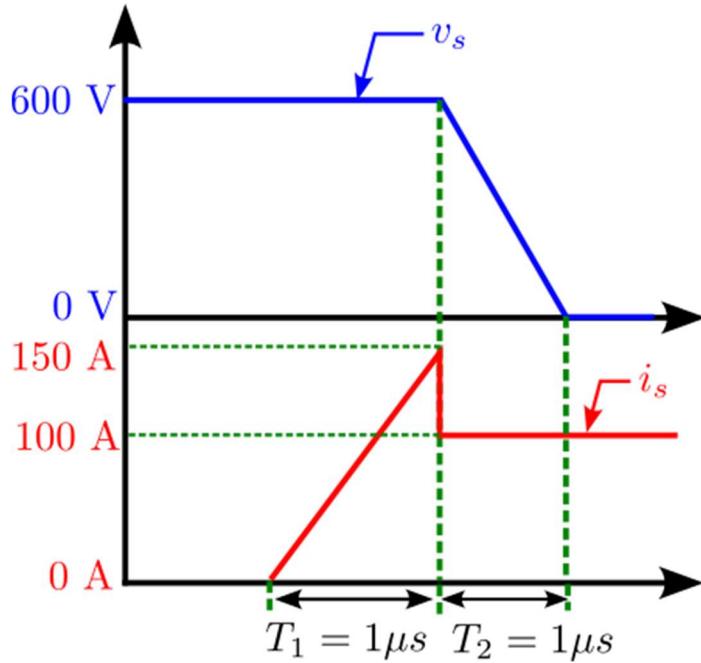
$$P_{cond} = I_{rms}^2 R_{on}$$

Where,  $R_{on}$  is the on-state resistance of the MOSFET. Thus, the conduction loss is:

$$P_{cond} = 77.78 \times 0.5 = 38.89 W$$

**Question 2: (Numerical Type)**

The voltage ( $v_s$ ) and current ( $i_s$ ) transition through a semiconductor switch during turn on transition are shown in the figure. The energy dissipated during the transition (in mJ) is \_\_\_\_\_.



Solution:

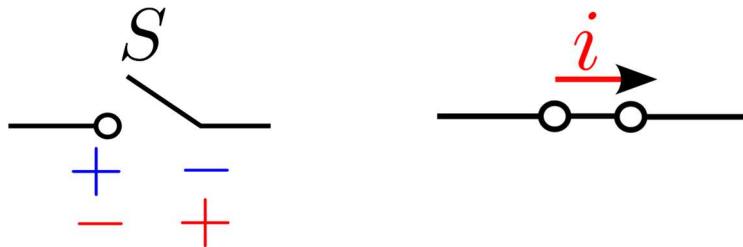
Answer range (74.9-75)

The energy dissipated during the switching transition can be written as

$$E_{sw} = \frac{1}{2} \times 150 \times 600 \times T_1 + \frac{1}{2} \times 100 \times 600 \times T_2 = 0.075 J = 75 \text{ mJ}$$

*Question 3:*

An electronic switch 'S' is required to block voltage of either polarity during its OFF state as shown in the figure 1(a). This switch is required to conduct in only one direction in its ON state as shown in the figure 1(b).



Which of the following are valid realization of the switch 'S'.



- (a) Only 1
- (b) 1 and 2
- (c) 1 and 3
- (d) 3 and 4

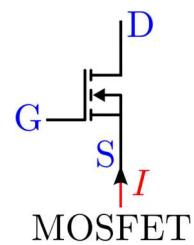
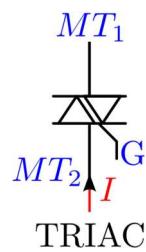
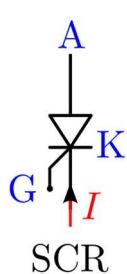
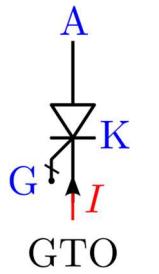
Solution: **Correct option is (c)**

Thyristor can block voltages of either polarity but can carry current only in forward direction.

Similarly, a diode in series with BJT can block voltages in either direction and can conduct current only in forward direction.

*Question 4:*

*Four power semiconductor devices are shown in the figure along with their relevant terminals. The device(s) that can carry dc current continuously in the direction shown when the gate signal is HIGH is (are)*



- (a) Triac only
- (b) Triac and MOSFET
- (c) Triac and GTO
- (d) SCR and Triac

Solution: **Correct option is (b)**

SCR and GTO allow conduction of current from anode to cathode. Hence current cannot flow in the given direction in GTO and SCR.

Triac and MOSFET can conduct current in both directions. Hence, current can flow in the given direction for both MOSFET and Triac.

**Question 5: Numerical type**

A steady dc current of 100 A is flowing through a power module (S, D) as shown in Fig. (a). The V-I characteristics of the IGBT (S) and the diode (D) are shown in Fig. (b) and (c), respectively. The conduction power loss in the power module (S, D) in watts, is \_\_\_\_\_.

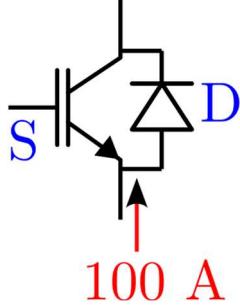


Fig. (a)

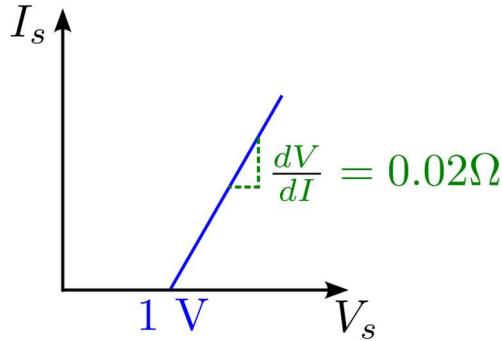


Fig. (b): VI Characteristic of IGBT

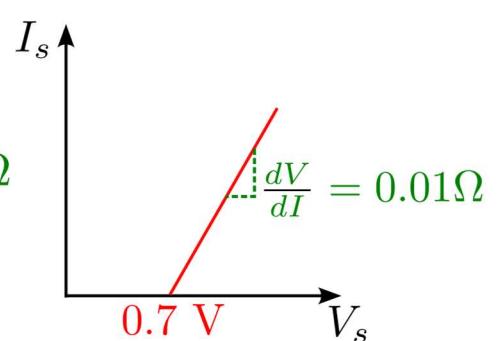


Fig. (c): VI Characteristic of Diode

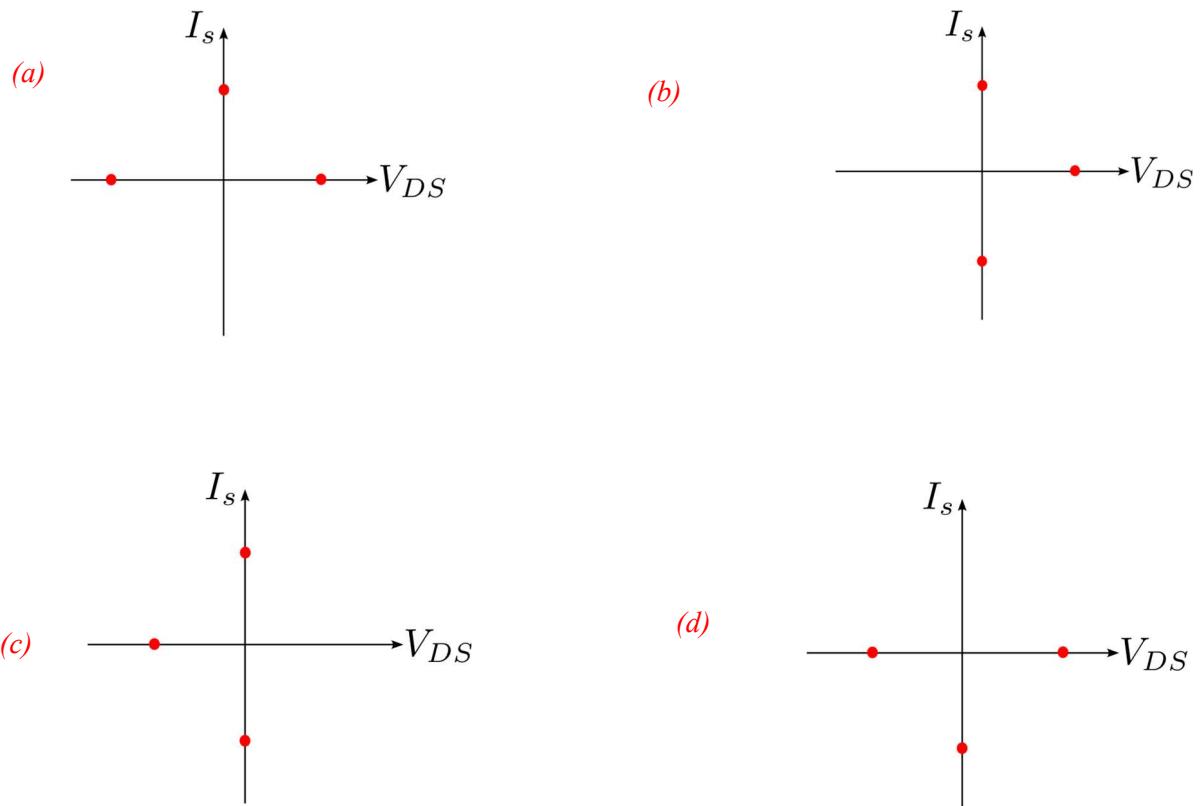
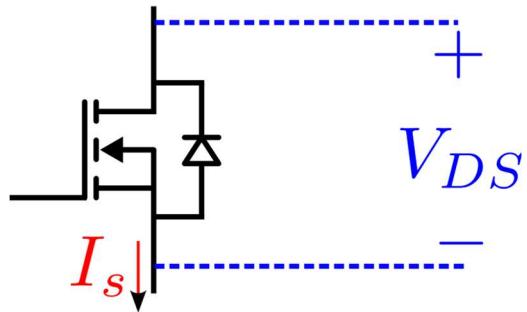
Solution: Answer range (169-171)

IGBT, denoted by 'S', will not allow the flow of the current in the direction as shown in Fig. a. Hence, only the diode will be conducting. As shown in Fig. (c), the forward voltage drop of the diode is 0.7 V and the on-state resistance is  $0.01\Omega$ . Thus, the conduction losses in the diode can be calculated as

$$P_{loss} = 0.7 \times 100 + 100^2 \times 0.01 = 170 \text{ W}$$

*Question 6:*

Figure shows a MOSFET with integral body diode. It is employed as a power switching device in the ON and OFF states through appropriate control. The ON-OFF states of the switch are given on the  $V_{DS}$  –  $I_s$  plane by



**Solution: Correct option is (b)**

MOSFET with body diode can carry current in either direction. However, MOSFET with body diode can only block voltages of positive polarity (i.e.  $V_{DS} > 0$ ). If  $V_{DS} < 0$ , the antiparallel diode will start conducting and hence the switching block cannot block voltage of opposite polarity.

*Question 7:*

*For the power semiconductor devices IGBT, MOSFET, Diode and Thyristor, which of the following statements is true?*

- (a) All four are majority carrier devices.
- (b) All four are minority carrier devices.
- (c) IGBT and MOSFET are majority carrier devices, whereas Diode and Thyristor are minority carrier devices.
- (d) MOSFET is majority carrier device, whereas IGBT, Thyristor and Diode are minority carrier device.

**Solution:** Correct option is (d)

Only MOSFET is a majority carrier device whereas all others are minority carrier devices.

*Question 8:*

*The conduction loss versus device current characteristic of a power MOSFET is best approximated by:*

- (a) Parabola
- (b) Straight line
- (c) Rectangular hyperbola
- (d) Exponentially decaying function

Solution: Correct option is (a)

Conduction power loss of a MOSFET can be calculated as

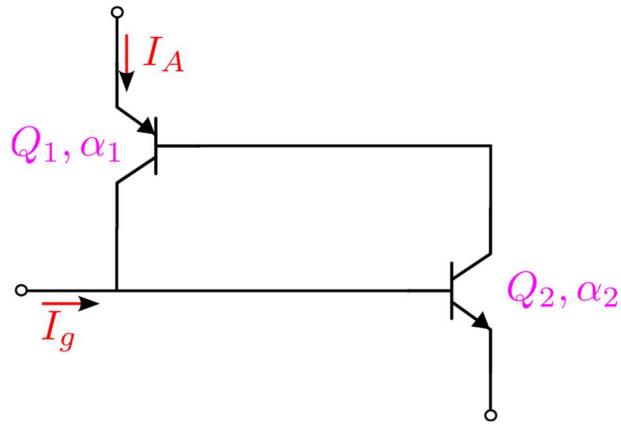
$$P_{loss} = R_{DS(on)} I_{rms}^2$$

The above equation can be compared with the equation of the parabola as given below.

$$y = a x^2$$

Question 9:

In the figure,  $Q_1$  and  $Q_2$  have common collector current gain values of  $\alpha_1$  and  $\alpha_2$  respectively. (collector - emitter current gain of BJT). Find the expression for  $I_A$ .



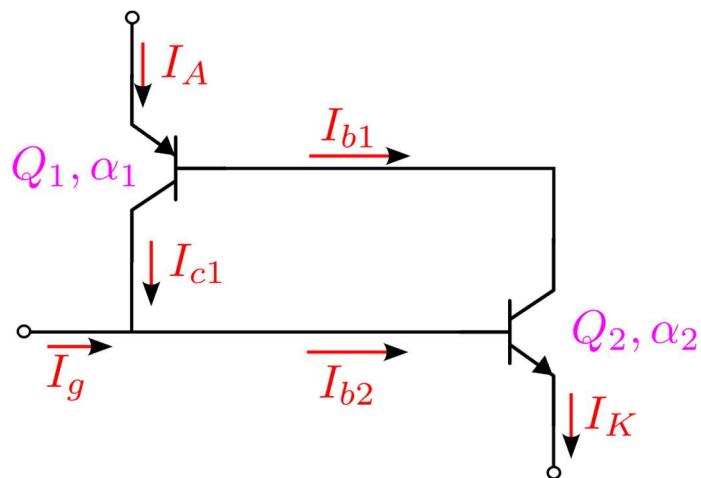
$$(a) \frac{\alpha_2 I_g}{1 - \alpha_1 - \alpha_2}$$

$$(b) \frac{(\alpha_1 + \alpha_2) I_g}{\alpha_2}$$

$$(c) \frac{\alpha_2 I_g}{1 + \alpha_1 + \alpha_2}$$

$$(d) \frac{\alpha_1 I_g}{1 - \alpha_1 - \alpha_2}$$

Solution: Correct option is (a)



$$I_{c1} = \alpha_1 I_A$$

$$I_{b1} = \alpha_2 I_K$$

Applying KCL we also have,

$$I_A = I_{c1} + I_{b1} = \alpha_1 I_A + \alpha_2 I_K$$

Again, we also have

$$I_K = I_{b2} + I_{b1} = I_{b2} + \alpha_2 I_K$$

Therefore, we have

$$I_K = \frac{I_{b2}}{1 - \alpha_2}$$

Again, applying KCL we have

$$I_{b2} = I_{c1} + I_g = \alpha_1 I_A + I_g$$

Thus, the expression for  $I_K$  can now be written as

$$I_K = \frac{\alpha_1 I_A + I_g}{1 - \alpha_2}$$

Therefore, we have

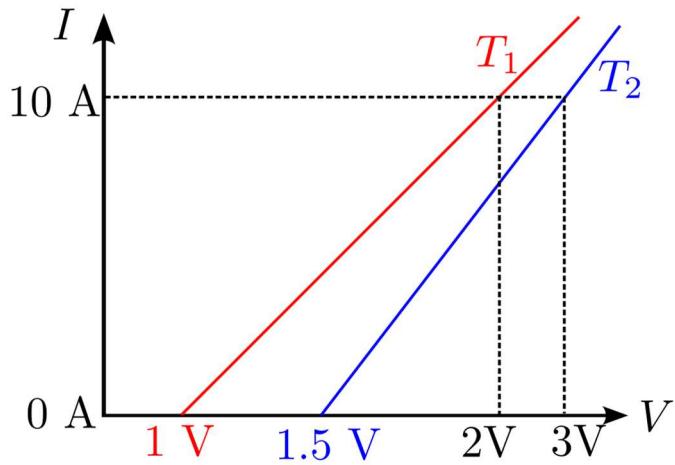
$$I_A = \alpha_1 I_A + \alpha_2 \frac{\alpha_1 I_A + I_g}{1 - \alpha_2}$$

Re-arranging the equation, we get,

$$I_A = \frac{\alpha_2 I_g}{1 - \alpha_1 - \alpha_2}$$

*Question 10:*

*Two thyristors  $T_1$  and  $T_2$  are being operated in parallel. Their V-I characteristic when they are ON are given in figure. The common voltage across the thyristors is 1.8 V. Power loss in  $T_1$  and  $T_2$  respectively are (in watts):*



- (a) 8, 2
- (b) 64, 4
- (c) 20, 30
- (d) 14.4, 3.6

Solution: Correct option is (d)

The equation for VI characteristic for  $T_1$  can be written as

$$I_1 = 10V_1 - 10$$

The equation for VI characteristic for  $T_2$  can be written as

$$I_2 = \frac{20}{3}V_2 - 10$$

As the voltage across the thyristors in parallel is 1.8 V we can find the current flowing through each thyristor from the above equations putting  $V_1 = V_2 = 1.8 V$

From the above equations we get

$$I_1 = 8 A \quad \text{and} \quad I_2 = 2 A$$

Thus,

power loss in  $T_1 = 8 \times 1.8 = 14.4 \text{ Watts}$

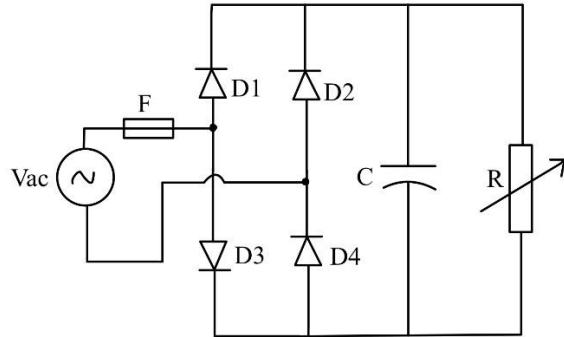
And

power loss in  $T_2 = 2 \times 1.8 = 3.6 \text{ Watts}$

**Question 1:**

While connecting the diodes of a full bridge rectifier, the Power electronics engineer made a mistake and connected one of the diodes with wrong polarity as shown in the figure below. The circuit was then connected to 230V AC supply, through a semiconductor fuse. Which of the following statements are FALSE?

(Assume the forward drop of diode is 0 V)



1. Circuit will work properly during positive half cycle and no current will flow during negative half cycle.
  2. The Semiconductor fuse used in the circuit would blow up immediately.
  3. The capacitor will blow up if fuse is not used.
  4. The load resistor will blow up if fuse is not used.
  5. Diode D1 and D4 will be damaged if fuse is not used.
  6. Diode D2 will not be damaged.
  7. Diode D3 and D4 will be damaged if fuse is not used.
- a) 1,3,4,6  
b) 2,3,5,6  
c) 1,3,4,5  
d) 1,2,6,7

Solution: Correct option is (c)

Due to the wrong connection made, during positive half cycle, D3 and D4 will be forward biased and thus the AC supply is shorted and huge currents will flow and the semiconductor fuse will blow up. Semiconductor fuses are extremely fast and can act in few milliseconds or even less than a millisecond. So, if the fuse is used, the diodes D3 and D4 will be protected. Otherwise, they will blow up. In the negative half cycle, there is no path for current to flow. Hence D2, Output Capacitor C and Load Resistor R will not blow up whether fuse is used or not.

D1 is forward biased during positive half cycle, but no current will flow through D1 and through  $R \parallel C$ , because the supply has a dead short through D3 and D4 and all the currents will flow through D3 and D4. Therefore, D1 will not be damaged.

**Question 2:**

In a particular rectifier circuit, the AC supply (230V, 50Hz) is turned ON exactly at the zero crossing (using a Zero Crossing Detection Circuit). Based on the load conditions, the Power Electronics Engineer calculated the amplitude of the inrush current during the first cycle when the supply is turned ON. The amplitude came out to be 75A. Also, his circuit will be operating in an ambient temperature of 37.5°C. The engineer checks through the datasheet of IN4007 to see whether it can handle 75A of surge current at the starting. He finds out that the maximum tolerable surge current of IN4007 diode at 37.5°C is \_\_\_\_\_.

(The datasheet is attached. The student is advised to go through the data sheet thoroughly and find the value of surge current. Assume for simplicity that the inrush current pulse is square pulse)

(<https://www.vishay.com/docs/88503/ln4001.pdf>)

**Solution: Range (28-30)**

Since the source is turned at zero crossing, for the source to reach the peak, it will take 5ms for the source to reach the peak value. So, the inrush current pulse will flow for 5ms. Even though it is not exactly a square, as allowed in the question, we will take it as a square.

This inrush current happens only in the first cycle when the supply is turned ON. It doesn't repeat for the consecutive cycles and therefore we have to look at the **non-repetitive peak forward surge current** value mentioned in the datasheet. Looking at the tables, we get

MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	SYMBOL	IN4001	IN4002	IN4003	IN4004	IN4005	IN4006
Maximum repetitive peak reverse voltage	$V_{RRM}$	50	100	200	400	600	800
Maximum RMS voltage	$V_{RMS}$	35	70	140	280	420	560
Maximum DC blocking voltage	$V_{DC}$	50	100	200	400	600	800
Maximum average forward rectified current 0.375" (9.5 mm) lead length at $T_A = 75^\circ\text{C}$	$I_{F(AV)}$				1.0		A
Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load	$I_{FSM}$				30		A
Non-repetitive peak forward surge current square waveform $T_A = 25^\circ\text{C}$ (fig. 3) $t_p = 5\text{ ms}$	$I_{FSM}$			45			A
				35			
				30			
Maximum full load reverse current, full cycle average 0.375" (9.5 mm) lead length $T_L = 75^\circ\text{C}$	$I_{R(AV)}$			30		$\mu\text{A}$	
Rating for fusing ( $t < 8.3\text{ ms}$ )	$i_{FT}(t)$			3.7		$\text{A}^2\text{s}$	
Operating junction and storage temperature range	$T_J, T_{STG}$			-50 to +150			$^\circ\text{C}$

The tables provide the value at  $25^\circ\text{C}$ . In order to get the exact value at  $37.5^\circ\text{C}$ , we need to look at the characteristics. We can see from the characteristics, that the value of surge current is nearly 29 A at  $37.5^\circ\text{C}$  (marked in RED).

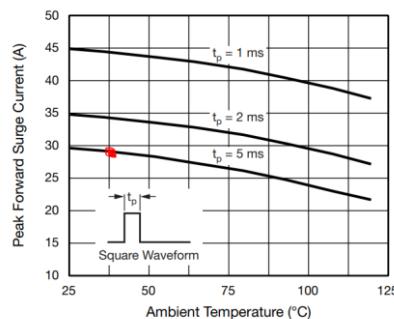
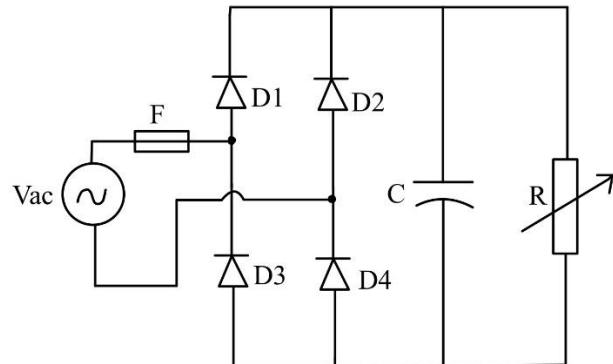


Fig. 3 - Non-Repetitive Peak Forward Surge Current

**Question 3:**

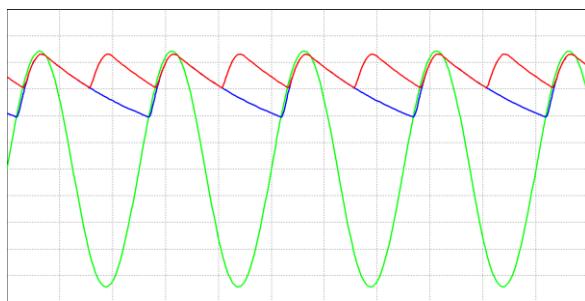
In the diode bridge rectifier circuit given below, which of the following statements are true, if diode D2 is damaged and acts as OPEN for the entire time of operation.



1. The Capacitor voltage ripple for a given load current will be lesser than the circuit in which D2 is working properly.
  2. If the load current is extremely small, the output voltage will appear to be approximately the same whether D2 is working properly or not.
  3. If the load current is very large, the output voltage can also come down to zero, before the positive half of the next cycle.
- a) 1,2,3  
b) 2,3  
c) 1,3  
d) None are correct

**Solution: (b)**

When D2 is open, no current will flow during the negative half cycle and therefore the capacitor will discharge for a longer time and thus the capacitor voltage ripple will be larger.



The green waveform is the input voltage. The red waveform is the output voltage when D2 is working properly. The blue waveform is the output voltage when D2 is OPEN.

When the load current is very large, the capacitor will discharge quickly and be at 0V.

When the load current is very small, the capacitor will discharge very slowly and thus the output voltage ripple will be less and the voltage waveform will look alike in both the cases.

*Question 4:*

*While selecting the capacitor for the diode full bridge rectifier, the Power Electronics Engineer must look into several parameters to decide the capacitor and one of them is the **maximum voltage across the capacitor**. The engineer must design this rectifier for a particular country where the standard AC voltage is 110Vrms ,60Hz. There can be a fluctuation of 40% around the standard value. Considering the fluctuation in supply voltage, and giving a margin of 20% on top of the fluctuations, what is the nearest voltage rating of the capacitor that the engineer arrives at:*

- a) 218 V
- b) 154 V
- c) 282V
- d) 262 V

**Solution: (D)**

$$\text{Standard average RMS voltage} = 110 \text{ Vrms}$$

$$\text{Maximum RMS voltage of the supply} = 110 + 110 \times \frac{40}{100} = 154 \text{ Vrms}$$

$$\text{The peak voltage for the maximum condition} = \text{Vrms} \times \sqrt{2} = 154 \times 1.414 = 217.756 \text{ V}$$

$$\text{Adding 20\% margin to this we get } V_m = 217.756 \times 1.2 = 261.307 \approx 262 \text{ V}$$

The engineer will obviously not find a capacitor of this exact voltage rating, but he must choose a voltage rating for the capacitor very near to 262 V that is available in the market.

**Question 5:**

For a particular application, after the circuit designer did all the necessary circuit analysis he came up with the following values for the capacitor

$$C = 215 \mu F ; V_c = 320V ; I_{CRMS} = 1.5A$$

A datasheet of a series of capacitors were handed to him. All the capacitors in this datasheet are rated at 500V. So the voltage aspect is taken care of. **He has to make sure that at all times, the capacitance should be 215uF.** The designer goes through the datasheet and write the code for the capacitor that he will choose finally is \_\_\_\_\_.

(The datasheet of the Electrolytic capacitor is attached. The student is advised to go through the datasheet thoroughly and find the code of the capacitor required for the above application.

( [https://www.nichicon.co.jp/english/series\\_items/catalog\\_pdf/e-lgc.pdf](https://www.nichicon.co.jp/english/series_items/catalog_pdf/e-lgc.pdf) )

Solution: LGC2H271MELA50

Voltage is 500V for all the capacitors. Therefore, we need not worry about voltage as it is way beyond 320V.

Now the capacitance designed is 215uF. We will be tempted to choose from the 220uF category. But the datasheet states that the capacitance has a tolerance of 20%.

Capacitance Tolerance	$\pm 20\%$ at 120Hz, 20°C
-----------------------	---------------------------

This implies that in the worst-case scenario, the capacitance will be

$$220 - 220 * \frac{20}{100} = 176 \mu F$$

Therefore, the designer will choose the 270uF category. Considering the tolerance, the minimum capacitance will be:

$$270 - 270 * \frac{20}{100} = 216 \mu F$$

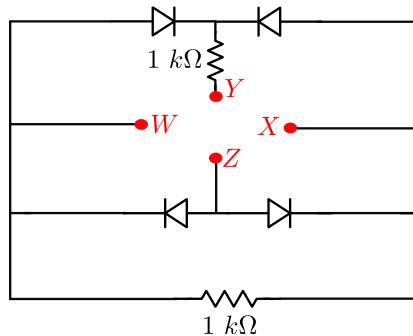
Now within this section, there are 4 available capacitors, and they differ mainly in the maximum RMS value permissible.

270	22 x 60	1620	1.10	LGC2H271MELZ60
	25 x 50	1600	1.10	LGC2H271MELA50
	30 x 35	1480	1.10	LGC2H271MELB35
	35 x 30	1430	1.10	LGC2H271MELC30

For our application, the maximum RMS value is 1.5 A. Therefore, the designer will choose the capacitor with rms current higher than that which is 1.6 A which corresponds to LGC2H271MELA50.

*Question 6:*

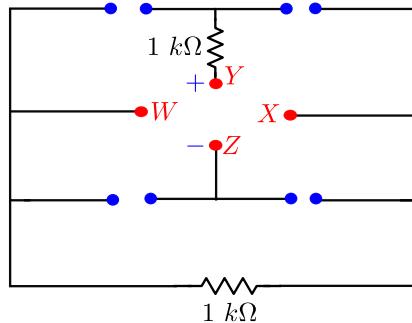
A voltage  $100 \sin(\omega t)$  is applied across  $YZ$ . Assuming diodes to be ideal, the voltages measured across  $WX$  (in volts) is



- (a)  $\sin(\omega t)$
- (b)  $(\sin(\omega t) + |\sin(\omega t)|)/2$
- (c)  $(\sin(\omega t) - |\sin(\omega t)|)/2$
- (d) 0 for all  $t$

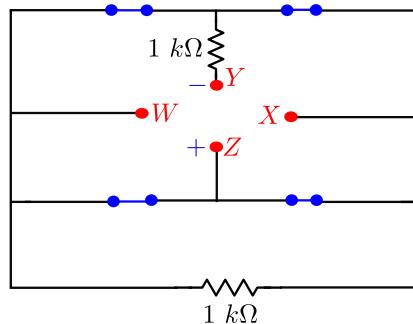
**Solution:** Correct option is (d)

During the positive half cycle the circuit becomes:



Thus, the voltage across ‘ $WX$ ’ during the positive half cycle is 0 V.

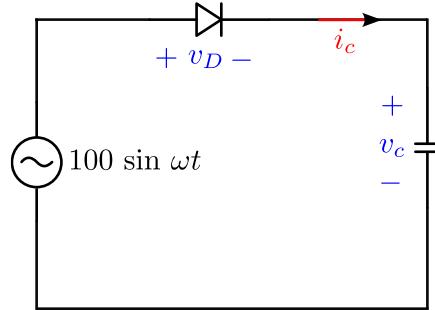
During the negative half cycle the circuit becomes:



Thus, the voltage across ‘ $WX$ ’ during the negative half cycle is 0 V.

**Question 7: Numerical type**

In the circuit shown below find the rms value of the voltage (in volts) across the diode in steady state.



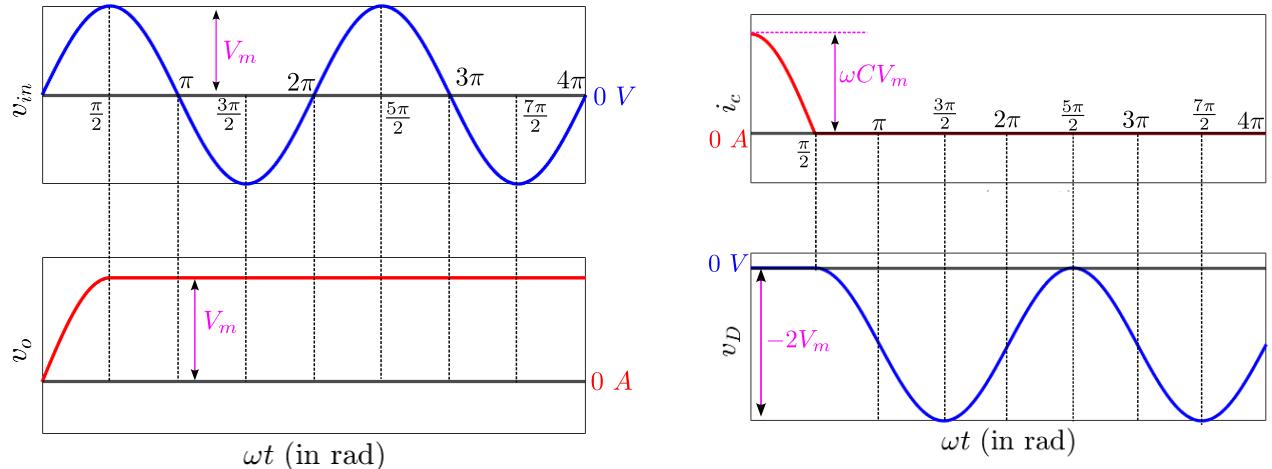
Solution: Answer range (121-123)

In the positive half cycle, the diode gets forward biased and starts conducting for the period

$$0 \leq \omega t \leq \frac{\pi}{2}. \text{ Thus, during this period}$$

$$v_c = 100 \sin(\omega t)$$

At  $\omega t = \frac{\pi}{2}$ , the voltage across the capacitors reaches its maximum value  $V_m = 100 V$ . Thus, the diode gets reverse biased for  $\omega t > \frac{\pi}{2}$  and the current through the diode,  $i_c$  stays put at 0 A. The corresponding waveforms are illustrated in the figures below:



Therefore, at steady state i.e. for  $\omega t > \frac{\pi}{2}$ , the expression for the diode voltage can be written as

$$v_D = V_m(\sin(\omega t) - 1)$$

Thus, from the expression we can conclude that the average value of the  $v_D$  is

$$V_{D,\text{avg}} = \langle v_D \rangle_T = \frac{V_m}{2\pi} \int_0^{2\pi} (\sin(\omega t) - 1) d(\omega t) = V_m$$

Rms value of the fundamental component of  $v_D$  is

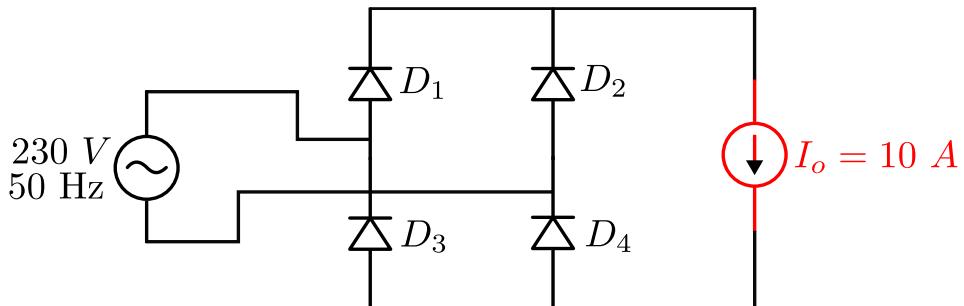
$$V_{1,rms} = \frac{V_m}{\sqrt{2}}$$

The rms value of the voltage across diode is thus given by

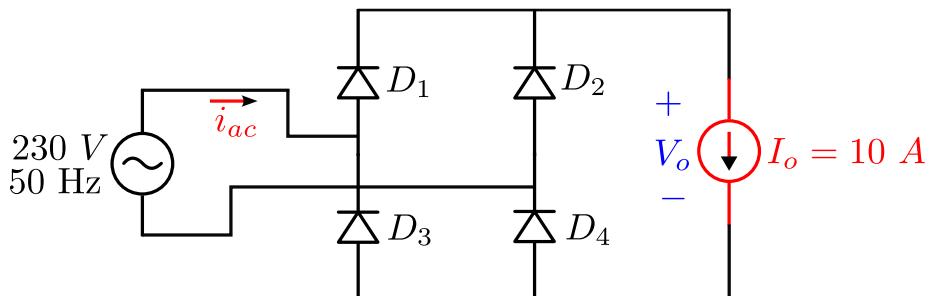
$$V_{D,rms} = \sqrt{V_{D,avg}^2 + V_{1,rms}^2} = \sqrt{\frac{3}{2}} V_m = 122.47 V$$

Question 8:

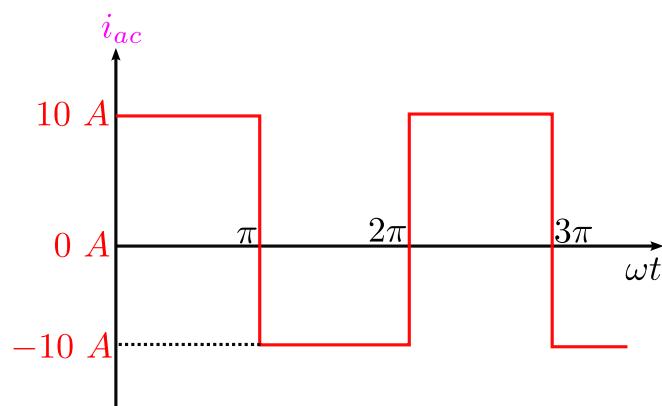
The figure shows the circuit of a rectifier fed from a 230 V (rms), 50 Hz sinusoidal voltage source. If we want to replace the current source with a resistor so that the rms value of the current supplied by the voltage source remains unchanged, the value of resistance (in  $\Omega$ ) is \_\_\_\_\_ (Assume diodes to be ideal).



Solution: Answer range (22.99-23)



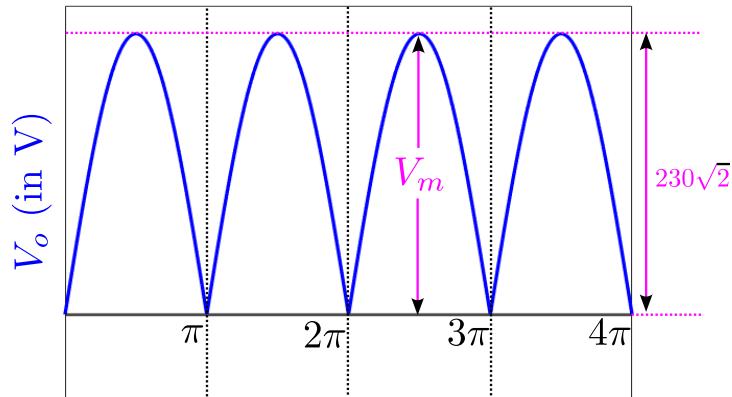
With the current source in the circuit, the waveform of  $i_{ac}$  is illustrated in the figure below



Thus, the rms value of the current,  $i_{ac}$ , supplied by the voltage source is

$$i_{ac,rms} = 10 \text{ A}$$

The waveform of the output voltage,  $V_o$ , is illustrated in the figure below



The rms value of the output voltage,  $V_o$ , is given by

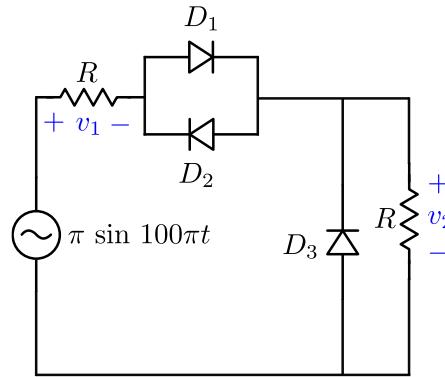
$$V_{o,rms} = \frac{V_m}{\sqrt{2}} = 230 \text{ V}$$

Now, if we want to replace the current source with a resistive load such that the rms current remains same as  $i_{ac,rms}$ , then the value of the resistive load can be obtained as

$$R_L = \frac{V_{o,rms}}{i_{ac,rms}} = 23 \Omega$$

*Question 9:*

For the circuit shown below assume the diodes  $D_1$ ,  $D_2$  and  $D_3$  to be ideal.



The dc components of voltages  $v_1$ , and  $v_2$  respectively are

- (a) 0 V and 1 V
- (b) -0.5 V and 0.5 V
- (c) 1 V and 0.5 V
- (d) 1 V and 1 V

Solution: **Correct option is (b)**

During the positive half cycle,  $D_1$  is forward biased and  $D_2$  and  $D_3$  are reverse biased. Thus, during this period

$$v_1 = v_2 = \frac{\pi}{2} \sin(100\pi t)$$

During the negative half cycle,  $D_1$  is reverse biased and  $D_2$  and  $D_3$  are forward biased. Thus, during this period

$$v_1 = \pi \sin(100\pi t) \quad \text{and} \quad v_2 = 0 \text{ V}$$

Now, we can calculate the average value of  $v_1$  as

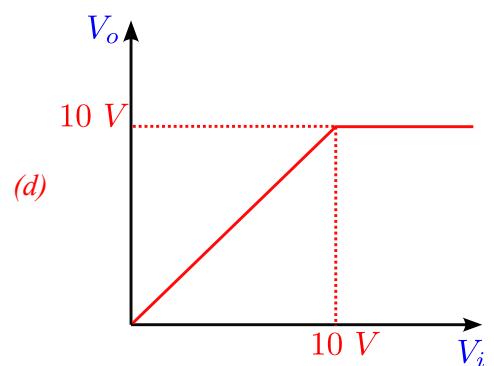
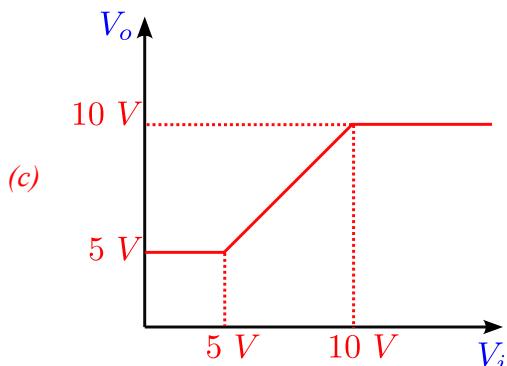
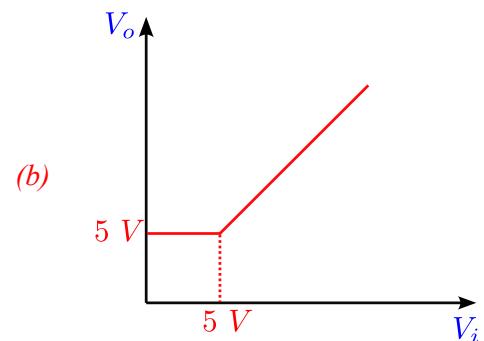
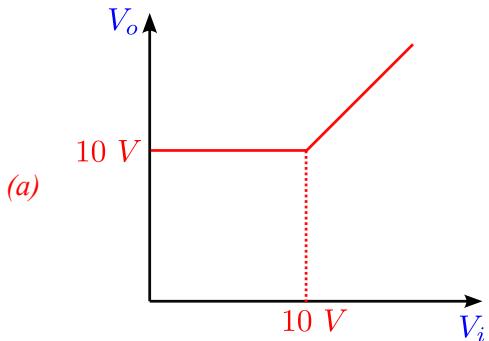
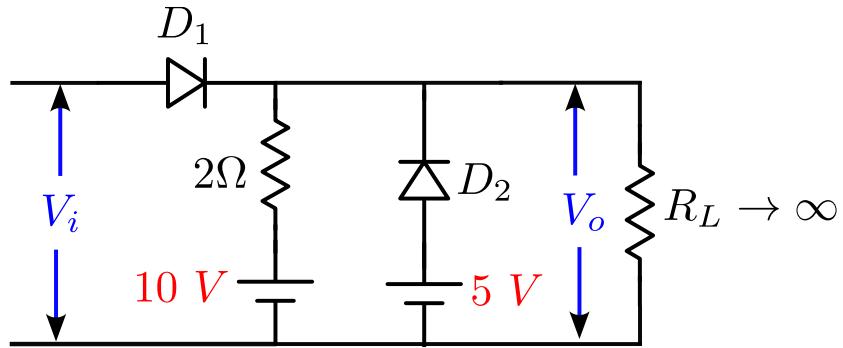
$$\langle v_1 \rangle_T = \frac{1}{2\pi} \left[ \int_0^{\pi} \frac{\pi}{2} \sin(\omega t) d(\omega t) + \int_{\pi}^{2\pi} \pi \sin(\omega t) d(\omega t) \right] = -\frac{1}{2}$$

Similarly, we can calculate the average value of  $v_2$  as

$$\langle v_2 \rangle_T = \frac{1}{2\pi} \left[ \int_0^{\pi} \frac{\pi}{2} \sin(\omega t) d(\omega t) \right] = \frac{1}{2}$$

*Question 10:*

*Assuming the diodes to be ideal, the transfer characteristics of the circuit will be*



Solution: Correct option is (a)

The output voltage  $V_o$  becomes equal to  $V_i$  only when  $V_i > 10\text{ V}$ . Else,  $V_o = 10\text{ V}$ , as there is no path for the current to flow and hence no voltage drop across  $2\Omega$  resistor.

**Question 1: Numerical type**

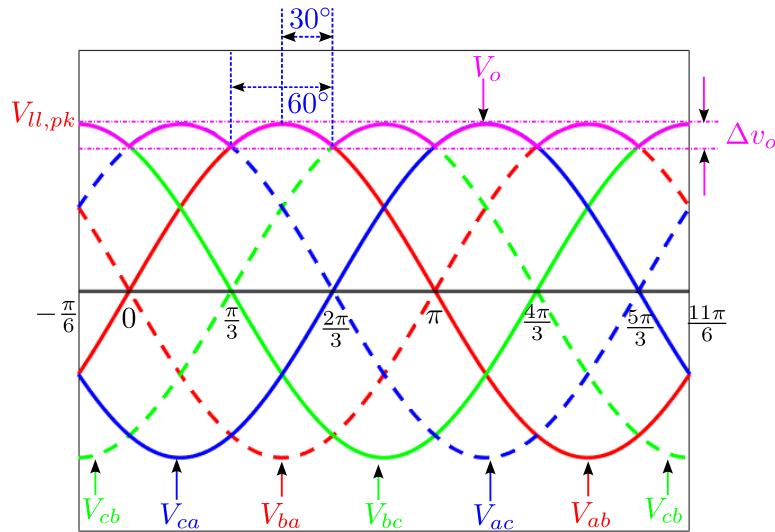
A three-phase bridge rectifier is supplied by 400V (line-line rms), 50Hz, three phase grid. The full bridge rectifier is connected to a resistive load of 1000Watt. If the maximum output voltage ripple requirement is 15% of the peak line-to-line input voltage, what is the minimum possible capacitor (in  $\mu F$ ) \_\_\_\_\_.

Solution: Answer range (0-0)

The peak value of line-to-line input voltage ( $V_{ll,pk}$ ) =  $400\sqrt{2} V$

Therefore, the permissible value of the output ripple is  $= 0.15 \times V_{ll,pk} = 84.85 V$

Let us now calculate the ripple voltage of the output of the three-phase rectifier under consideration. The waveforms of the line-to-line voltages and the corresponding output voltage ( $V_o$ ) of a rectifier are shown in the figure below:



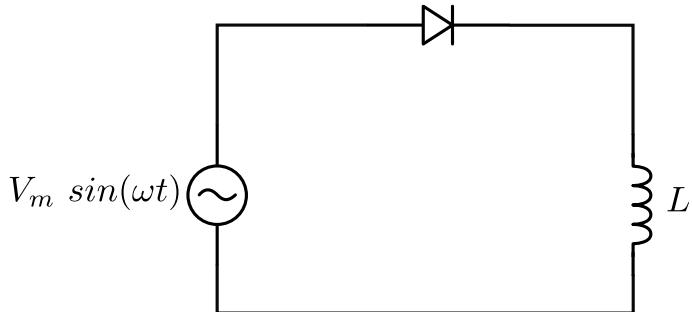
The ripple in the output voltage of the rectifier can be calculated as follows:

$$\Delta v_o = V_{ll,pk} - V_{ll,pk} \cos 30^\circ = 400\sqrt{2} \left(1 - \frac{\sqrt{3}}{2}\right) = 75.78 V$$

As the ripple of the output voltage,  $\Delta v_o$ , is itself lower than the permissible value of the ripple voltage, therefore there is no requirement of extra capacitor filter.

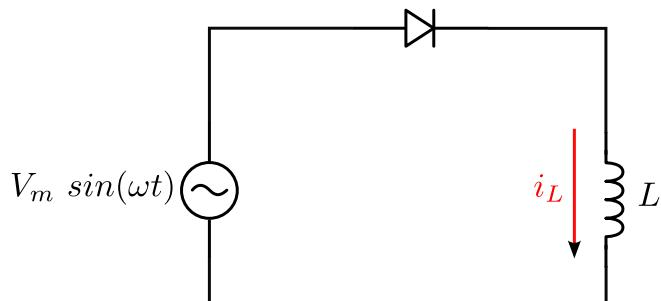
*Question 2:*

In the circuit shown below an ideal diode connects the ac source with a pure inductance L. The circuit is initially relaxed. The diode conducts for



- (a)  $90^\circ$
- (b)  $180^\circ$
- (c)  $270^\circ$
- (d)  $360^\circ$

Solution: Correct option is (d)



The expression for the inductor current is given by

$$i_L(t) = \frac{1}{L} \int V_m \sin \omega t \, dt = -\frac{V_m}{L} \cos \omega t + K$$

Where  $K$  is the integral constant.

To obtain the value of  $K$  we need to apply the initial conditions. We know that the circuit was initially relaxed. Thus, we can write

$$i_L(t = 0) = 0 = -\frac{V_m}{L} + K$$

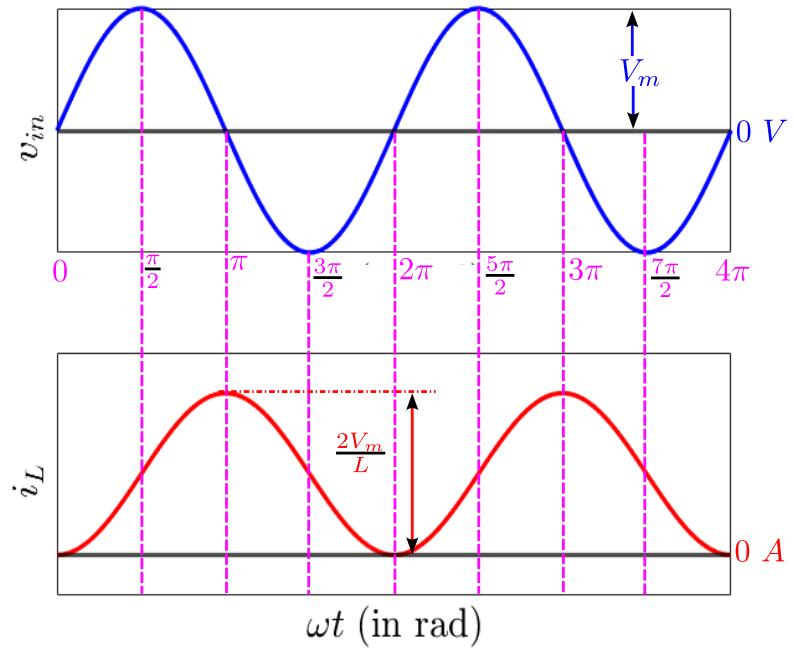
Thus, the value of  $K$  can be obtained as

$$K = \frac{V_m}{L}$$

The equation of the inductor current can therefore be written as:

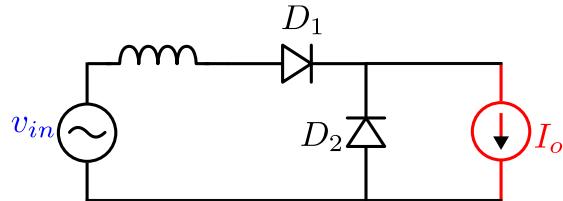
$$i_L(t) = \frac{V_m}{L} (1 - \cos \omega t)$$

For any value of 't', the above expression is always positive and hence the diode will always conduct as it is never reverse biased. The waveform of the inductor current,  $i_L(t)$ , is shown in the figure below.



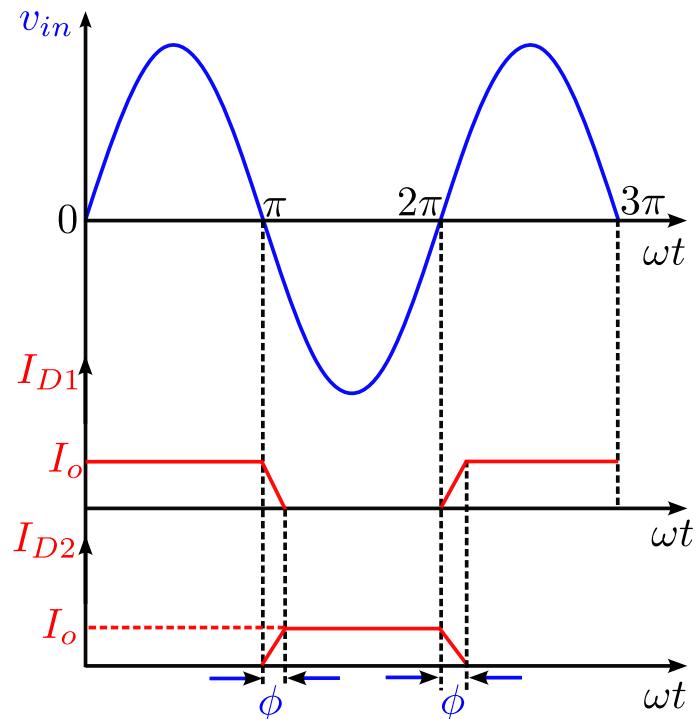
**Question 3:**

In the circuit shown below, the diodes are ideal, the inductance is small, and  $I_o \neq 0$ . Which of the following statements is true.



- (a)  $D_1$  conducts for greater than  $180^\circ$  and  $D_2$  conducts for greater than  $180^\circ$
- (b)  $D_2$  conducts for greater than  $180^\circ$  and  $D_1$  conducts for  $180^\circ$
- (c)  $D_1$  conducts for  $180^\circ$  and  $D_2$  conducts for  $180^\circ$
- (d)  $D_1$  conducts for greater than  $180^\circ$  and  $D_2$  conducts for  $180^\circ$

Solution: Correct option is (a)



The diode  $D_1$  does not get reverse biased immediately when  $v_{in}$  becomes negative because of the energy stored in the source inductance. Thus, the current  $I_{D1}$  flowing through  $D_1$  gradually goes to zero as shown in the figure above. However, the load demands a constant current  $I_o$ . To maintain the load current at  $I_o$ ,  $D_2$  starts conducting at  $\omega t = \pi$ . At  $\omega t = \pi + \Phi$ , the current  $I_{D1}$  goes to zero and  $I_{D2}$ , flowing through the diode  $D_2$ , free wheels and carries the current  $I_o$ .

From the figure it is evident that option (a) is correct.

**Question 4: Numerical type**

The input voltage of a converter is:

$$V_{in} = 100\sqrt{2} \sin(100\pi t) V$$

The current drawn by the converter is:

$$i_{in} = 10\sqrt{2} \sin(100\pi t - \frac{\pi}{3}) + 5\sqrt{2} \sin(300\pi t + \frac{\pi}{4}) + 2\sqrt{2} \sin(500\pi t - \frac{\pi}{6}) A$$

The input power factor of the converter is \_\_\_\_\_.

Solution: Answer range (0.4 - 0.47)

The active power consumed can be calculated as

$$P = \frac{100\sqrt{2} \times 10\sqrt{2}}{2} \cos \frac{\pi}{3} = 500 W$$

The rms value of the current drawn by the converter can be calculated as

$$i_{rms} = \sqrt{10^2 + 5^2 + 2^2} = 11.35$$

Total input VA can be calculated as

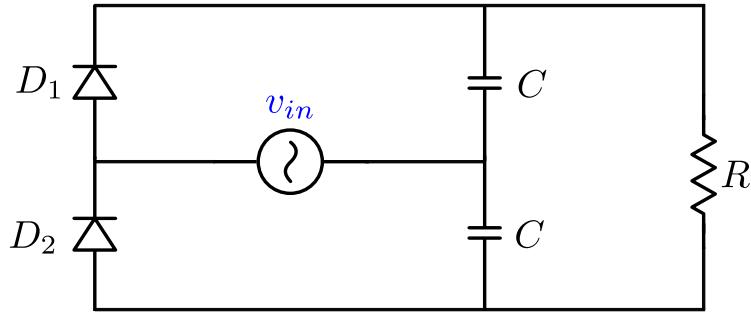
$$VA_{in} = i_{rms} \times v_{in,rms} = 11.3578 \times 100 = 1135.78$$

Power factor of the converter can then be calculated as

$$p.f. = \frac{P}{VA_{in}} = \frac{500}{1135.78} = 0.44$$

**Question 5:**

In the circuit given below, the input voltage  $v_{in} = 100 \sin(100\pi t)$ . For  $100\pi RC = 50$ , the average voltage across  $R$  (in volts) under steady state is nearest to



- (a) 100
- (b) 31.8
- (c) 63.6
- (d) 200

Solution: Correct option is (d)

The time constant of the circuit can be calculated as

$$RC = \frac{50}{100\pi} \approx 0.16 \text{ s}$$

As the frequency of the source voltage,  $v_{in}(t)$ , is 50 Hz, the frequency of the fully rectified sine wave would be 100 Hz. Thus, the time period of the fully rectified sine wave is 0.01 s. The time constant is exceeding the time period by more than a factor of 10. Thus, we can assume that the load resistance,  $R$ , is large enough to maintain the voltage across the capacitors. We can now redraw the circuit as shown below:

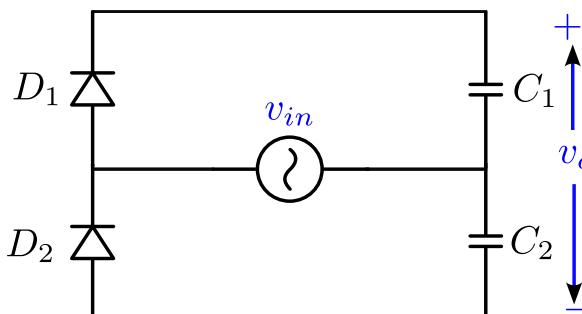


Fig. (a)

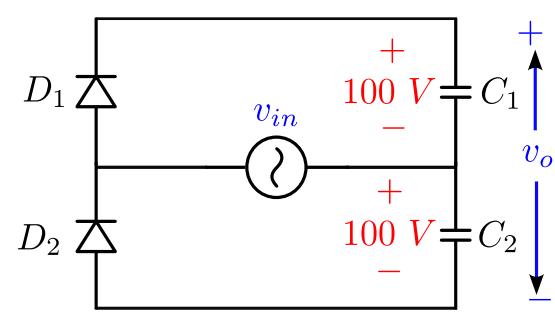


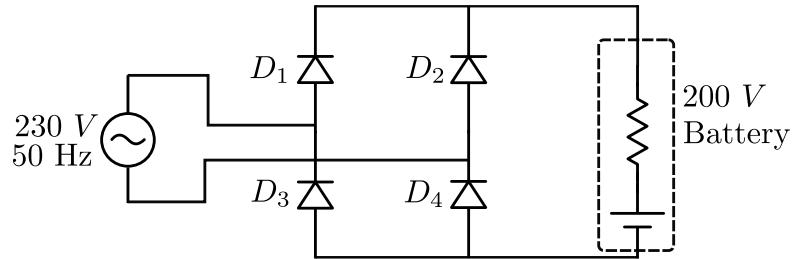
Fig. (b)

During the positive half cycle  $D_1$  will be conducting till the voltage across the capacitor,  $C_1$ , reaches the peak value of the input voltage  $v_{in}$  after which the diode  $D_1$  gets reverse biased.

In the negative half cycle  $D_2$  will be conducting till the voltage across the capacitor,  $C_2$ , reaches the peak value of the input voltage  $v_{in}$  after which the diode  $D_2$  gets reverse biased. Thus, at steady state the voltage across the capacitors will be as shown in the Fig. (b).

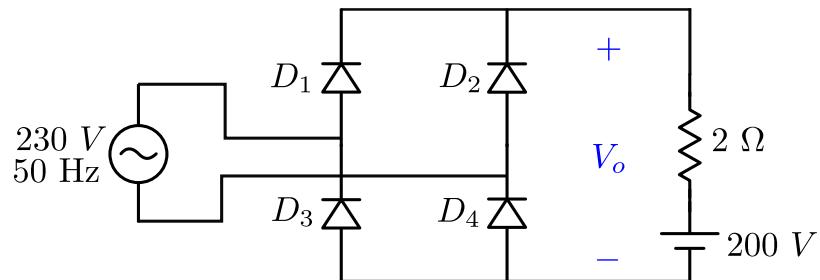
*Question 6:*

A single-phase full bridge rectifier is used to charge a battery of 200 V having an internal resistance of  $2\Omega$ . If the diode  $D_2$  gets open circuited due to some fault, what would be the average charging current?

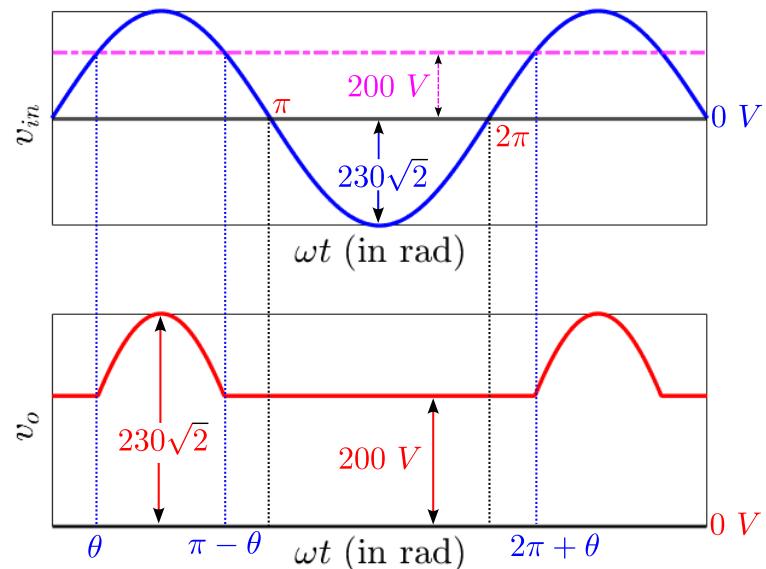


- (a) 11.9 A
- (b) 15 A
- (c) 23.8 A
- (d) 3.54 A

Solution: Correct option is (a)



If one of the diodes gets open circuited, the diode bridge starts acting as a half bridge rectifier. In order to determine the average current, we need to find the average value of output voltage,  $V_o$ . The waveform of the  $V_o$  is shown in the figure below.



The diodes  $D_1$  and  $D_4$  gets forward biased only when  $v_{in}(t)$  exceeds 200 V.

The value of  $\theta$  can be calculated as below:

$$\theta = \sin^{-1}\left(\frac{200}{230\sqrt{2}}\right) = 37.94^\circ = 0.662 \text{ radians}$$

The average value of the output voltage can be calculated as:

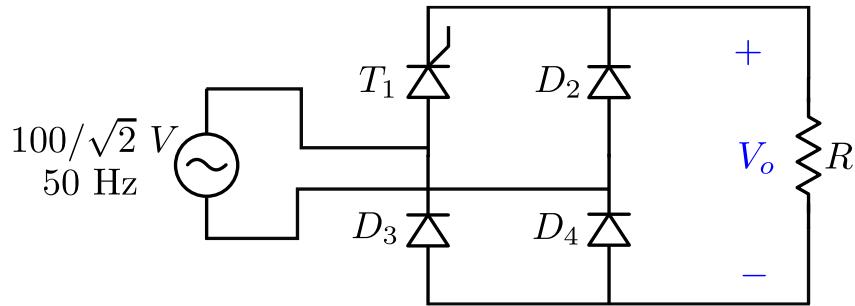
$$V_o = \frac{1}{2\pi} \left( \int_0^\theta 200 \cdot d(\omega t) + \int_\theta^{\pi-\theta} 230\sqrt{2} \sin(\omega t) \cdot d(\omega t) + \int_{\pi-\theta}^{2\pi} 200 \cdot d(\omega t) \right) = 223.8 \text{ V}$$

The average value of current can be calculated as

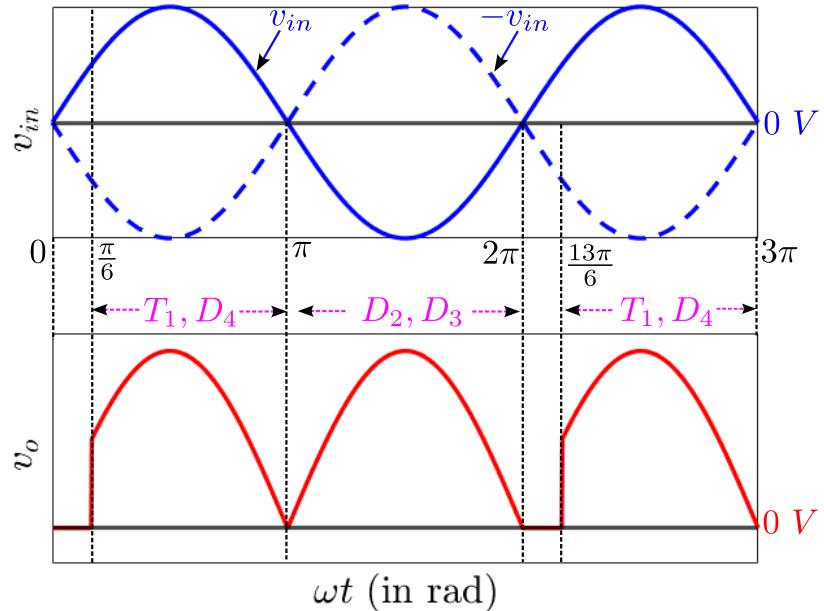
$$I_{o,avg} = \frac{223.8 - 200}{2} = 11.9 \text{ A}$$

**Question 7: Numerical type**

In the given rectifier, the firing angle of thyristor (SCR)  $T_1$  measured from the positive going zero crossing of  $V_s$  is  $30^\circ$ . If the input voltage,  $v_{in}$ , is  $100 \sin(100\pi t)$  V, the average voltage across  $R$  (in Volts) under steady-state is \_\_\_\_\_.



Solution: Answer range (61-62)



During the period  $0 \leq \omega t \leq \frac{\pi}{6}$ , none of the switches will be conducting as  $T_1$  is not fired and  $D_2$  and  $D_3$  are reverse biased.

For  $\frac{\pi}{6} \leq \omega t \leq \pi$ ,  $T_1$  and  $D_4$  starts conducting as  $T_1$  is fired at  $\omega t = \frac{\pi}{6}$ .

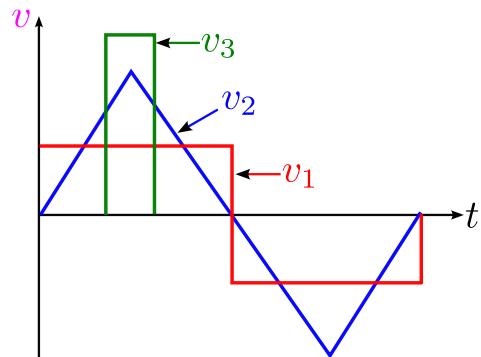
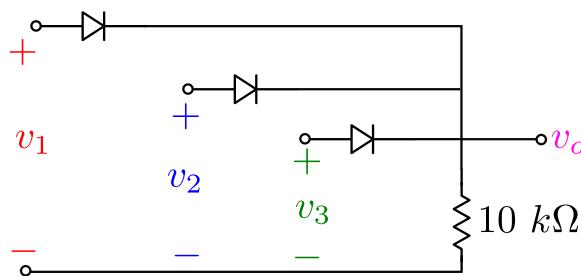
For  $\pi \leq \omega t \leq 2\pi$ ,  $D_2$  and  $D_3$  starts conducting as these diodes are forward biased.

The waveform of the output voltage,  $v_o$ , is shown in the figure above. Thus, the average value of the output voltage can be calculated as

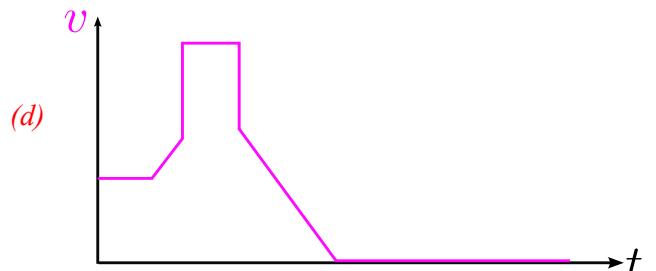
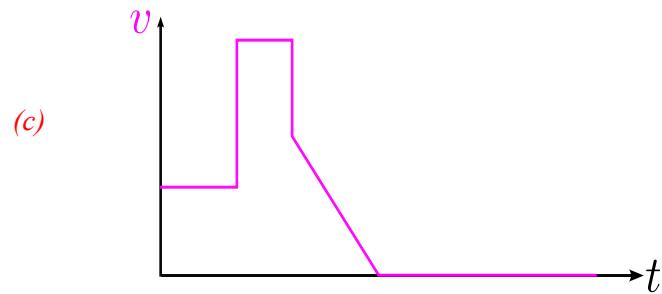
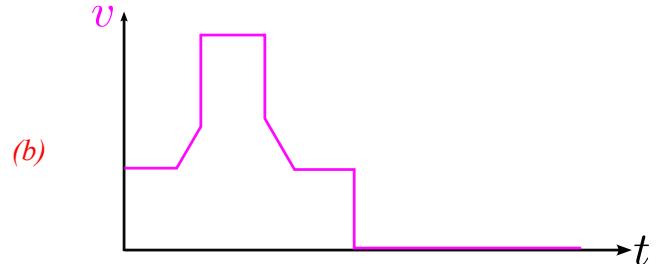
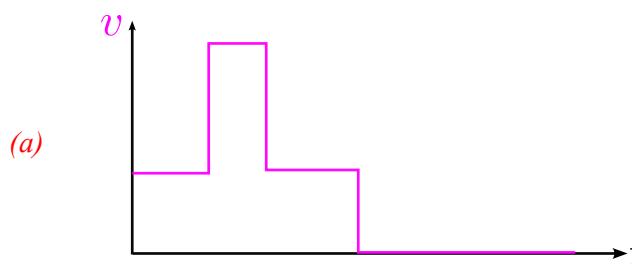
$$V_o = \frac{1}{2\pi} \left( \int_{\frac{\pi}{6}}^{\pi} 100 \sin(\omega t) \cdot d(\omega t) + \int_{\pi}^{2\pi} 100 \sin(\omega t) \cdot d(\omega t) \right) = 61.53 \text{ V}$$

*Question 8:*

In the circuit shown below, three signals of the Fig. (b) are impressed on the input terminals of Fig. (a)



If the diodes are ideal then the voltage,  $v_o$ , is

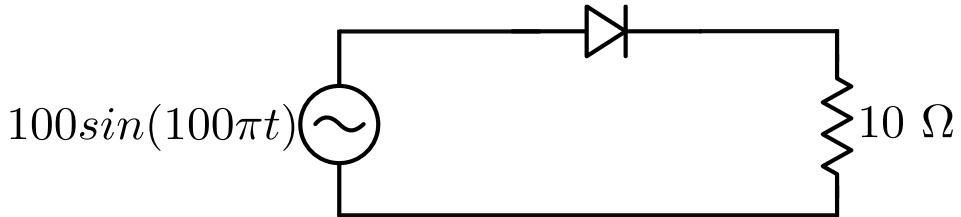


Solution: Correct option is (b)

The output voltage would be maximum of  $(v_1(t), v_2(t), v_3(t))$  at any instant in time.

**Question 9: Numerical type**

In the circuit shown below the diode used is ideal. The input power factor is \_\_\_\_\_ (Give answer upto two decimal places).



Solution: Answer range (0.65 - 0.75)

The rms value of the voltage across the  $10 \Omega$  resistor is

$$V_{o,rms} = \frac{V_m}{2} = 50 \text{ V}$$

Where,  $V_m$  is the peak value of sinusoidal supply voltage.

The power consumed by the resistor is therefore

$$P = \frac{50^2}{10} = 250 \text{ W}$$

The rms value of the source current is given as

$$I_{s,rms} = \frac{V_{o,rms}}{10} = 5 \text{ A}$$

Thus, total VA supplied to the load is

$$VA = V_{s,rms} \times I_{s,rms} = \frac{100}{\sqrt{2}} \times 5$$

Where,  $V_{s,rms}$  is the rms value of the source voltage.

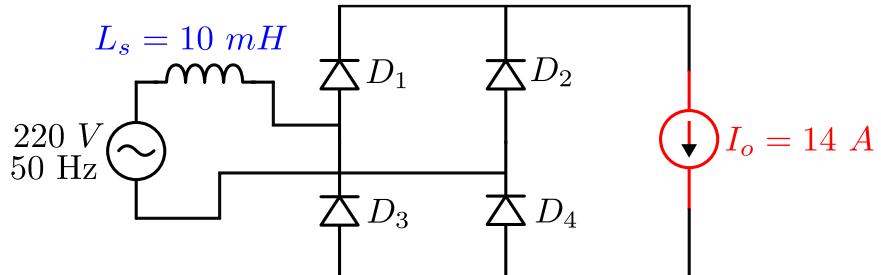
Thus, the input power factor can be calculated as

$$p.f. = \frac{P}{VA} = 0.707$$

**Question 10: Numerical type**

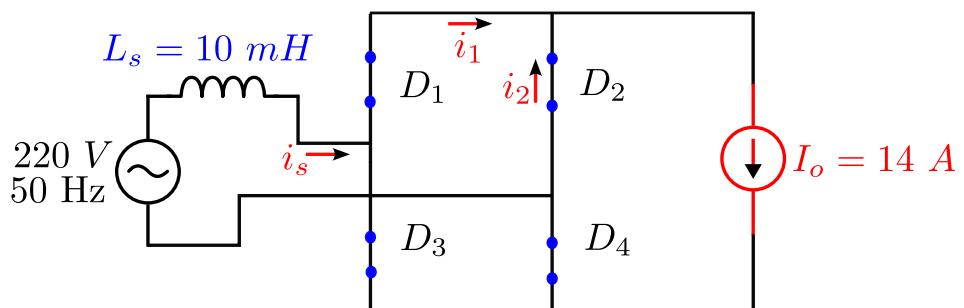
The figure shows an uncontrolled full bridge rectifier supplied from a 220 V, 50 Hz single phase ac source.

The load draws a constant current of  $I_o = 14 \text{ A}$ . The conduction angle of the diodes in degrees (rounded off to two decimal places) is \_\_\_\_\_.



Solution: Answer range (220-230)

In an uncontrolled full bridge rectifier without a source inductance,  $L_s$ , the load current immediately shifts from  $(D_1, D_4)$  to  $(D_2, D_3)$  and vice-versa as the polarity of the source voltage changes. But any practical voltage source comes with a source inductance which cannot be avoided. In such a case the current does not immediately shift from  $(D_1, D_4)$  to  $(D_2, D_3)$ , rather the current through the diodes  $(D_1, D_4)$  gradually reduces and current through the diodes  $(D_2, D_3)$  gradually increases as the polarity of the source voltage goes from positive to negative. During this small period of time, called the overlapping period, all the four diodes will be conducting and the voltage across the current source will be 0 V during this overlapping period.



Applying KCL we have,

$$i_1 + i_2 = I_o$$

As  $I_o = \text{constant}$ , we can write

$$\frac{di_1}{dt} + \frac{di_2}{dt} = 0 \rightarrow \frac{di_1}{dt} = -\frac{di_2}{dt}$$

Again, applying KCL at the input node we have

$$i_s = i_1 - i_2$$

Taking derivative w.r.t 't' on both sides we get

$$\frac{di_s}{dt} = \frac{di_1}{dt} - \frac{di_2}{dt} = 2 \frac{di_1}{dt}$$

As all the diodes are conducting, the entire supply voltage appears across the source inductance. Therefore, we can write:

$$v_{in} = L_s \frac{di_s}{dt} = 2L_s \frac{di_1}{dt}$$

Say the current  $i_1$  is increasing from 0 to  $I_o$  during this period ' $\mu$ '. Therefore, integrating the above equation, we get

$$\int_0^\mu 220\sqrt{2} \sin(\omega t) \cdot d(\omega t) = 2\omega L_s \int_0^{I_o} di_1$$

Therefore, we have

$$220\sqrt{2} (1 - \cos \mu) = 2\omega L_s I_o$$

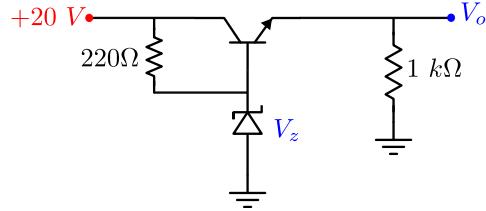
Thus, the overlapping period ' $\mu$ ' can be calculated as

$$\mu = \cos^{-1} \left( 1 - \frac{2\omega L_s I_o}{220\sqrt{2}} \right) = 44.17^\circ$$

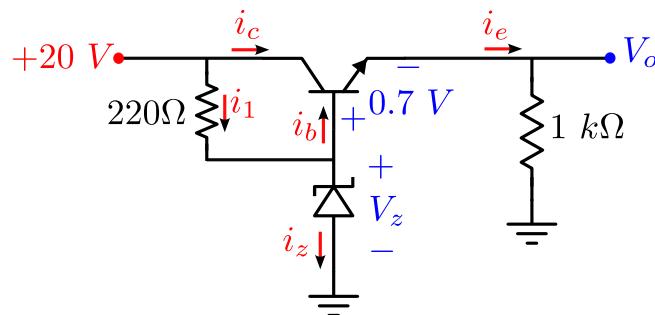
The conduction angle of the diode is therefore  $= 180^\circ + 44.17^\circ = 224.17^\circ$

**Question 1: Numerical type**

In the regulator circuit shown below  $V_Z = 12 \text{ V}$ ,  $\beta = 50$ ,  $V_{BE} = 0.7 \text{ V}$ . The Zener current (in mA) is \_\_\_\_\_.



Solution: Answer range (36.0 - 36.2)



Applying KVL we can obtain the value of the output voltage as

$$V_o = V_z - 0.7 = 11.3 \text{ V}$$

Now, the emitter current can be calculated as

$$i_e = \frac{V_o}{1k} = 11.3 \text{ mA}$$

As the BJT is operating in linear region and hence the base current can be calculated as

$$i_b = \frac{i_e}{1 + \beta} = 0.22 \text{ mA}$$

We can calculate  $i_1$  as

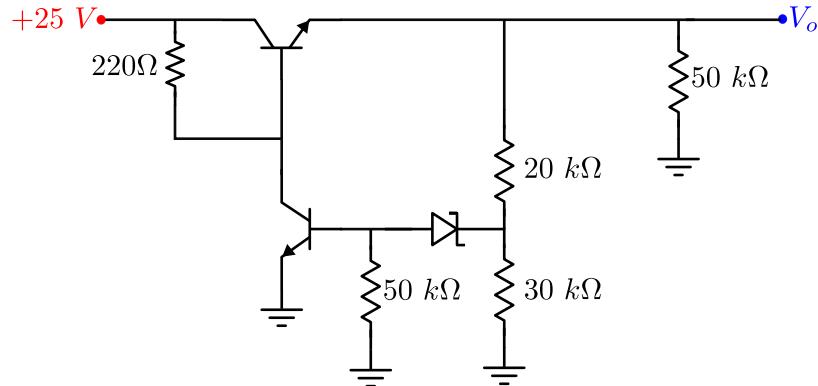
$$i_1 = \frac{20 - V_Z}{0.22k} = \frac{20 - 12}{0.22} = 36.36 \text{ mA}$$

Now applying KCL we can write

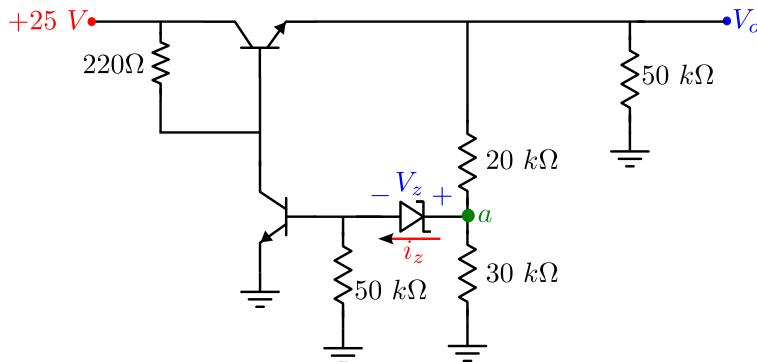
$$i_z = i_1 - i_b = 36.14 \text{ mA}$$

**Question 2: Numerical type**

In the series voltage regulator circuit shown below assume the Zener diode to be ideal. Given that:  $V_Z = 8.3 \text{ V}$ ,  $\beta = 50$ ,  $V_{BE} = 0.7 \text{ V}$ , What would be the output voltage,  $V_o$ , (in Volts) \_\_\_\_\_.



Solution: Answer range (14.8-15.2)



In this problem, we must assume first whether the transistors are ON or OFF and whether the Zener is in reverse breakdown region or not. Based on the assumption, we solve the circuit to see whether our assumptions are right or wrong. Based on this method, we have found out that both the transistors are ON, and the Zener is in reverse breakdown. **Please note that “ON” here doesn’t mean it is in saturation. It means that the transistors are in linear region, and it basically behaves like a resistor. For series regulator circuits, normally the transistors operate in linear region.**

The potential at the point ‘a’ can be calculated as

$$V_a = V_{BE} + V_Z = 9 \text{ V}$$

As Zener diode is assumed to ideal, then we have

$$i_z \approx 0 \text{ A}$$

Now, applying potential division we have

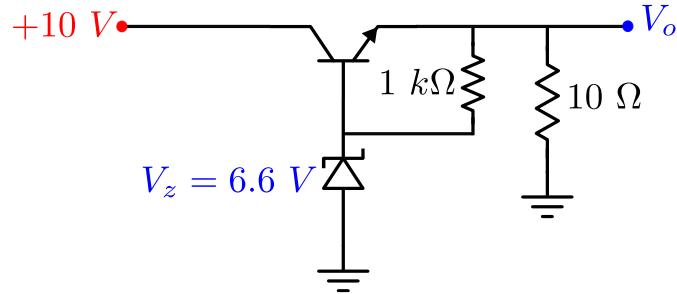
$$V_a = \frac{30}{30 + 20} V_o = \frac{3}{5} V_o$$

Thus, the output voltage  $V_o$  can be calculated as

$$V_o = \frac{5}{3} V_a = 15 \text{ V}$$

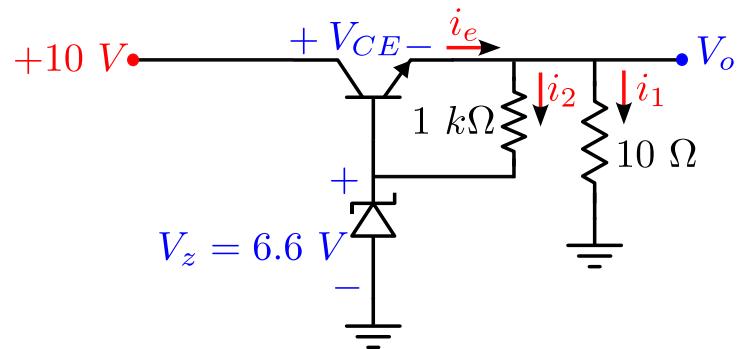
*Question 3:*

The three terminal linear voltage regulator is connected to a  $10 \Omega$  load resistor as shown in the figure below. If  $V_{in}$  is 10 V, what is the power dissipated in the transistor. (Assume  $V_{BE} = 0.6$  V)



- (a) 0.6 W
- (b) 4.2 W
- (c) 2.4 W
- (d) 5.4 W

Solution: Correct option is (c)



The output voltage of the linear voltage regulator can be calculated as

$$V_o = V_z - V_{BE} = 6.6 - 0.6 = 6 \text{ V}$$

$i_1$  can be calculated as follows

$$i_1 = \frac{V_o}{10} = 0.6 \text{ A}$$

$i_2$  can be calculated as follows

$$i_2 = \frac{V_o - V_z}{1k} = -0.6 \text{ mA}$$

Applying KCL we get the value of emitter current,  $i_e$ , as

$$i_e = i_1 + i_2 = 0.599 \text{ A}$$

Now, the emitter-collector voltage can be calculated as

$$V_{CE} = 10 - V_o = 10 - 6 = 4 \text{ V}$$

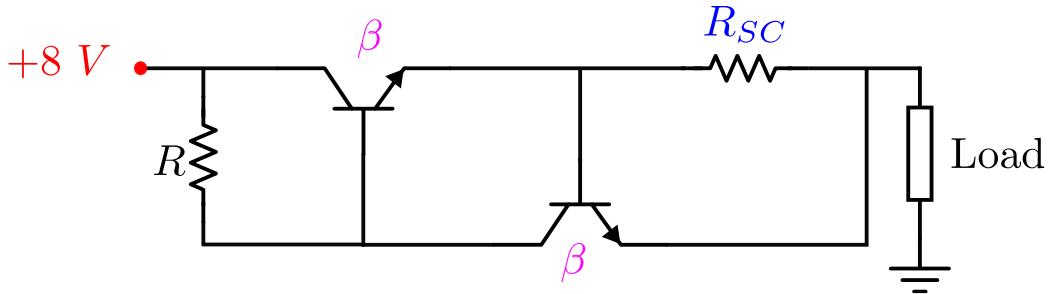
Thus, the power dissipated in the transistor can now be calculated as

$$P = V_{CE} \times i_e = 2.39 \text{ W}$$

*Question 4:*

A 5V regulator uses a 12 W series pass transistor. Find  $R_{sc}$  for output short circuit protection.

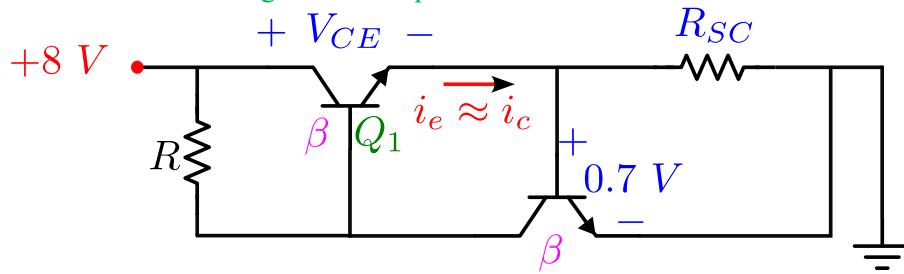
(Assume  $V_{BE} = 0.7 V$ ,  $\beta \rightarrow \infty$ )



- (a)  $0.13 \Omega$
- (b)  $0.23 \Omega$
- (c)  $0.33 \Omega$
- (d)  $0.43 \Omega$

Solution: **Correct option is (d)**

If the load gets shorted the circuit given in the question becomes as shown below



The transistor is rated for 12 W. Thus,  $R_{sc}$  should be chosen such that the current flowing through the transistor  $Q_1$  during short circuit conditions does not cause a power dissipation more than the rated power of  $Q_1$ .

The collector to emitter voltage can be calculated as

$$V_{CE} = 8 - 0.7 = 7.3 V$$

The rated power of transistor  $Q_1$  is 12 W. Thus, the maximum permissible current through  $Q_1$  can be calculated as

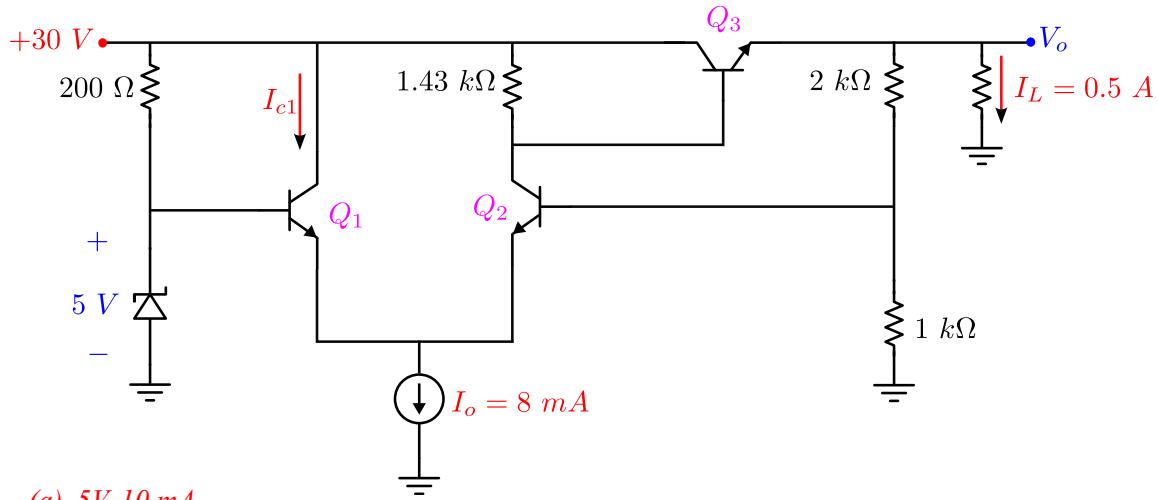
$$i_{c,max} \approx i_{e,max} = \frac{12}{V_{CE}} = 1.64 A$$

As  $\beta \rightarrow \infty$ , the base current of the transistors can be neglected, and we can assume that  $i_{e,max}$  is flowing through  $R_{sc}$ . Thus,  $R_{sc}$  can be calculated as

$$R_{sc} = \frac{0.7}{1.64} \approx 0.43 \Omega$$

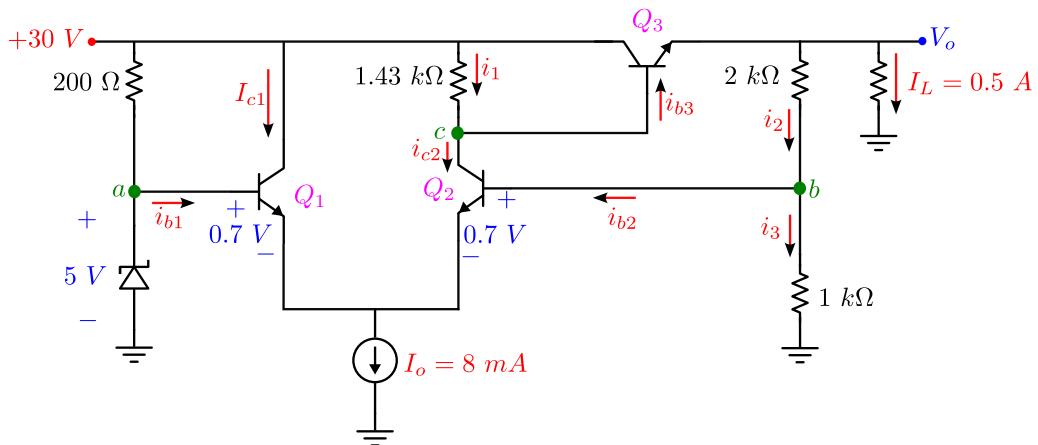
Question 5:

In the circuit diagram given below assume that  $Q_1$  and  $Q_2$  has infinite current gain (i.e.  $\beta_1 \approx \beta_2 \rightarrow \infty$ ) The current gain of transistor  $Q_3$ ,  $\beta_3 = 99$ . Calculate  $V_o$  (in V),  $I_{c1}$  (in mA) if  $I_L = 0.5$  A. (Assume  $V_{BE} = 0.7$  V)



- (a) 5V, 10 mA
- (b) 5V, 4.95 mA
- (c) 15V, 4.95 mA
- (d) 15V, 3.05 mA

Solution: Correct option is (d)



From the above circuit diagram, we can conclude that

$$V_a = V_b = 5 V$$

As  $\beta_2 \rightarrow \infty$  and  $\beta_1 \rightarrow \infty$ , we have

$$i_{b1} = i_{b2} = 0$$

Thus, applying potential divider we can write

$$V_b = \frac{1}{3} V_o$$

Thus, the output voltage,  $V_o$ , can be calculated as

$$V_o = 3 \times V_b = 15 \text{ V}$$

The potential at point ‘c’ can be calculated as

$$V_c = V_o + 0.7 = 15.7 \text{ V}$$

Thus,  $i_1$  can be calculated as

$$i_1 = \frac{30 - V_c}{1.43} \text{ mA} = 10 \text{ mA}$$

Since  $i_{b2} = 0$ , the current flowing through  $2 \text{ k}\Omega$  can be calculated as

$$i_2 = \frac{V_o}{3} = 5 \text{ mA}$$

Applying KCL, the emitter current of  $Q_3$  can be calculated as

$$i_{e3} = I_L + i_2 = 505 \text{ mA}$$

Thus, the base current of  $Q_3$  is

$$i_{b3} = \frac{i_{e3}}{1 + \beta_3} = 5.05 \text{ mA}$$

Thus, the collector current of  $Q_2$  is

$$i_{c2} = i_1 - i_{b3} = 4.95 \text{ mA}$$

Since  $i_{b2} = 0$ , we can write

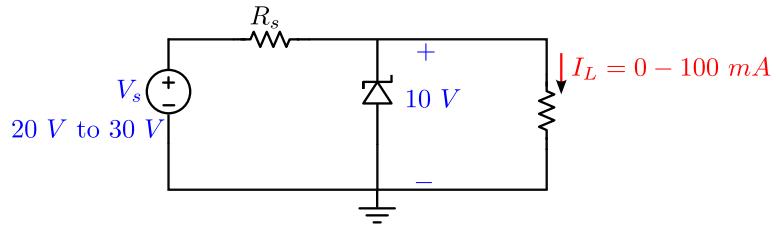
$$i_{c2} = i_{e2} = 4.95 \text{ mA}$$

Thus, the collector current of  $Q_1$  is

$$I_{C1} = I_0 - i_{e2} = 8 - 4.95 = 3.05 \text{ mA}$$

**Question 6: Numerical type**

Find the value of  $R_s$  (in  $\Omega$ ) as a worst-case design, if  $V_s$  ranges from 20 V to 30 V and  $I_L$  ranges from 0 to 100 mA and  $I_{Z(knee)} = 1 \text{ mA}$ .



Solution: Answer range (98.5-99.5)

$I_{Z(knee)}$  is the minimum current that must flow through the Zener diode so that it can maintain a voltage of  $V_Z = 10 \text{ V}$ .

Worst case condition would be:

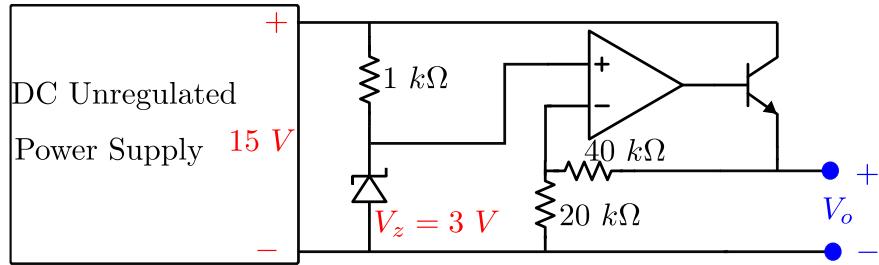
$$V_s = 20 \text{ V} \text{ and } I_L = 100 \text{ mA}$$

Because it would be the case when the voltage drop across  $R_s$  would be maximum. The value of  $R_s$  can then be calculated as

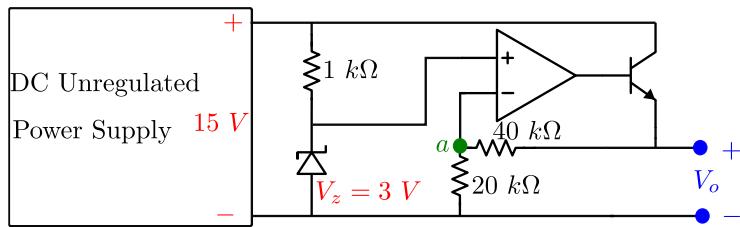
$$R_s = \frac{20 - 10}{I_{Z(knee)} + I_L} = \frac{10}{101} \times 10^3 \Omega = 99 \Omega$$

**Question 7: Numerical type**

Find the output voltage,  $V_o$  (in volts), of the regulated power supply shown in the figure. Assume the op-amp to be ideal.



Solution: Answer range (8.9-9)



As the op-Amp is ideal, the gain of op-Amp is infinite. And hence due to virtual grounding

$$V_a = V_z = 3 \text{ V}$$

Again, we have

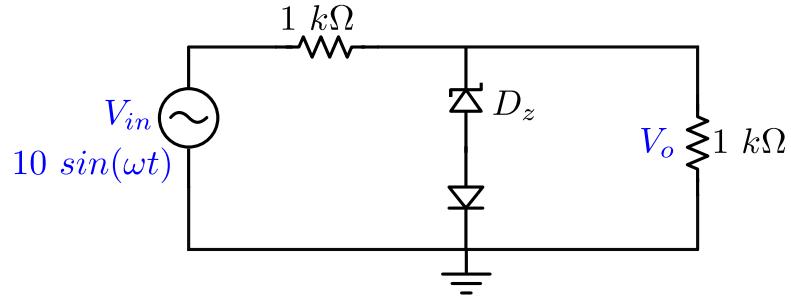
$$V_a = \frac{20}{20 + 40} V_o = \frac{1}{3} V_o$$

The output voltage of regulated power supply is

$$V_o = 3V_a = 9 \text{ V}$$

*Question 8:*

The cut-in voltage of both Zener diode  $D_z$  and  $D$  shown in the figure below is 0.7 V while breakdown voltage of the Zener is 3.3 V and reverse breakdown of  $D$  is 50 V. The other parameters can be assumed to be the same as those of an ideal diode. The values of the peak output voltage ( $V_o$ ) are



- (a) 3.3 V in the positive half cycle and 1.4 V in the negative half cycle
- (b) 4 V in the positive half cycle and 5 V in the negative half cycle
- (c) 3.3 V in both positive and negative half cycle
- (d) 5 V in both positive and negative half cycle

Solution: Correct option is (b)

In the positive half cycle,

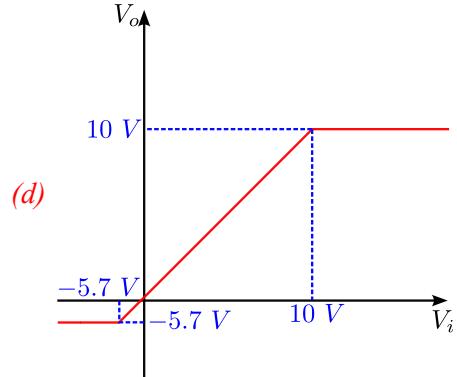
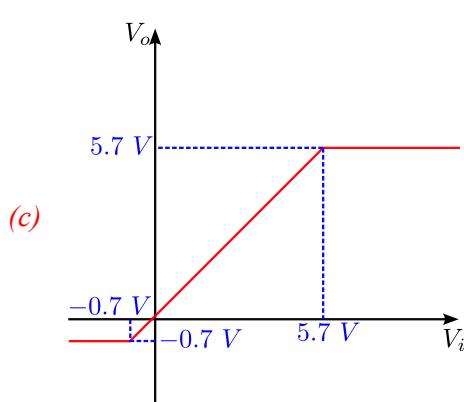
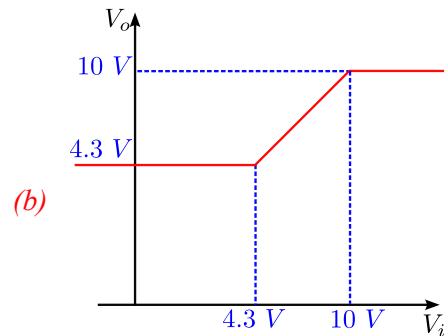
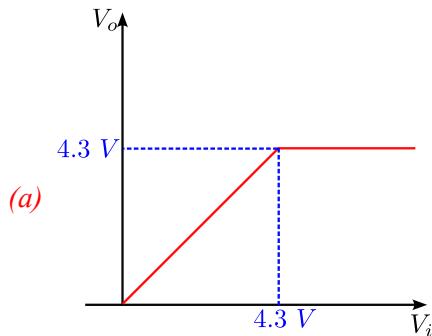
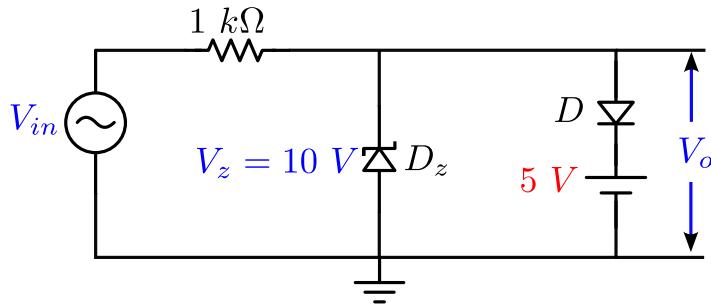
When  $V_o$  exceeds ( $V_z + 0.7 V = 4 V$ ), it gets clamped to 4 V

In the negative half cycle,

The diode  $D$  remains reverse biased and hence  $V_o = \frac{V_{in}}{2}$ . Hence, the peak value of  $V_o$  in the negative half cycle is 5 V.

**Question 9:**

Assuming forward voltage drop of the diodes to be 0.7 V, the input-output transfer characteristics of the circuit is



Solution: Correct option is (c)

When  $-0.7 \text{ V} \leq V_{in} \leq 5.7 \text{ V}$ ,

Diode D remains reverse biased. The Zener diode acts as open circuit as  $V_{in}$  has not exceeded its breakdown voltage ( $V_z = 10 \text{ V}$ ). Thus. During this period  $V_o = V_{in}$

When  $V_{in} > 5.7 \text{ V}$ ,

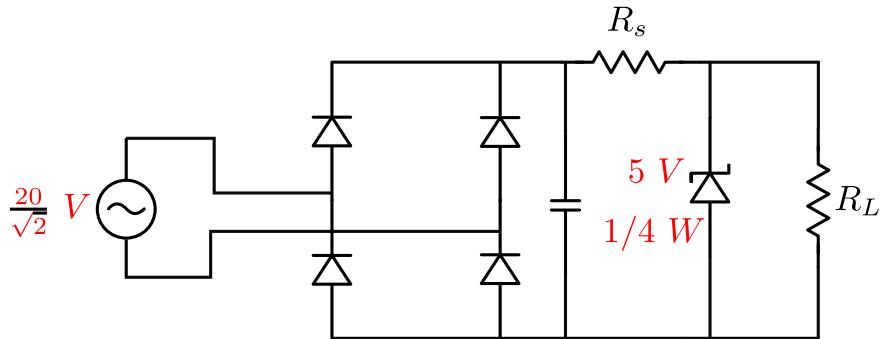
The output voltage gets clamped at 5.7 V.

When  $V_{in} \leq -0.7 \text{ V}$ ,

The Zener diode starts acting as a forward biased diode and hence the output voltage gets clamped at -0.7 V.

**Question 10: Numerical Type**

The sinusoidal ac source in the figure has rms value of  $\frac{20}{\sqrt{2}} V$ . Considering all possible values of  $R_L$ , the minimum value of  $R_s$  in  $\Omega$  to avoid burnout of the Zener diode is \_\_\_\_\_.



Solution: Answer range (299-300)

If  $R_L \rightarrow \infty$  (i.e. open circuit condition),

The load current would flow through the Zener diode. Thus, we should ensure that the power dissipation during this condition does not exceed the rated value of  $0.25 W$ . Therefore,

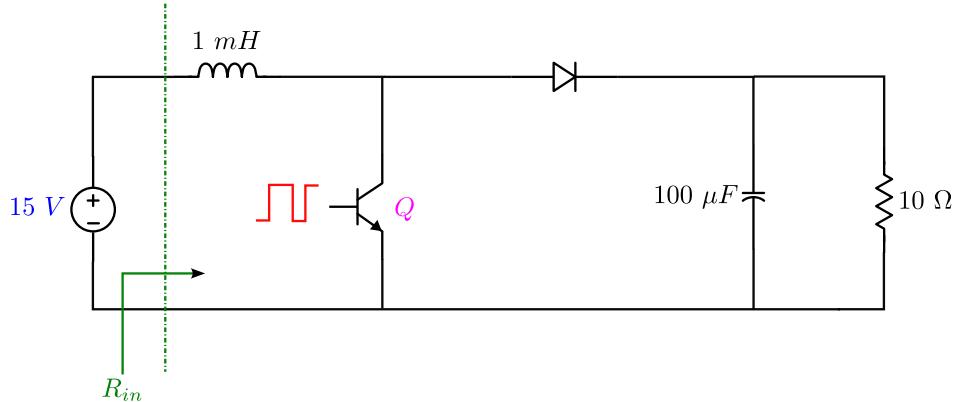
$$i_{Z,max} = \frac{0.25}{5} = 0.05 A$$

Considering the worst-case condition, the voltage across the capacitor will be almost close to the peak value of the source voltage. Thus, the value of resistance  $R_s$  should be

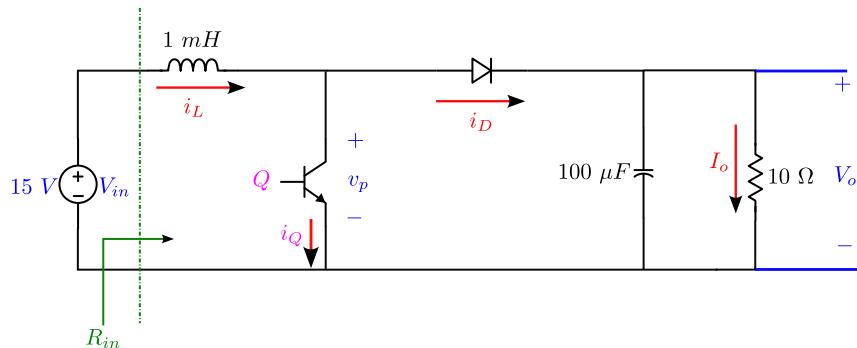
$$R_s = \frac{20 - 5}{0.05} = 300 \Omega$$

**Question 1: Numerical type**

Consider a boost converter shown in the circuit schematic. Switch  $Q$  is operating at 25 kHz with a duty cycle of 0.6. Assume the diode and switch to be ideal. Under steady-state conditions, the average resistance,  $R_{in}$ , as seen by the source is \_\_\_\_\_  $\Omega$ . (Round off to two decimal places)



Solution: Answer Range (1.55 - 1.65)



The output voltage of the boost converter can be calculated as

$$V_o = \frac{1}{1-D} \times V_{in} = \frac{15}{1-0.6} = 37.5 V$$

Thus, the load current,  $I_o$ , is

$$I_o = \frac{V_o}{10} = 3.75 V$$

By small ripple approximation we can derive

$$I_o = (1-D)I_L$$

Where,  $I_L$  is the average value of the inductor current,  $i_L$ . Thus, we can calculate  $I_L$  as

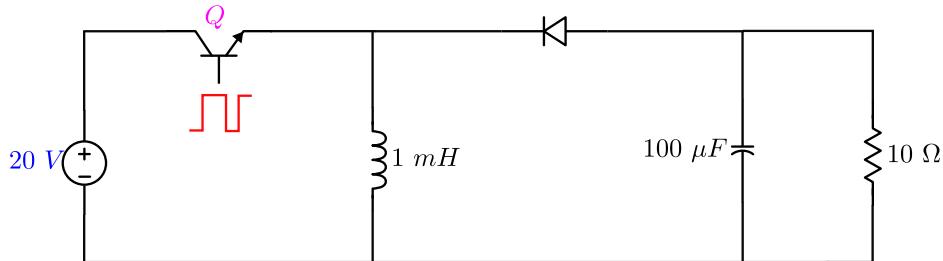
$$I_L = \frac{I_o}{(1-D)} = \frac{3.75}{(1-0.6)} = 9.375 A$$

$I_L$  is the average current as seen by the source  $V_{in}$ . Thus, the average value of resistance as seen by the source is

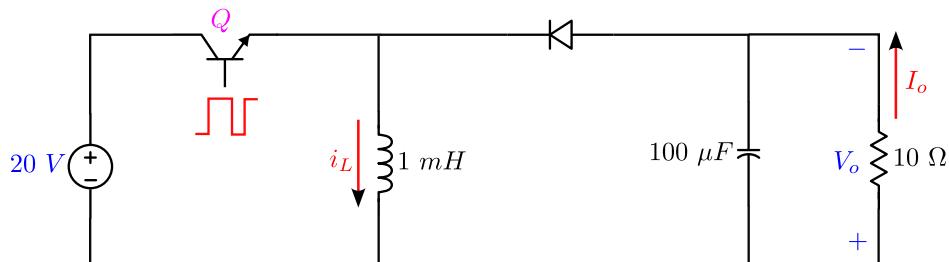
$$R_{in} = \frac{V_{in}}{I_L} = \frac{15}{9.375} = 1.6 \Omega$$

**Question 2: Numerical type**

Consider the buck-boost converter as shown in the circuit schematic below. Switch  $Q$  is operating at 25 kHz and 0.75 duty-cycle. Assume diode and switch to be ideal. Under steady-state conditions, the average current flowing through the inductor is \_\_\_\_\_ A.



Solution: Answer range (24-24)



The output voltage of a buck-boost converter is given by

$$V_o = \frac{D}{1-D} V_{in} = \frac{0.75}{1-0.75} \times 20 = 60 \text{ V}$$

The output current,  $I_o$ , can then be calculated as

$$I_o = \frac{V_o}{10} = 6 \text{ A}$$

Now, by small ripple approximation we can write

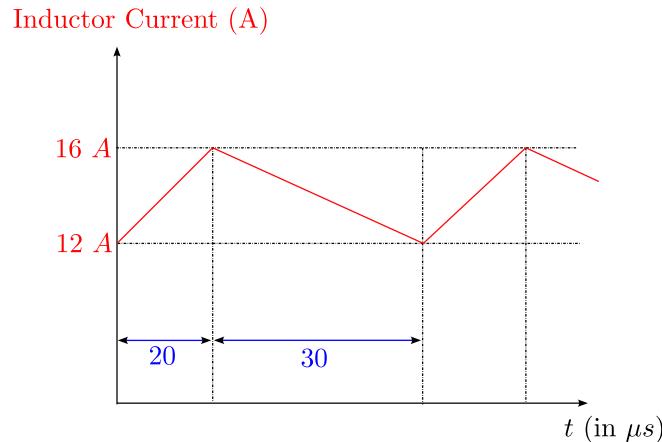
$$I_o = (1 - D)I_L$$

Where,  $I_L$  is the average value of the inductor current  $i_L$ . Thus, we can calculate the average value of the inductor current as

$$I_L = \frac{I_o}{(1 - D)} = 24 \text{ A}$$

**Question 3: Numerical type**

The steady-state current flowing through the inductor of a DC-DC buck-boost converter is shown below. If the peak-to-peak ripple in output voltage of converter is 1 V, then the value of the output capacitor, in  $\mu F$ , is \_\_\_\_\_ (round off to nearest integer).



Solution: Answer range (167-169)

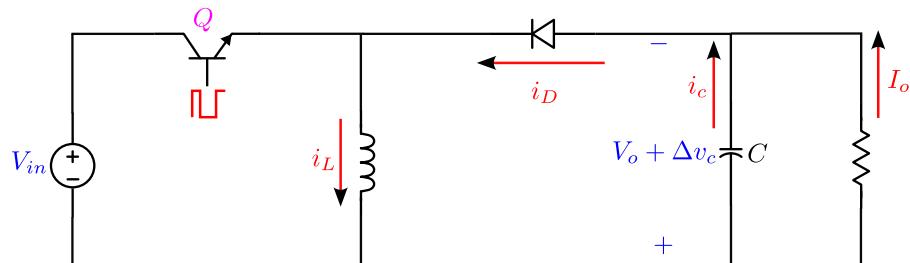


Fig. a

The waveform of the inductor current,  $i_L$ , diode current,  $i_D$ , and capacitor ripple current,  $i_c$  are shown in the Fig . b.

The average value of  $i_D$  is the load current  $I_o$  and is indicated by a dotted blue line in the Fig . b. Thus, we can calculate  $I_o$  as

$$I_o = \frac{1}{50} \left( 12 \times 30 + \frac{1}{2} \times 30 \times 4 \right) = 8.4 \text{ A}$$

The ripple current flowing through the capacitor can be obtained by subtracting the load current  $I_o$  from the diode current as shown in Fig. b. (Since net charge stored in the capacitor over a cycle is 0 Coulomb, or in other words, average current through the capacitor is 0 A). The charge stored in the capacitor ( $\Delta Q_c$ ) during the on time of the switch is indicated by the shaded yellow area in Fig . b.

We can determine ( $\Delta Q_c$ ) as

$$\Delta Q_c = C(\Delta v_c) = 8.4 \times 20 \mu C$$

Thus, output capacitor filter requirement is

$$C = \frac{8.4 \times 20}{\Delta v_c} = 168 \mu F$$

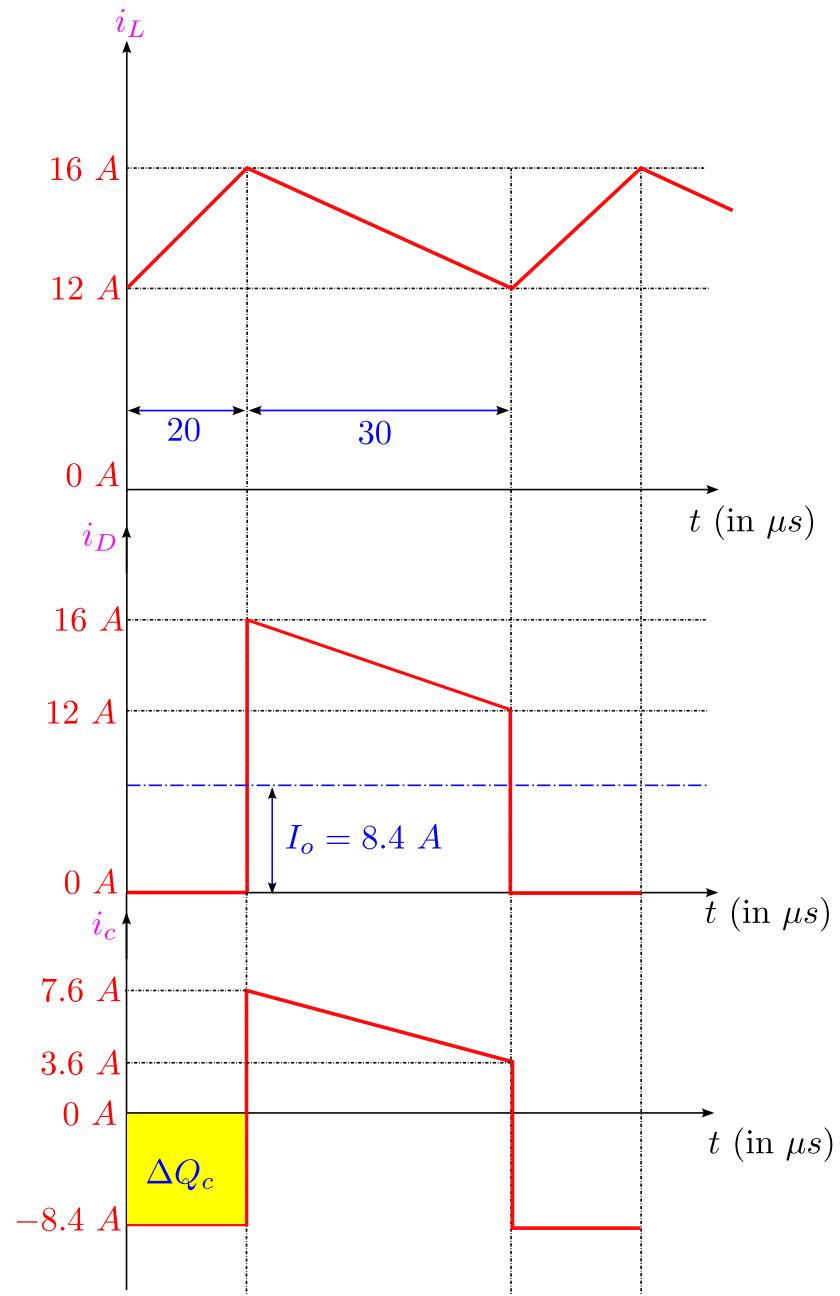
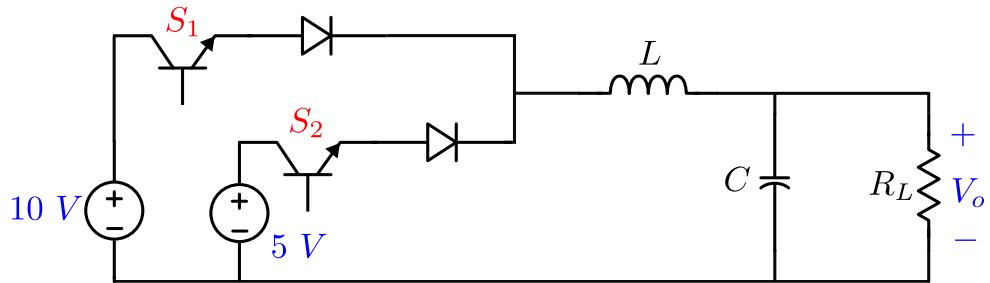


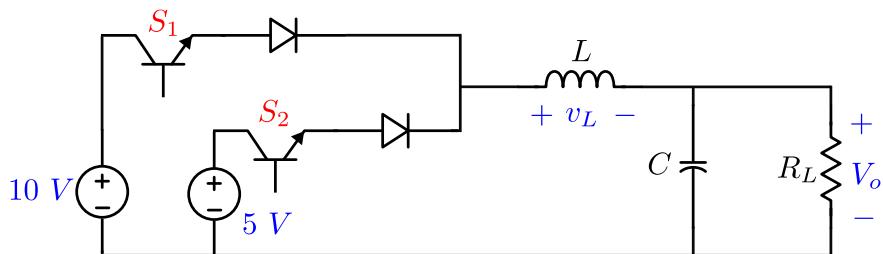
Fig. b

**Question 4: Numerical type**

The circuit shown in the figure is meant to supply a resistive load  $R_L$  from two separate DC voltage sources. The switches  $S_1$  and  $S_2$  are controlled so that only one of them is ON at any instant.  $S_1$  is turned on for 0.2 ms and  $S_2$  is turned on for 0.3 ms in a 0.5ms switching cycle time period. Assuming continuous conduction of the inductor current and negligible ripple on the capacitor voltage, the output voltage  $V_o$  (in volts) across  $R_L$  is \_\_\_\_\_.



**Solution:** Answer range (6.99 - 7)



During  $0 < t < 0.2 \text{ ms}$ , the switch  $S_1$  is on. Thus, the voltage across the inductor during this period is

$$v_L = 10 - V_o$$

During  $0.2 \text{ ms} < t < 0.5 \text{ ms}$ , the switch  $S_2$  is on. Thus, the voltage across the inductor during this period is

$$v_L = 5 - V_o$$

Now, applying volt-sec balance across the inductor we can write

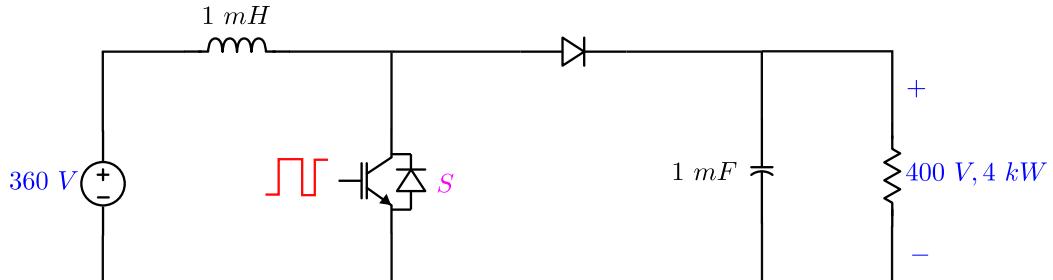
$$(10 - V_o) \times 0.2 + (5 - V_o) \times 0.3 = 0$$

Solving the above equation, we get

$$V_o = 7 \text{ V}$$

**Question 5: Numerical type**

A DC-DC boost converter as shown in the figure below is used to boost 360 V to 400 V at a power of 4kW. All devices are ideal considering continuous inductor current, the rms current in the solid-state switch (*S*), (in Amperes) is \_\_\_\_\_ . (Neglect the ripple in Inductor Current)



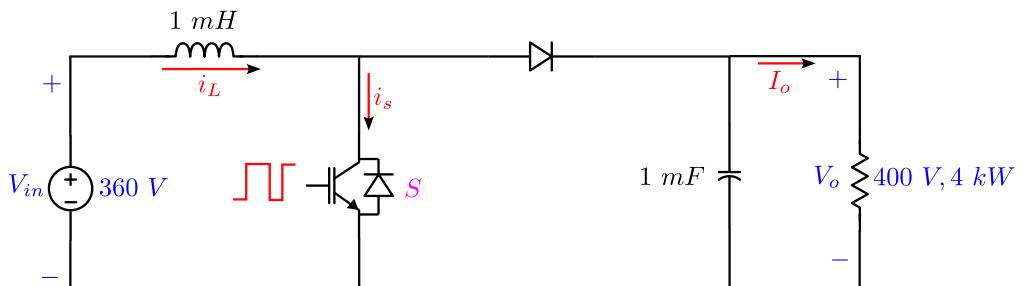
**Solution:** Answer range (3.0 – 4.0)

The output power is given as

$$P_o = V_o I_o = 4 \times 10^3 \text{ W}$$

From the input and output voltages of the boost converter we can calculate the duty ratio, *D*, as

$$D = 1 - \frac{V_{in}}{V_o} = 0.1$$



The average value of the load current can then be calculated as

$$I_o = \frac{P_o}{V_o} = \frac{4 \times 10^3}{4 \times 10^2} = 10 \text{ A}$$

Now, as the semiconductor switches are considered ideal, we can neglect the losses in these devices. Thus, we can equate the input power to output power as shown below

$$P_{in} = P_o = 4 \times 10^3 \text{ W}$$

The average value of inductor current can be written as

$$I_L = \langle i_L \rangle_{avg} = \frac{P_{in}}{V_{in}} = 11.11 \text{ A}$$

The rms value of the current flowing through the switch '*S*' can be calculated as follows

$I_{s,rms} = \sqrt{D} I_L = 3.51 \text{ A}$  (Neglecting Ripple in Inductor current. You can draw the waveform for the switch current and then calculate rms value and you will get the same expression)

**Question 6:**

A chopper is employed to charge a battery as shown in the figure below. The charging current is 5 A. The duty ratio is 0.2. The chopper output voltage is also shown in figure. The peak-to-peak ripple current in the charging current is

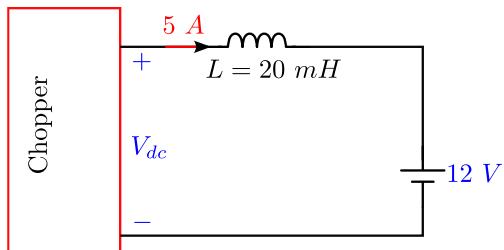


Fig. (a)

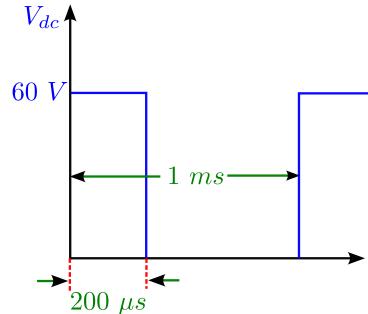


Fig. (b)

- (a) 0.48 A
- (b) 1.2 A
- (c) 0.24 A
- (d) 0.96 A

Solution: **Correct option is (a)**

For the time interval  $0 < t < 200 \mu s$ , the voltage across the inductor can be calculated as

$$v_L = 60 - 12 = L \frac{\Delta i_L}{\Delta t}$$

Therefore, the ripple current can be calculated as

$$\Delta i_L = \frac{48}{L} \times \Delta t = \frac{48}{20 \times 10^{-3}} \times 200 \times 10^{-6} = 0.48 A$$

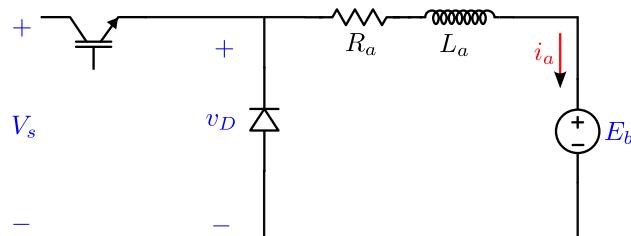
**Question 7:**

A step-down chopper operates from a dc voltage source,  $V_s$ , feeds a dc motor armature with a back emf of  $E_b$ . From oscilloscope traces, it is found that the armature current increases for time,  $t_r$ , falls to zero over the time,  $t_f$ , and remains zero for the time,  $t_o$ , in every chopping cycle, then the average dc voltage across the freewheeling diode is: [Assume Diode forward drop to be 0V]

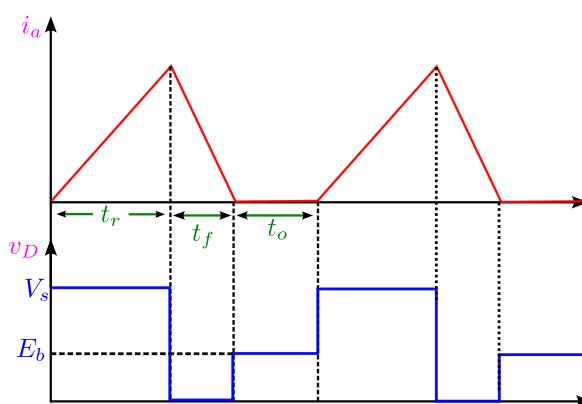
- (a)  $\frac{V_s t_r}{t_r + t_f + t_o}$
- (b)  $\frac{V_s t_r + E_b t_f}{t_r + t_f + t_o}$
- (c)  $\frac{V_s t_r + E_b t_o}{t_r + t_f + t_o}$
- (d)  $\frac{V_s t_r + E_b (t_f + t_o)}{t_r + t_f + t_o}$

Solution: **Correct option is (c)**

A dc motor armature is excited from a step-down chopper. The equivalent circuit is shown in the schematic below



The waveforms of the armature current,  $i_a$ , and the diode voltage,  $v_D$ , is shown in the figure below:



The average value of voltage across the diode can be calculated from the waveform of  $v_D$  as

$$V_D = \langle v_D \rangle_T = \frac{V_s t_r + E_b t_o}{t_r + t_f + t_o}$$

**Question 8: Numerical type**

The semiconductor switch shown in the Fig. (a) is operated at a frequency of 20 kHz and duty ratio of 0.5. The circuit operates in steady state,  $V_1 = 100$  V and  $V_2 = 275$  V. The diagram of inductor current  $I_L$  is shown in Fig. (b). The value of  $\beta T$  is \_\_\_\_\_  $\mu s$ .

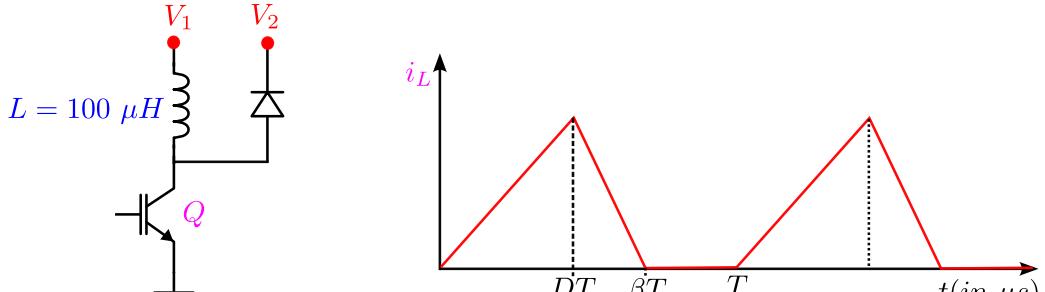
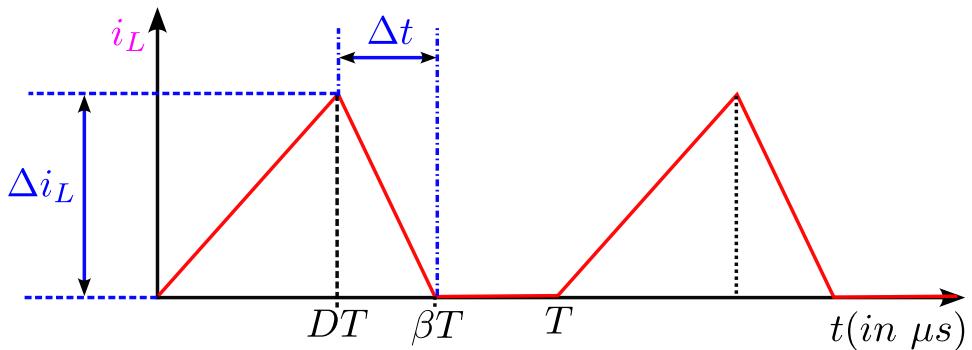


Fig. (a)

Fig. (b)

Solution: Answer range (38 - 40)



When the switch  $Q$  is on the voltage across the inductor can be written as

$$v_L = V_1 = 100 = L \times \frac{\Delta i_L}{DT}$$

Thus, the ripple current in the inductor,  $\Delta i_L$ , can be evaluated as

$$\Delta i_L = \frac{100}{L} \times DT = 25 A$$

Now, as the switch  $Q$  turns off, the diode starts conducting and the voltage across the inductor becomes

$$v_L = V_1 - V_2 = -175 = -L \times \frac{\Delta i_L}{\Delta t}$$

Negative sign is taken as the slope is negative. Now,  $\Delta t$  can be calculated as

$$\Delta t = \frac{L \times \Delta i_L}{175} = 14.29 \mu s$$

Now, we have

$$\beta T = \Delta t + DT = 39.28 \mu s$$

**Question 9: Numerical type**

In continuation with previous question, if  $V_2 = 300 \text{ V}$ , what is the power transferred (in Watts) from the dc voltage source  $V_1$  to dc voltage source  $V_2$ . Assume the controlled and uncontrolled switches to be ideal.

Solution: Answer range (936-938)

In the previous question we have found that

$$\Delta i_L = \frac{100}{L} \times DT = 25 \text{ A}$$

Now, when the switch  $Q$  is turned off,

$$v_L = V_1 - V_2 = -200 = -L \times \frac{\Delta i_L}{\Delta t}$$

Thus,  $\Delta t$  can be calculated as

$$\Delta t = \frac{L \times \Delta i_L}{200} = 12.5 \mu\text{s}$$

The switch is switched at 20 kHz. Thus, the time-period ( $T$ ) can be calculated as

$$T = \frac{1}{20 \times 10^3} = 50 \mu\text{s}$$

Thus, the average value of the inductor current can be calculated as

$$I_L = \langle i_L \rangle_{avg} = \frac{1}{50} \left( \frac{1}{2} \times (DT + \Delta t) \times \Delta i_L \right) = 9.375 \text{ A}$$

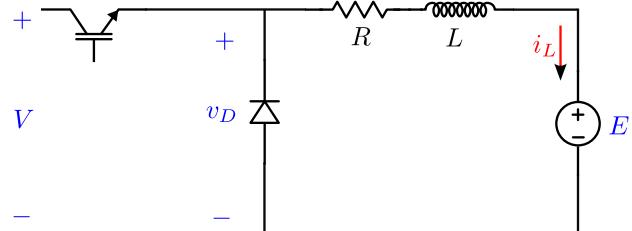
Thus, power transferred from voltage source  $V_1$  to  $V_2$  can be calculated as

$$P = I_L \times V_1 = 9.375 \times 100 = 937.5 \text{ W}$$

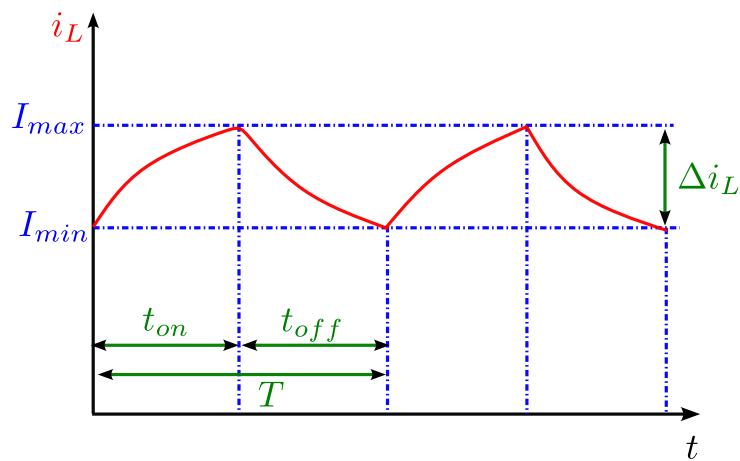
**Question 10:**

A DC chopper feeds an RLE load as shown in the figure below. The value of E is increased by 20%, the current ripple

- (a) Increases by 20%
- (b) Decreases by 20%
- (c) Increases by 10%
- (d) Remains same



Solution: Correct option is (d)



The expression for  $I_{max}$  can be derived as

$$I_{max} = \frac{V}{R} \left[ \frac{1 - e^{-t_{on}/t_a}}{1 - e^{-T/t_a}} \right] - \frac{E}{R}$$

Where  $t_a = \frac{L}{R}$  is the time constant of the circuit.

The expression for  $I_{min}$  can be derived as

$$I_{min} = \frac{V}{R} \left[ \frac{e^{t_{on}/t_a} - 1}{e^{T/t_a} - 1} \right] - \frac{E}{R}$$

Thus, the inductor current ripple can be calculated as

$$\Delta i_L = I_{max} - I_{min} = \frac{V}{R} \left[ \frac{1 - e^{-\frac{t_{on}}{t_a}}}{1 - e^{-\frac{T}{t_a}}} \right] - \frac{V}{R} \left[ \frac{e^{\frac{t_{on}}{t_a}} - 1}{e^{\frac{T}{t_a}} - 1} \right]$$

Thus, the ripple current is independent of 'E'.

[Hint for Derivation: For  $T_{ON}$  and  $T_{OFF}$  draw the 2 circuits. First consider the  $T_{ON}$  circuit (which is an RL circuit with 2 sources  $V$  and  $E$ ), solve for  $i_L$ , with initial condition as  $I_{min}$ . In the expression

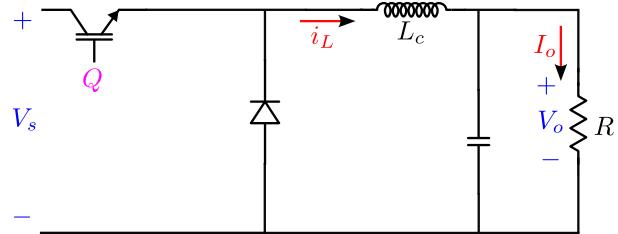
*obtained for  $i_L$  substitute  $t=t_a$  to obtain  $I_{max}$ . Then consider the  $T_{OFF}$  circuit (which is an RL circuit with just  $E$  as source. Ignore diode drop), solve for  $i_L$ , with initial condition as  $I_{max}$ . In the expression obtained for  $i_L$ , substitute  $t=T$  to obtain  $I_{min}$ . Then you can solve for  $I_{max}$  and  $I_{min}$ . ]*

*Question 1:*

The boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) in a DC-DC converter is the operating condition where the inductor current just touches zero at the end of the switching cycle but doesn't stay at zero for any significant duration.

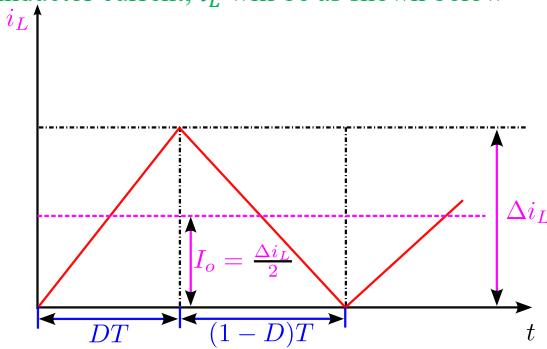
In the chopper circuit shown in the figure below, the input dc voltage has a constant value,  $V_s$ . The output voltage,  $V_o$ , is assumed to be ripple free. The switch,  $Q$ , is operated with a switching time-period,  $T$ , and a duty ratio,  $D$ . What is the value of critical inductance,  $L_c$ , at the boundary of continuous and discontinuous conduction of the inductor current,  $i_L$ .

- (a)  $L_c = \frac{V_s D(1-D)T}{2I_o}$
- (b)  $L_c = \frac{2V_o}{(1-D)TI_o}$
- (c)  $L_c = \frac{V_s (1-D^2)}{2I_o}$
- (d)  $L_c = \frac{V_o (T-1)}{2DTI_o}$



Solution: Correct option is (a)

The waveform of the inductor current,  $i_L$  will be as shown below



When the switch  $Q$  is off, the voltage across the inductor is given as

$$v_L = -L_c \frac{\Delta i_L}{(1-D)T} = -V_o$$

Thus, we can write

$$L_c = V_o \frac{(1-D)T}{\Delta i_L}$$

At the boundary of continuous and discontinuous conduction mode

$$I_o = \frac{\Delta i_L}{2}$$

The relationship between output and input voltage of a buck converter is given by

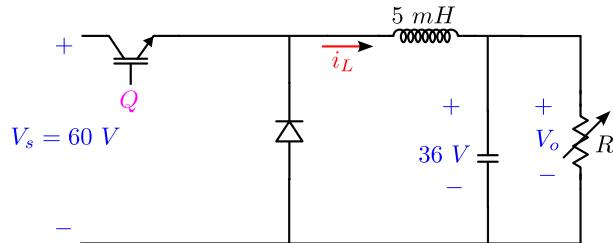
$$V_o = DV_s$$

Thus, the expression for  $L_c$  is given as

$$L_c = V_o \frac{(1-D)T}{\Delta i_L} = V_s \frac{D(1-D)T}{2I_o}$$

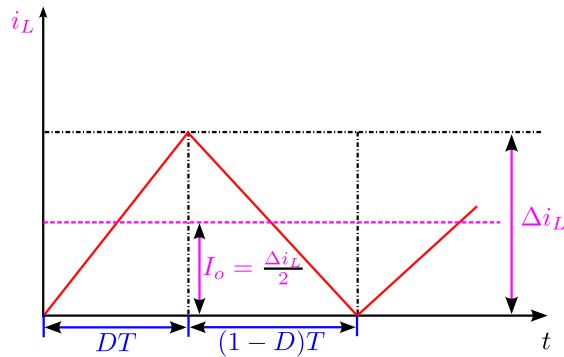
**Question 2: Numerical type**

A buck converter feeding a variable resistive load is shown in the figure below. The switching frequency of the switch,  $Q$ , is 100 kHz and the duty ratio of 0.6. The output voltage,  $V_o$ , is 36 V. Assume that all the components are ideal, and the output voltage is ripple free. The value of  $R$  (in  $\Omega$ ) that will make the inductor current,  $i_L$ , just continuous is \_\_\_\_\_.



Solution: Answer range (2500-2500)

The waveform of the inductor current,  $i_L$  will be as shown below



When the switch  $Q$  is off, the voltage across the inductor is given as

$$v_L = -L \frac{\Delta i_L}{(1 - D)T} = -V_o$$

Thus, the inductor current ripple is given as

$$\Delta i_L = V_o \frac{(1 - D)T}{L} = 2I_o$$

Thus, the load current is given by

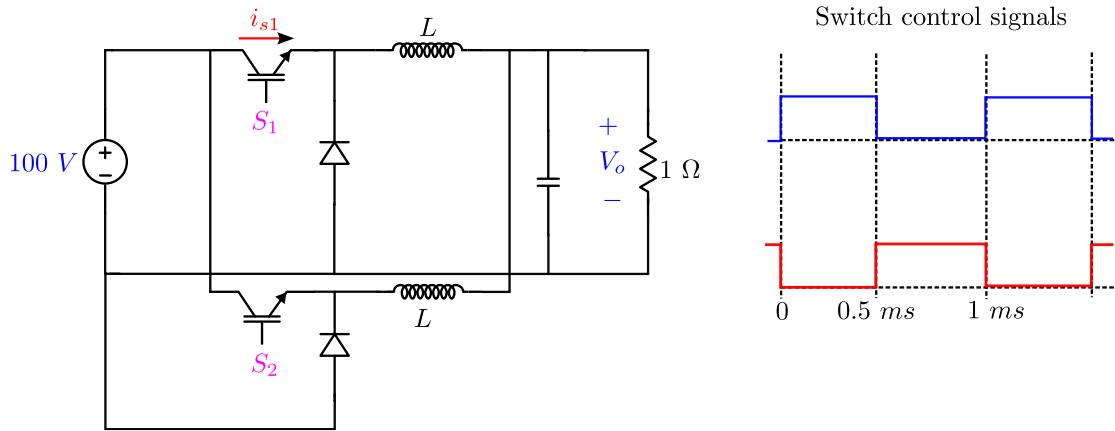
$$\frac{V_o}{R} = V_o \frac{(1 - D)T}{2L}$$

Thus, the value of the load resistance is given as

$$R = \frac{2L}{(1 - D)T} = \frac{2Lf}{(1 - D)} = 2500 \Omega$$

**Question 3: Numerical type**

The figure shows two buck converters connected in parallel. The common input dc voltage for the converters has a value of 100 V. The converters have inductors of identical value. The load resistance is 1 Ω. The capacitor voltage has negligible ripple. Both converters operate in continuous conduction mode. The switching frequency is 1 kHz and the switch control signals are as shown. The circuit operates in steady state. Assuming that the converters share the load equally, the average value of the current of switch  $S_1$ ,  $i_{s1}$ , (in Ampere) up to two decimal places \_\_\_\_\_.



**Solution:** Answer range (12-13)

Two buck converters are connected in parallel. Thus, the output voltage,  $V_o$ , is given by

$$V_o = DV_{in} = 0.5 \times 100 = 50 V$$

Thus, the load current can be calculated as

$$I_o = \frac{50}{1} = 50 A$$

Now, power balance equation is given by

$$100 \times i_{s1} + 100 \times i_{s2} = V_o I_o$$

Where,  $i_{s2}$  is the average value of current flowing through switch  $S_2$ .

As the load is shared equally, we must have

$$i_{s1} = i_{s2}$$

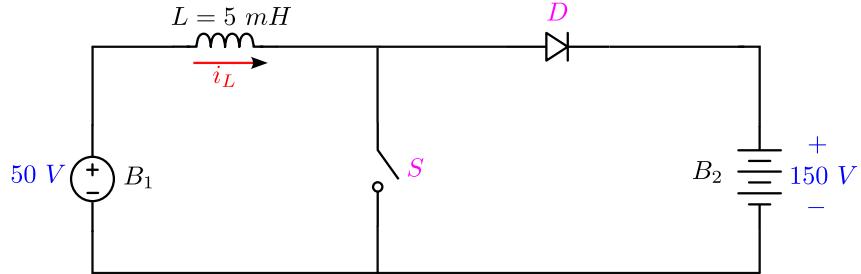
Thus,  $i_{s1}$  can be calculated as

$$2 \times 100 \times i_{s1} = V_o I_o$$

$$i_{s1} = \frac{V_o I_o}{2 \times 100} = \frac{50 \times 50}{2 \times 100} = 12.5 A$$

**Question 4: Numerical type**

A dc-to-dc converter shown in the figure is charging a battery bank,  $B_2$ , whose voltage is constant at 150 V.  $B_1$  is another battery bank whose voltage is constant at 50 V. The value of the inductor  $L$  is 5 mH and the ideal switch  $S$  is operated with a switching frequency of 5 kHz with a duty ratio of 0.4. Once the circuit has reached steady state and assuming the diode  $D$  to be ideal, the power transferred from  $B_1$  to  $B_2$  (in Watt) is \_\_\_\_\_ (up to 2 decimal places).



**Solution:** Answer range (11-13)

When the switch,  $S$ , is on, the voltage across the inductor is given as

$$v_L = 50 = L \frac{\Delta i_L}{DT}$$

During this period, the inductor current rises from its minimum value  $I_{min}$  to its maximum value  $I_{max}$

Thus, the ripple inductor current can be calculated as

$$\Delta i_L = \frac{50}{L} DT = \frac{50}{5 \times 10^{-3}} \times 0.4 \times \frac{1}{5 \times 10^3} = 0.8 A$$

Let us calculate the time,  $t_f$ , for the inductor current to fall from  $I_{max}$  to  $I_{min}$ . The inductor current starts falling when the switch  $S$  is off. During this period, the voltage across the inductor is given as

$$v_L = 50 - 150 = -100 = -L \frac{\Delta i_L}{t_f}$$

Thus,  $t_f$  can be calculated as

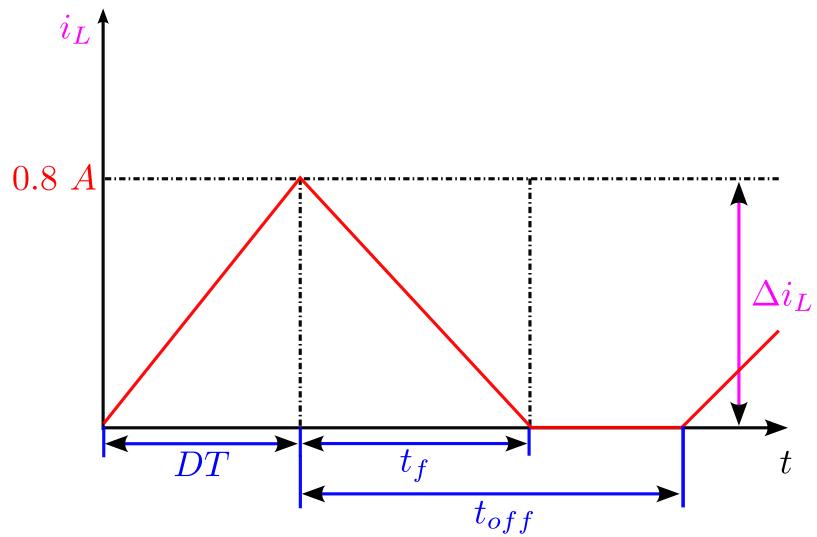
$$t_f = \frac{L \times \Delta i_L}{100} = 40 \mu s$$

The off period of the switch  $S$  can be calculated as

$$t_{off} = (1 - D) \frac{1}{f_{sw}} = 120 \mu s$$

As  $t_{off} > t_f$ , the inductor current is discontinuous as shown in the figure below. Thus, the average value of the inductor current can be calculated as

$$I_L = \frac{1}{T} \times \left[ \frac{1}{2} \times DT \times \Delta i_L + \frac{1}{2} \times t_f \times \Delta i_L \right] = 0.24 A$$

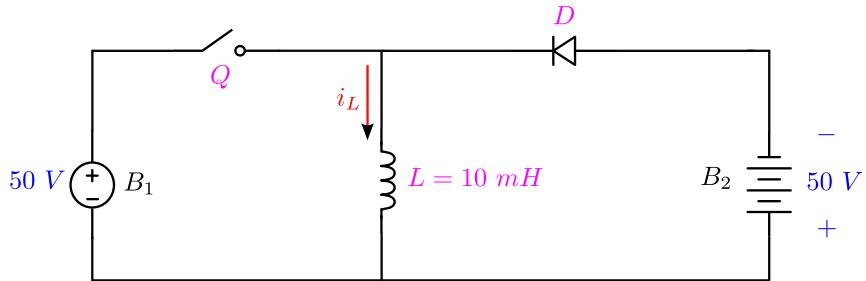


Thus, the power transferred from  $B_1$  to  $B_2$  is

$$P = I_L \times 50 = 12 \text{ W}$$

*Question 5:*

In the dc-dc converter shown in the figure below, the switch, Q, is switched at a frequency of 10 kHz with a duty ratio of 0.6. All the components of the circuit are ideal and the initial current in the inductor is 0 A. Energy stored in the inductor in mJ (rounded off to 2 decimal places) at the end of 10 complete switching cycles is \_\_\_\_\_.



Solution: Answer range (4.95-5.05)

The initial current of the inductor,  $I_{L0} = 0 \text{ A}$ .

In the on period of the first cycle the increase in inductor current,  $\Delta i_{L1}$ , can be calculated as

$$\Delta i_{L1} = \frac{50}{L} \times t_{on} = \frac{50}{L} \times DT = 0.3 \text{ A}$$

In the off period of the first cycle the decrease in inductor current,  $-\Delta i_{L2}$ , can be calculated as

$$-\Delta i_{L2} = -\frac{50}{L} \times t_{off} = \frac{50}{L} \times (1 - D)T = -0.2 \text{ A}$$

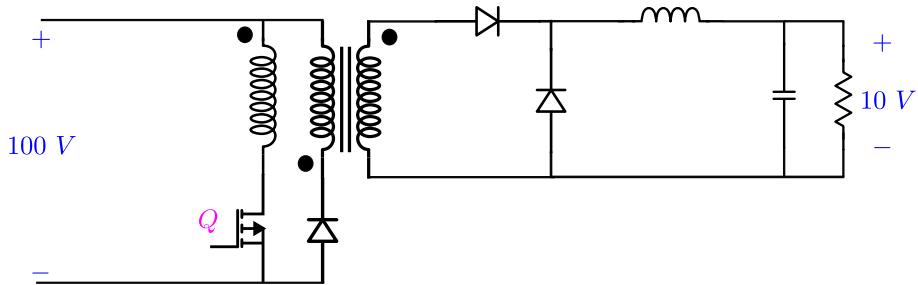
Thus, we can conclude that in every cycle during the ON period of switch Q the inductor current increases by 0.3 A and during the off period of switch the inductor current decreases by 0.2 A. Thus, net increase in the inductor current at the end of each cycle is 0.1 A. Thus, at the end of 10 complete switching cycles the inductor current increases by  $10 \times 0.1 \text{ A} = 1 \text{ A}$ . As the initial inductor current was 0 A. The inductor current at the end of 10 complete cycles is 1 A.

Thus, the energy stored in the inductor at the end of 10 complete cycles can be calculated as

$$E = \frac{1}{2} \times L \times i_L^2 = \frac{1}{2} \times 10 \times 10^{-3} \times 1 = 5 \text{ mJ}$$

**Question 6**

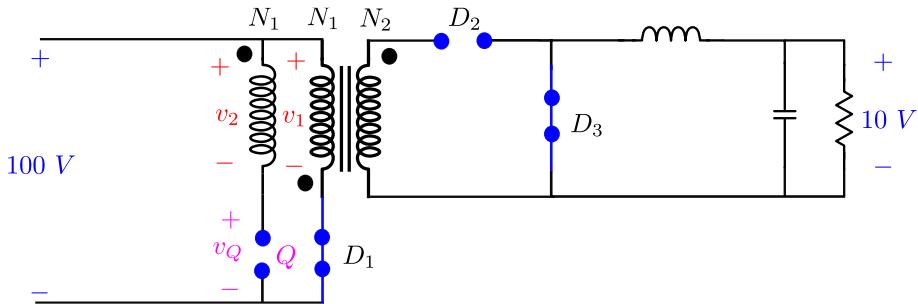
In a forward converter supplying a 10 V load from 100 V unregulated source, a bifilar wound demagnetizing winding is used to reset the core flux. If the leakage inductance as seen from the primary side is negligible, then what is the voltage stress (in Volts) on the primary switch Q? [Assume all the switches to be ideal.] \_\_\_\_\_.



Solution: Answer range (200-200)

As the demagnetizing winding is a bifilar wound winding it has the same number of turns as the primary winding.

To find the voltage stress across the switch Q we need to find the voltage across the switch when the switch is off and the core flux is being reset. The circuit therefore becomes as shown below



As switch Q is off and the diode D<sub>1</sub> is on, therefore

$$v_1 = 100 \text{ V}$$

Based on the dot polarity we can write

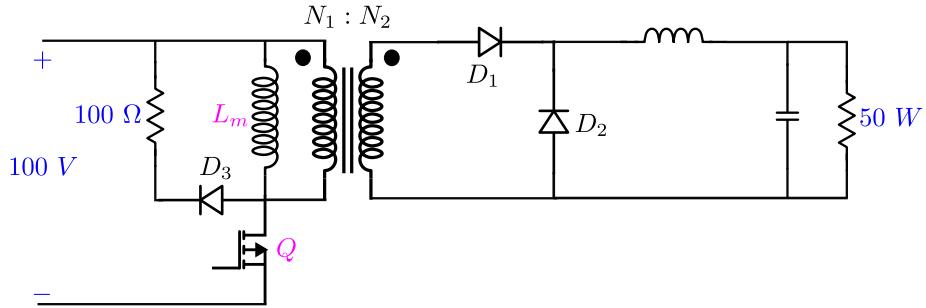
$$v_2 = -v_1 = -100 \text{ V}$$

Thus, the voltage across the switch Q is

$$v_Q = 100 - v_2 = 200 \text{ V}$$

**Question 7:**

A forward converter operates from an input voltage of 100V and supplies 50W load. The power semiconductor switch is operating at 20kHz and 50% duty cycle. The magnetizing inductance ( $L_m$ ) of the forward converter is 5 mH. A diode and a resistor is used across the primary winding for free-wheeling action. The resistor in the free-wheeling circuit has a value of 100 Ω. The wattage rating of the resistor should be greater than what value?



Solution: Answer range (12-13)

When the switch  $Q$  is turned off, the diode  $D_3$  is turned on and the energy in the magnetizing inductance is dissipated in the resistance 100 Ω. The magnetizing inductance stores energy during the on period of the switch. During the on period of the switch  $Q$  the voltage across the magnetizing inductance can be written as

$$v_L = 100 = L_m \frac{I_{m,pk}}{t_{on}} = L_m \frac{I_{m,pk}}{DT}$$

Where,  $I_{m,pk}$  is the peak value of the magnetizing current flowing through the magnetizing inductance  $L_m$ .

$$I_{m,pk} = \frac{100 \times D \times T}{L_m} = 0.5 A$$

Thus, the energy stored in the magnetizing inductance can now be calculated as

$$E = \frac{1}{2} \times L_m \times I_{m,pk}^2 = 0.625 mJ$$

Thus, the power that needs to be dissipated per cycle can be calculated as

$$P_{dis} = E \times f_{sw} = 12.5 W$$

*Question 8:*

*For a circuit realization of DC-DC converters which of the following rules are to be followed:*

1. *Current source should not be open circuited*
  2. *Voltage source should not be short circuited*
  3. *Inductor currents should not be interrupted*
  4. *Capacitor voltages should not be shorted*
- (a) *Only 1 and 2*  
(b) *Only 3 and 4*  
(c) *Only 1,2 and 4*  
(d) *All are true*

Solution: Correct option is (d)

*Question 9:*

*A dc-to-dc chopper supplied from a fixed DC voltage source feeds a fixed resistive-inductive load. The chopper operates at 1kHz and 50% duty cycle. Without changing the value of the average DC current through the load, if it is desired to reduce the ripple of the load current, the control action needed will be*

- (a) Increase the chopper frequency keeping the duty cycle constant
- (b) Increase the chopper frequency and duty cycle in equal ratio
- (c) Decrease only the chopper frequency
- (d) Decrease only the duty cycle

Solution: **Correct option is (a)**

The average load current can be expressed as

$$I_o = \frac{DV_{in}}{R}$$

So, if we want to keep the load current constant the duty ratio,  $D$ , must be kept constant.

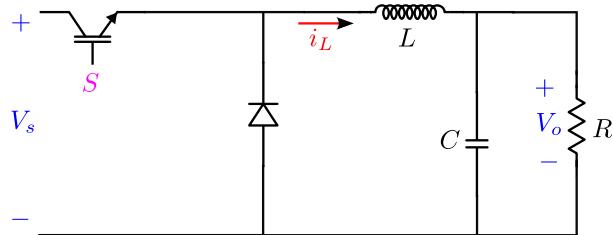
The expression for current ripple can be derived from transient analysis as

$$\Delta i_L \approx \frac{V_{in}}{4fL}$$

Thus, by increasing frequency current ripple can be reduced.

*Question 10:*

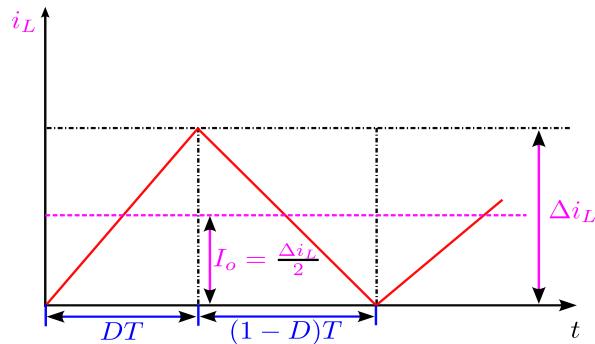
In the buck converter circuit shown in the figure below the input DC voltage has a constant value  $V_s$ . The output voltage  $V_o$  is assumed to be ripple free. The switch  $S$  is operated with a switching time period  $T$  and duty ratio  $D$ . What is the value of  $D$  at the boundary of continuous and discontinuous conduction of inductor current  $i_L$ .



- (a)  $D = 1 - \frac{V_s}{V_o}$
- (b)  $D = \frac{2L}{RT}$
- (c)  $D = 1 - \frac{2L}{RT}$
- (d)  $D = \frac{RT}{L}$

**Solution:** Correct option is (c)

The waveform of the inductor current,  $i_L$  will be as shown below



When the switch  $Q$  is off, the voltage across the inductor is given as

$$v_L = -L \frac{\Delta i_L}{(1-D)T} = -V_o$$

Thus, the inductor current ripple is given as

$$\Delta i_L = V_o \frac{(1-D)T}{L} = 2I_o$$

Thus, the load current is given by

$$\frac{V_o}{R} = V_o \frac{(1-D)T}{2L}$$

Thus, we have

$$D = 1 - \frac{2L}{RT}$$

*Question 1:*

*Energy stored in an inductor is given by  $\frac{1}{2}Li^2$ . Most of the energy is stored in*

- (a) *The rate of change of flux in the air gap*
- (b) *The mmf of the core material*
- (c) *The permeance of the core*
- (d) *The reluctance of the winding*

Solution: Correct option is (a)

Most of the energy is stored in the air gap.

*Question 2:*

*Transformers with bifilar winding will have*

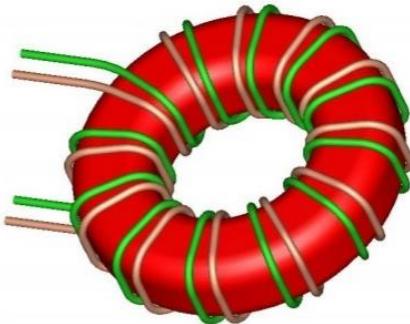
- (a) *Low interwinding capacitance, low leakage inductance and high insulation breakdown between windings*
- (b) *High interwinding capacitance, high leakage inductance and low insulation breakdown between windings*
- (c) *Low interwinding capacitance, low leakage inductance and low insulation breakdown between windings*
- (d) *High interwinding capacitance, low leakage inductance and low insulation breakdown between windings*

Solution: Correct option is (d)

**Bifilar windings** refer to a winding technique where two (or more) conductors are wound together in parallel around a core. These conductors are usually insulated from each other and can be connected in different configurations depending on the application. The term "bifilar" comes from "bi-" meaning two, and "filar" meaning thread or wire.

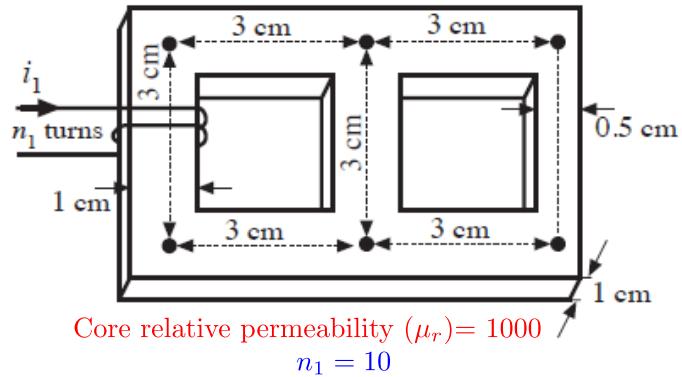
As the two conductors are placed close to each other they have very low leakage inductance and high interwinding capacitance. As the separation between the two parallel conductors is very low the insulation breakdown between the windings is low.

The figure below shows a simple bifilar winding wound around a toroidal core.



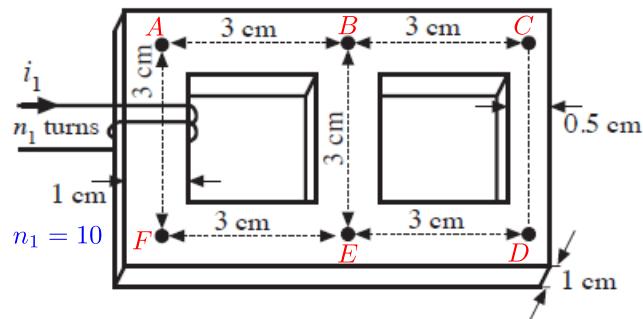
*Question 3:*

The core illustrated in Fig. (a) is 1 cm thick. All legs are 1 cm wide, except for the right-hand side vertical leg, which is 0.5 cm wide. You may neglect nonuniformities in the flux distribution caused by turning corners.



Determine the inductance of the winding in  $\mu\text{H}$ .

Solution: Answer range (109-111)



The mean magnetic path length  $EFAB = l_1 = 9 \text{ cm}$

The area of cross-section of the core  $= A_c = 1 \text{ cm}^2$

Thus, the reluctance of the path  $EFAB$  is given by

$$\mathcal{R}_1 = \frac{l_1}{\mu_r \mu_0 A_c} = \frac{9 \times 10^{-2}}{10^3 \times 4\pi \times 10^{-7} \times 10^{-4}} = 7.162 \times 10^5 \text{ H}^{-1}$$

The mean magnetic path length  $BE = l_2 = 3 \text{ cm}$

Thus, the reluctance of the path  $BE$  is given by

$$\mathcal{R}_2 = \frac{l_2}{\mu_r \mu_0 A_c} = \frac{3 \times 10^{-2}}{10^3 \times 4\pi \times 10^{-7} \times 10^{-4}} = 2.39 \times 10^5 \text{ H}^{-1}$$

The mean magnetic path length  $BC = l_3 = 3 \text{ cm}$

Thus, the reluctance of the path  $BC$  is given by

$$\mathcal{R}_3 = \mathcal{R}_2 = \frac{l_3}{\mu_r \mu_0 A_{c2}} = \frac{3 \times 10^{-2}}{10^3 \times 4\pi \times 10^{-7} \times 10^{-4}} = 2.39 \times 10^5 \text{ H}^{-1}$$

Similarly, the reluctance of the path ED is

$$\mathcal{R}_4 = \mathcal{R}_3 = \mathcal{R}_2 = \frac{l_3}{\mu_r \mu_o A_{c2}} = \frac{3 \times 10^{-2}}{10^3 \times 4\pi \times 10^{-7} \times 10^{-4}} = 2.39 \times 10^5 H^{-1}$$

The width of the leg CD is 0.5 cm. Thus, the cross-sectional area of the core of this leg is half of  $A_c$ . Thus, we have the cross-sectional area of the leg ( $A_{c2}$ ) and the mean length of the magnetic path as

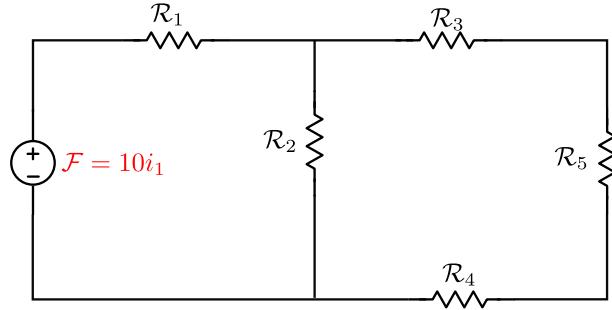
$$A_{c2} = 0.5 \text{ cm}^2; l_5 = 0.3 \text{ cm}$$

Thus, the reluctance can be calculated as

$$\mathcal{R}_5 = \frac{l_5}{\mu_r \mu_o A_c} = \frac{3 \times 10^{-2}}{10^3 \times 4\pi \times 10^{-7} \times 0.5 \times 10^{-4}} = 4.77 \times 10^5 H^{-1}$$

The magnetomotive force (MMF)= $\mathcal{F}=i_1 n_1 = 10i_1$

The equivalent magnetic circuit can now be drawn as shown below



The reluctance as seen from the MMF source is

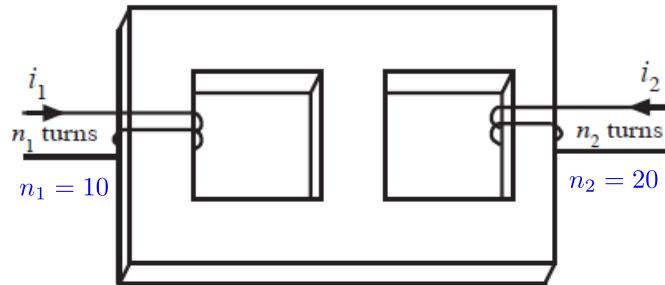
$$\mathcal{R}_{net} = \mathcal{R}_1 + \mathcal{R}_2 || (\mathcal{R}_3 + \mathcal{R}_4 + \mathcal{R}_5) = 9.07 \times 10^5 H^{-1}$$

The inductance of the winding can then be calculated as

$$L = \frac{n_1^2}{\mathcal{R}_{net}} = \frac{100}{9.07 \times 10^5} = 110 \mu H$$

**Question 4:**

A second winding is added to the same core described in Question 3. The new magnetic structure is illustrated in the figure below



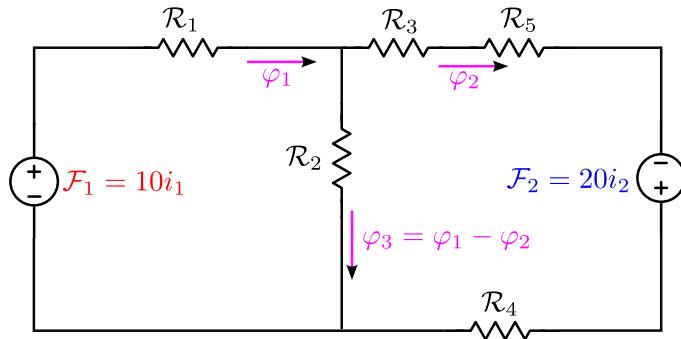
The electrical equations for this circuit may be written in the form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \end{bmatrix}$$

Find the value of  $L_{11}$  in  $\mu\text{H}$ .

Solution: Answer range (109-111)

On adding the second winding the magnetic circuit gets modified as shown in the figure below



From Faraday's law and the first line of the matrix equation we have

$$v_1 = n_1 \frac{d\varphi_1}{dt} = L_{11} \frac{di_1}{dt} + L_{12} \frac{di_2}{dt}$$

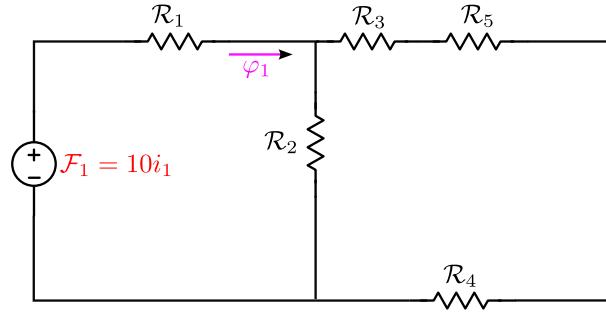
Thus, we have integrating both sides we get

$$\varphi_1 = \frac{L_{11}}{n_1} i_1 + \frac{L_{12}}{n_1} i_2$$

Thus, we have

$$L_{11} = \left. \frac{\varphi_1 n_1}{i_1} \right|_{i_2=0}$$

Now, if we make  $i_2 = 0$ , the magnetic circuit becomes



The reluctance as seen from the MMF source is

$$\mathcal{R}_{net} = \mathcal{R}_1 + \mathcal{R}_2 || (\mathcal{R}_3 + \mathcal{R}_4 + \mathcal{R}_5) = 9.07 \times 10^5 H^{-1}$$

Now, we can write

$$10i_1 = \mathcal{R}_{net} \times \varphi_1$$

Thus, we have

$$L_{11} = \frac{\varphi_1 n_1}{i_1} \Big|_{i_2=0} = \frac{10n_1}{\mathcal{R}_{net}} = \frac{100}{9.07 \times 10^5} = 110 \mu H$$

*Question 5:*

In continuation with Question 4, Find the value of  $L_{12}$  in  $\mu\text{H}$ .

Solution: Answer range (43.5 – 44.5)

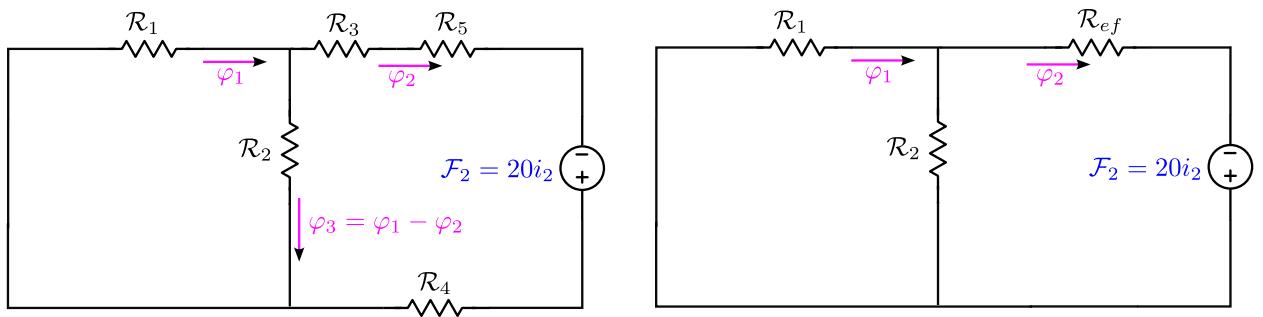
As discussed in the solution of Question 4

$$\varphi_1 = \frac{L_{11}}{n_1} i_1 + \frac{L_{12}}{n_1} i_2$$

Thus, we have

$$L_{12} = \left. \frac{\varphi_1 n_1}{i_2} \right|_{i_2=0}$$

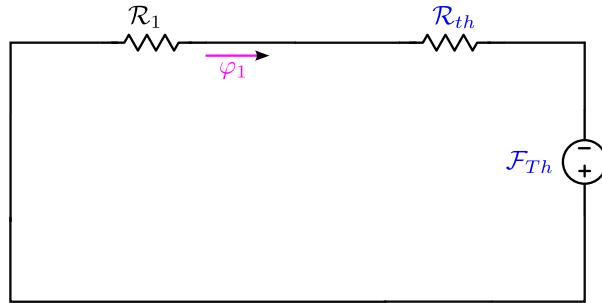
Now, if we make  $i_1 = 0$ , the magnetic circuit becomes



Where,

$$R_{ef} = R_3 + R_4 + R_5 = 9.55 \times 10^5 \text{ H}^{-1}$$

By applying Thevenin's theorem we can redraw the circuit as



Where,

$$R_{th} = \frac{R_{ef} \times R_2}{R_{ef} + R_2} = 1.91 \times 10^5 \text{ H}^{-1}$$

$$\mathcal{F}_{th} = \frac{R_2}{R_{ef} + R_2} \times \mathcal{F}_2 = 4i_2$$

Now,  $\varphi_1$  can be expressed as

$$\varphi_1 = \frac{\mathcal{F}_{th}}{\mathcal{R}_{th} + \mathcal{R}_1} = \frac{4i_2}{9.07 \times 10^5}$$

Thus, we now have

$$L_{12} = \left. \frac{\varphi_1 n_1}{i_2} \right|_{i_2=0} = \frac{4i_2}{9.07 \times 10^5} \times \frac{n_1}{i_2} = 44.1 \mu H$$

**Question 6:**

In continuation with Question 4, Find the value of  $L_{21}$  in  $\mu\text{H}$ .

Solution: Answer range (43.5 – 44.5)

From the second line of the matrix equation and Faraday's law we have

$$v_2 = n_2 \frac{d\varphi_2}{dt} = L_{21} \frac{di_1}{dt} + L_{22} \frac{di_2}{dt}$$

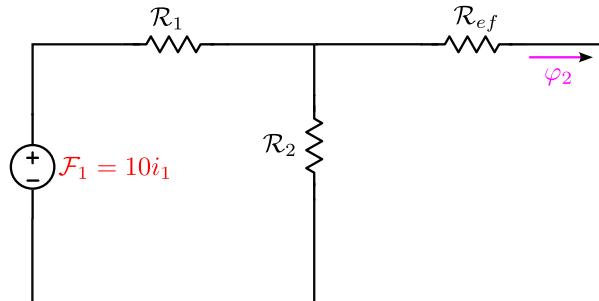
Thus, we have integrating both sides we get

$$\varphi_2 = \frac{L_{21}}{n_2} i_1 + \frac{L_{22}}{n_2} i_2$$

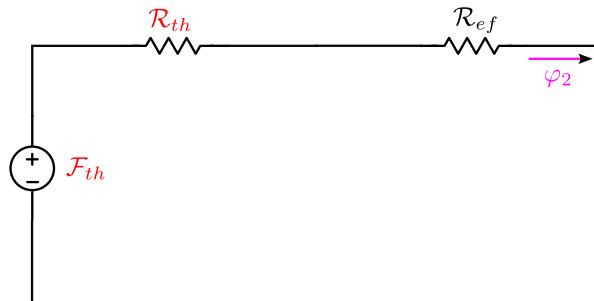
Thus, we have

$$L_{21} = \left. \frac{\varphi_2 n_2}{i_1} \right|_{i_2=0}$$

Now, if we make  $i_2 = 0$ , the magnetic circuit becomes



By applying Thevenin's theorem, the circuit can be redrawn as



Where,

$$R_{th} = \frac{R_1 \times R_2}{R_1 + R_2} = 1.79 \times 10^5 \text{ H}^{-1}$$

$$F_{th} = \frac{R_2}{R_1 + R_2} \times F_1 = 2.5i_1$$

Thus, we can calculate  $\varphi_2$  as

$$\varphi_2 = \frac{\mathcal{F}_{th}}{\mathcal{R}_{th} + \mathcal{R}_{ef}} = \frac{2.5i_1}{11.34 \times 10^5}$$

Thus, we can calculate  $L_{21}$  as

$$L_{21} = \left. \frac{\varphi_2 n_2}{i_1} \right|_{i_2=0} = \frac{2.5i_1}{11.34 \times 10^5} \times \frac{n_2}{i_1} = 44.09 \mu H$$

**Question 7:**

In continuation with Question 4, Find the value of  $L_{22}$  in  $\mu\text{H}$ .

Solution: Answer range (351-354)

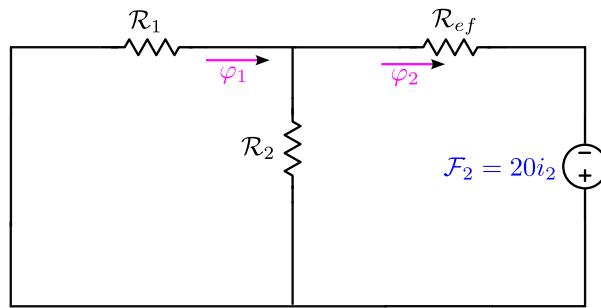
We have already seen in the solution to previous question that

$$\varphi_2 = \frac{L_{21}}{n_2} i_1 + \frac{L_{22}}{n_2} i_2$$

Thus, we have

$$L_{22} = \left. \frac{\varphi_2 n_2}{i_2} \right|_{i_1=0}$$

As we have already seen in the solution to Question 5, if we make  $i_1 = 0$ , the magnetic circuit becomes



The net reluctance as seen from the MMF source  $\mathcal{F}_2$  can be calculated as

$$\mathcal{R}_{net} = \mathcal{R}_{ef} + \mathcal{R}_1 || \mathcal{R}_2 = 11.34 \times 10^5 \text{ H}^{-1}$$

Thus, we can calculate  $\varphi_2$  as

$$\varphi_2 = \frac{\mathcal{F}_2}{\mathcal{R}_{net}} = \frac{20i_2}{11.34 \times 10^5}$$

Thus, we can calculate  $L_{22}$  as

$$L_{22} = \left. \frac{\varphi_2 n_2}{i_2} \right|_{i_1=0} = \frac{20i_2}{11.34 \times 10^5} \times \frac{n_2}{i_2} = 352.73 \mu\text{H}$$

*Question 8:*

The manufacturer's data sheet includes the plot for the core loss of the ferrite material as shown in the figure below. This plot passes through the points

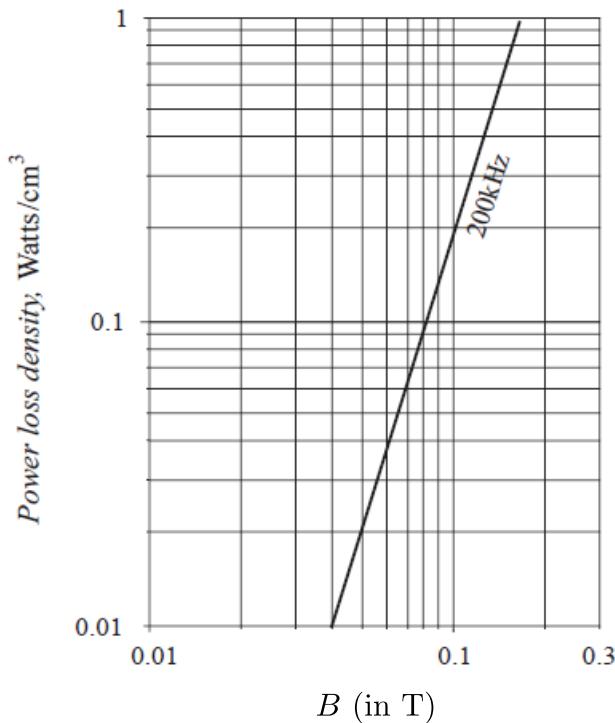
- $0.2 \text{ W/cm}^3$  at  $\Delta B = 0.1 \text{ T}$
- $0.01 \text{ W/cm}^3$  at  $\Delta B = 0.04 \text{ T}$

The Steinmetz empirical equation for the core loss at 200 kHz of the form

$$(\text{power loss density}) = K_{fe} B_{max}^\beta$$

where  $B_{max}$  is the peak sinusoidal flux density in Tesla and the power loss density is expressed in  $\text{W/cm}^3$ .

Find the numerical value of  $K_{fe}$  rounded off to two decimal places.



Solution: Answer range (370-372)

The Steinmetz equation is of the form

$$P = K_{fe} B^\beta$$

The curve given to us in the question is plotted in logarithmic scale. So, taking log on both sides we end up getting

$$\log P = \log K_{fe} + \beta \log B$$

Given that the curve passes through two points as

- $P_1 = 0.2 \text{ W/cm}^3$        $B_1 = 0.1 \text{ T}$
- $P_2 = 0.01 \text{ W/cm}^3$        $B_2 = 0.04 \text{ T}$

Putting these values in the above equation we get

$$\log P_1 = \log K_{fe} + \beta \log B_1$$

$$\log P_2 = \log K_{fe} + \beta \log B_2$$

Thus, we can express  $\beta$  from the above equation as

$$\beta = \frac{\log P_1 - \log K_{fe}}{\log B_1} = \frac{\log P_2 - \log K_{fe}}{\log B_2}$$

Solving the above equation, we can obtain the expression for  $\log K_{fe}$  as

$$\log K_{fe} = \left( \frac{\log P_1}{\log B_1} - \frac{\log P_2}{\log B_2} \right) \times \frac{\log B_1 \times \log B_2}{\log B_2 - \log B_1} = 2.57$$

Thus, we can obtain the value of

$$K_{fe} = 10^{2.57} = 371.91$$

*Question 9:*

*For the core loss data of Question 8, enter the numerical value of  $\beta$  (rounded off to two decimal places).*

Solution: Answer range (3.2-3.3)

As given in *Question 8*, the power loss curve passes through the point

- $P_1 = 0.2 \text{ W/cm}^3$        $B_1 = 0.1 \text{ T}$

In solution to *Question 8*, we have already obtained the value of  $K_{fe}$  as

$$K_{fe} = 371.91$$

Putting these values into Steinmetz equation we can write

$$P = K_{fe}B^\beta$$

Taking log on both sides we end up getting

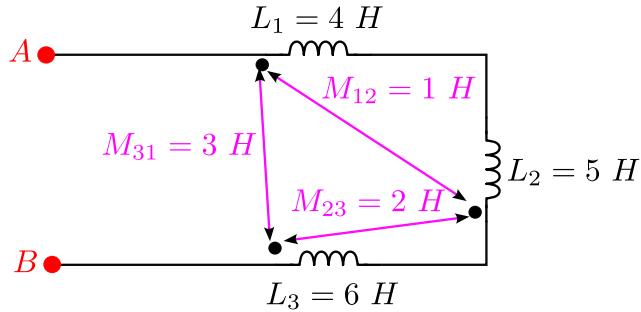
$$\log P_1 = \log K_{fe} + \beta \log B_1$$

Thus, the value of  $\beta$  can be obtained as

$$\beta = \frac{\log P_1 - \log K_{fe}}{\log B_1} = 3.27$$

*Question 10:*

The effective inductance of the circuit across the terminals  $A - B$  in the figure shown below is



- (a)  $9 \text{ H}$
- (b)  $21 \text{ H}$
- (c)  $11 \text{ H}$
- (d)  $6 \text{ H}$

Solution: **Correct option is (c)**

Apply KVL we can write

$$v_{AB} = \left( L_1 \frac{di_1}{dt} - M_{12} \frac{di_1}{dt} - M_{31} \frac{di_1}{dt} \right) + \left( L_2 \frac{di_1}{dt} - M_{12} \frac{di_1}{dt} + M_{23} \frac{di_1}{dt} \right) + \left( L_3 \frac{di_1}{dt} - M_{31} \frac{di_1}{dt} + M_{23} \frac{di_1}{dt} \right)$$

Thus, we can write the above equation as

$$v_{AB} = (L_1 + L_2 + L_3) \frac{di_1}{dt} + (2M_{23} - 2M_{12} - 2M_{31}) \frac{di_1}{dt}$$

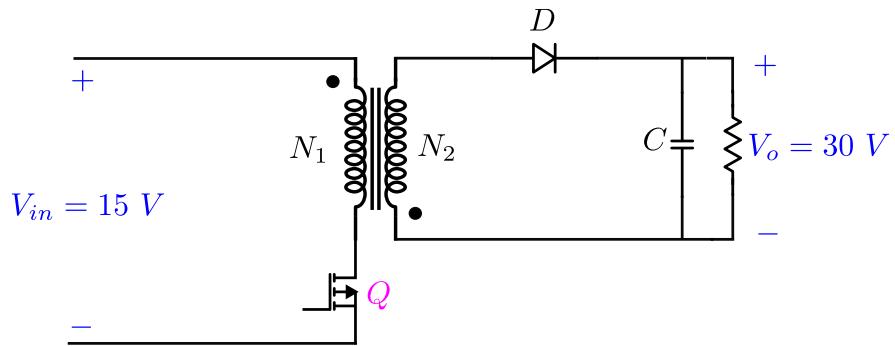
Thus, the equivalent inductance as seen from the terminals  $A - B$  is

$$L_{eq} = L_1 + L_2 + L_3 + 2M_{23} - 2M_{12} - 2M_{31} = 11 \text{ H}$$

*Question 1:*

In a flyback converter the switching frequency is 20 kHz with a duty cycle of 50%. The input voltage is 15 V and the output voltage is 30 V. The load current is 1 A. What is the voltage withstand capability of the primary side switch Q.

- (a) 15 V
- (b) 22.5 V
- (c) 30 V
- (d) 45 V



Solution: **Correct option is (c)**

To find the voltage stress across the switch  $Q$ , we need to calculate the voltage across the switch when it is off. The output voltage is assumed to be ripple free.

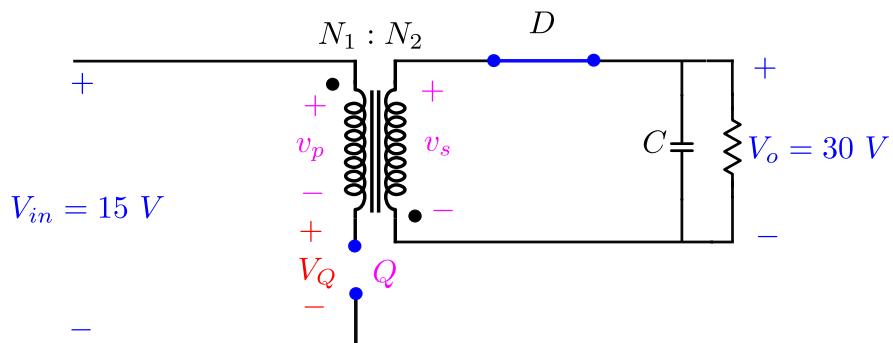
The input-output voltage relation is given as

$$V_o = \frac{N_2}{N_1} \frac{D}{1-D} V_{in}$$

Thus, we can calculate the turns ratio as

$$\frac{N_2}{N_1} = \frac{1-D}{D} \times \frac{V_o}{V_{in}} = 2$$

When the switch  $Q$  is off, the diode  $D$  is turned on. Thus, the circuit when the switch is off can becomes as shown below.



During this period,

$$v_s = 30 \text{ V}$$

Based on dot polarity we can write

$$v_p = -\frac{N_1}{N_2} \times v_s = -15 \text{ V}$$

Thus, the voltage across switch  $Q$  is

$$V_Q = V_{in} - v_p = 30 \text{ V}$$

*Question 2:*

*Which of the following statement is/are true regarding the flux walking phenomenon?*

*Statement 1: It cannot be observed in Full bridge converter.*

*Statement 2: It can cause saturation of the converter transformer.*

*Statement 3: Flux walking occurs because of volt-sec unbalance across the winding.*

*Statement 4: Flux walking problem can be solved by connecting a series inductance with the primary winding.*

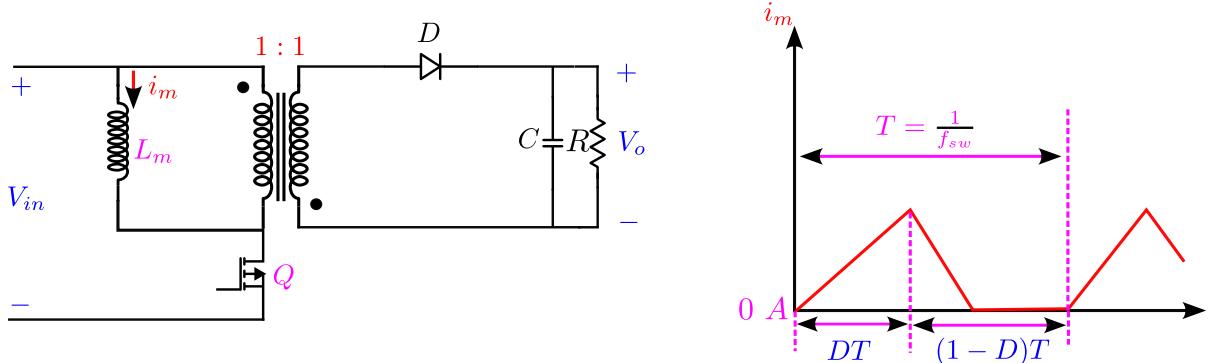
*Statement 5: Correcting the duty cycle in each PWM cycle can resolve the flux walking problem.*

- (a) Statement 2 and 5
- (b) Statement 1,2 and 5
- (c) Statement 2,4 and 5
- (d) Statement 2, 3 and 5

Solution: Correct option is (d)

*Question 3:*

A flyback converter with a turns-ratio of 1:1, has a magnetizing inductance of  $L_m$  and is operating at a frequency of  $f$  and duty cycle  $D$  supplying a load resistance  $R$ . The waveform of the magnetizing current is illustrated in the figure below. What will be the expression for voltage transfer ratio  $\frac{V_o}{V_{in}}$ .



- (a)  $\frac{V_o}{V_{in}} = \frac{D}{1-D}$
- (b)  $\frac{V_o}{V_{in}} = \frac{2D}{1-D}$
- (c)  $\frac{V_o}{V_{in}} = \sqrt{\frac{DR}{2fL_m}}$
- (d)  $\frac{V_o}{V_{in}} = D \sqrt{\frac{R}{2fL_m}}$

**Solution:** Correct option is (d)

When the switch  $Q$  is on, the voltage across the magnetizing inductance  $L_m$  is

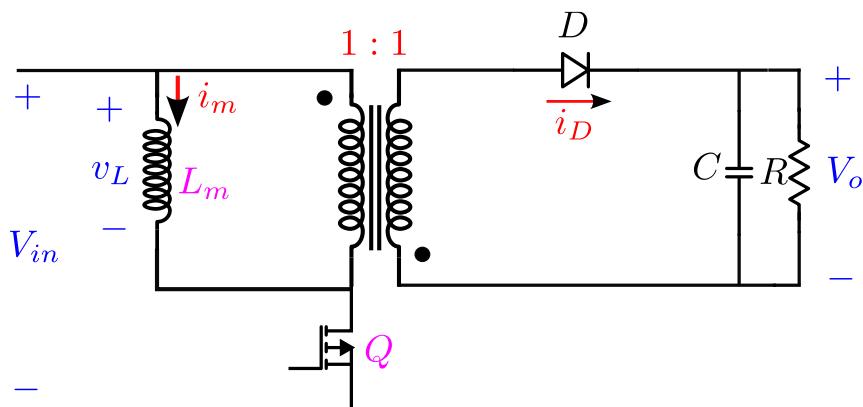
$$v_L = V_{in}$$

When the switch  $Q$  is off, and the magnetizing current  $i_m$  is non-zero, the voltage across  $L_m$  is

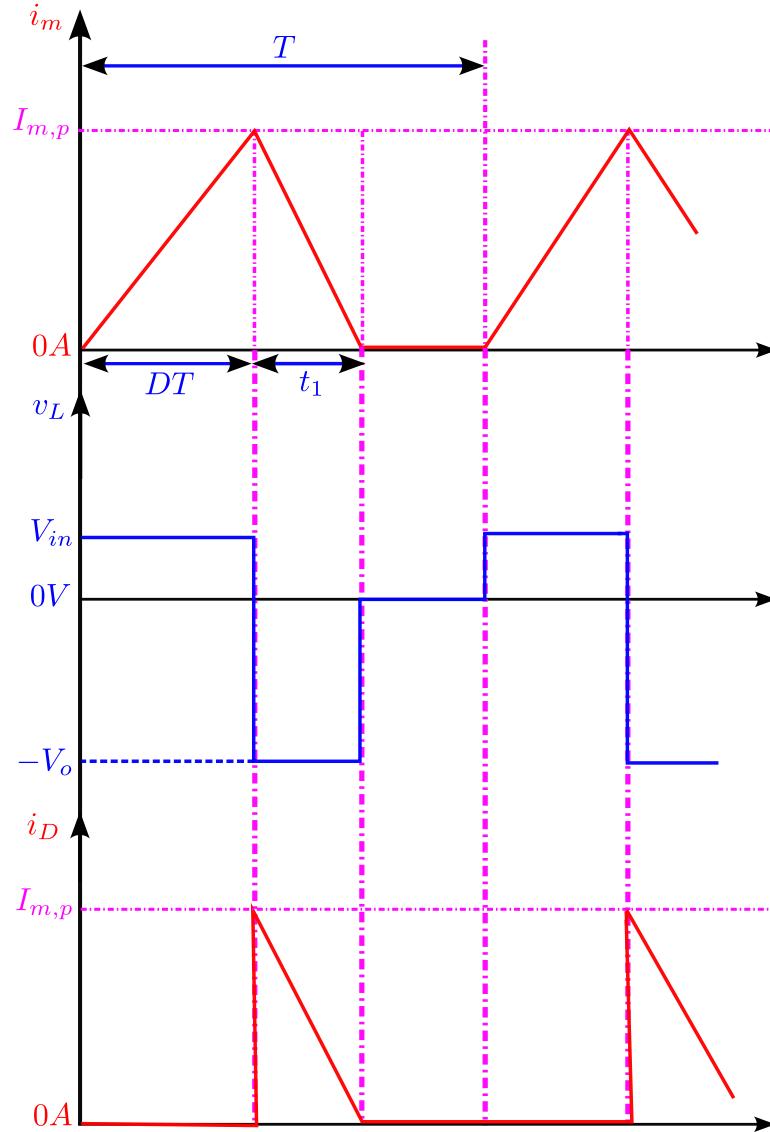
$$v_L = -V_o$$

When the switch  $Q$  is off, and the magnetizing current  $i_m$  is zero, the voltage across  $L_m$  is

$$v_L = 0$$



The waveform of the voltage  $v_L$  across the magnetizing inductance, diode current,  $i_D$ , and the magnetizing current,  $i_m$ , is illustrated in the figure below



During on period of the switch

$$v_L = V_{in} = L_m \frac{I_{m,p}}{DT}$$

Thus, we can write

$$I_{m,p} = \frac{V_{in}DT}{L_m}$$

We know that the load current flowing through  $R$  is the average value of the diode current,  $i_D$ . Thus, we can write

$$I_o = \frac{V_o}{R} = \frac{1}{2} \times t_1 \times I_{m,p} \times \frac{1}{T} = \frac{1}{2} \times t_1 \times \frac{V_{in}DT}{L_m} \times \frac{1}{T}$$

From the above equation we can obtain the value of  $t_1$  as

$$t_1 = \frac{2V_o L_m}{DRV_{in}}$$

Applying volt-second balance across the magnetizing inductance  $L_m$  we can write

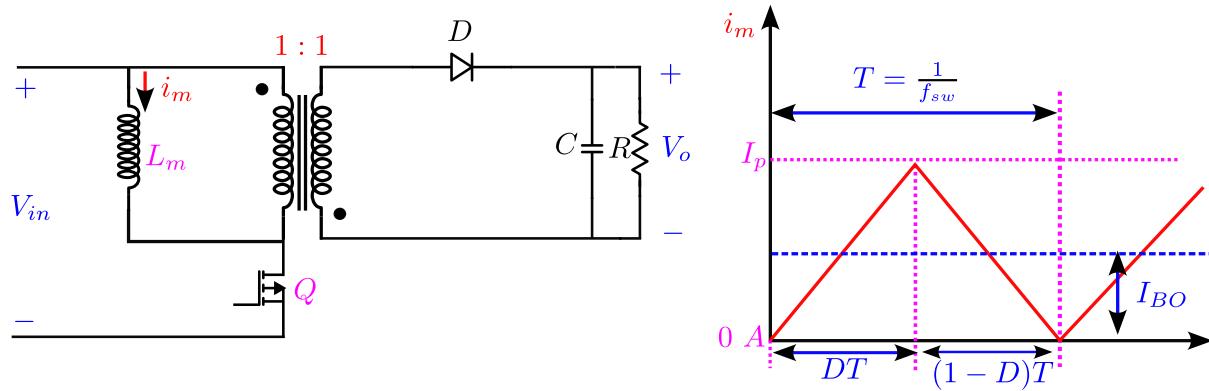
$$V_{in}DT - V_o t_1 = 0$$

Substituting the expression for  $t_1$  we can obtain the expression for voltage gain as

$$\frac{V_o}{V_{in}} = D \sqrt{\frac{R}{2f_{sw}L_m}}$$

**Question 4:**

In a regulated flyback converter with a turns ratio of 1:1,  $V_o = 12 V$ ,  $V_{in}$  ranging from 12 to 24 V,  $P_{load}$  is ranging from 6 to 60 W, and the switching frequency,  $f_{sw} = 200 \text{ kHz}$ . Calculate the maximum value of magnetizing inductance  $L_m$  (in  $\mu\text{H}$ ) that can be used such that the average value of the magnetization current is always below  $I_{BO}$  under all conditions. Assume the components to be ideal.



[Hint: Identify the condition at which  $i_m$  will attain its maximum value and do the necessary calculations]

Solution: Answer range (1.1-1.8)

The average value of  $i_m$  should always remain below  $I_{BO}$  essentially mean that the magnetization current will always be discontinuous and will reach the boundary condition of continuous and discontinuous mode of operation when the load current reaches its maximum value or in other words the peak value of the magnetization current reaches its maximum value.

$I_p$  will reach its maximum value when the duty cycle,  $D$ , is maximum. The relation between duty cycle and the input output voltage of the flyback converter is given by

$$D = \frac{1}{1 + \frac{V_o}{V_{in}}}$$

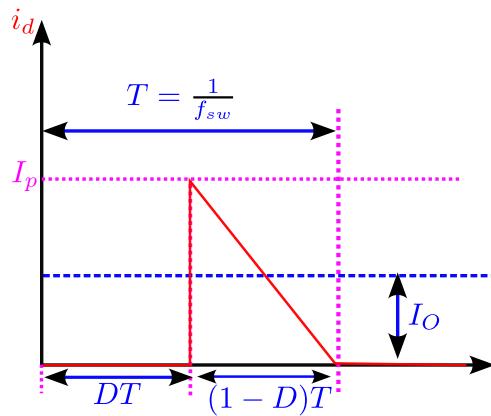
From the above expression, we can conclude that the duty cycle will be maximum if  $V_{in}$  is at its minimum value. Thus, we need to consider  $V_{in} = 12$ . In such a case the duty cycle is

$$D = \frac{1}{1 + \frac{12}{12}} = 0.5$$

Thus, the maximum value of the load current is

$$I_o = \frac{P_{load}}{V_o} = \frac{60}{12} = 5 \text{ A}$$

Now,  $I_o$  is the average value of the diode current. The waveform of the diode current is shown in the figure below



Thus, we can write  $I_o$  as

$$I_o = \frac{1}{2} \times (1 - D) \times I_p$$

Thus, the peak value of the load current can be calculated as

$$I_p = \frac{2I_o}{(1 - D)} = 20 \text{ A}$$

When the switch  $Q$  is on, the voltage across the magnetizing inductance,  $L_m$ , is

$$v_L = V_{in} = L_m \frac{I_p}{DT} = 12$$

Thus, the value of the magnetizing inductance,  $L_m$  is

$$L_m = \frac{v_L DT}{I_p} = \frac{12D}{I_p f_{sw}} = 1.5 \text{ } \mu\text{H}$$

*Question 5:*

A flyback converter (Converter A) shown in Fig. a is operating with a duty ratio of 0.5 such that the magnetizing current is continuous as shown in Fig. b. The magnetizing inductance of the converter is  $L_{m1}$ .

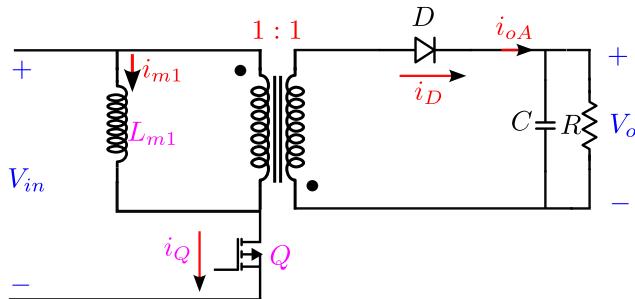


Fig. (a)

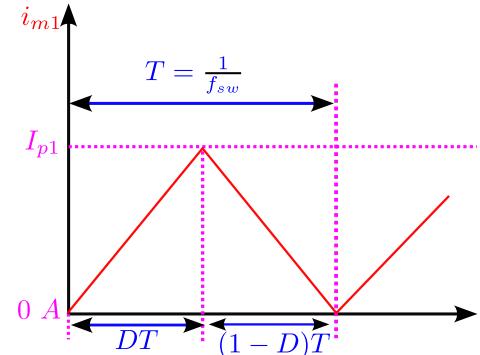


Fig. (b)

For the same application, to deliver same power to the load at same output voltage  $V_o$  another Converter B is designed by paralleling two half sized flyback converter as shown in Fig. c. Assume that both the flyback converters in Fig. c are sharing equal load. Then what would be the relationship between  $L_{m1}$  and  $L_{m2}$  such that the magnetizing current  $i_{m2}$  just reaches 0A at the end of each cycle. The switching signals of the switches  $Q_2$  and  $Q_3$  is illustrated in Fig. (d). All the switches  $Q_1$ ,  $Q_2$  and  $Q_3$  are operated at same frequency and same duty ratio.

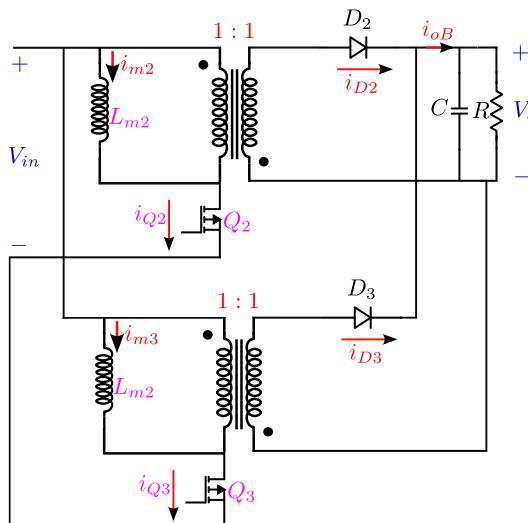


Fig. (c)

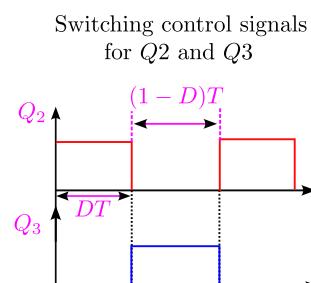
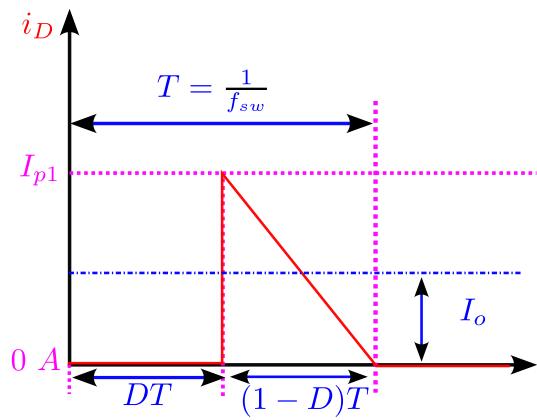


Fig. (d)

- (a)  $L_{m2} = 0.5 \times L_{m1}$
- (b)  $L_{m2} = 0.25 \times L_{m1}$
- (c)  $L_{m2} = 4 \times L_{m1}$
- (d)  $L_{m2} = 2 \times L_{m1}$

Solution: Correct option is (d)



For Converter A:

We can find the expression for  $I_{p1}$  as

$$I_{p1} = \frac{V_{in}DT}{L_{m1}}$$

We know that the average value of the diode current  $i_D$  is the load current  $I_o$ . The waveform of the diode current of Converter A is shown in the figure above. Thus, we can write

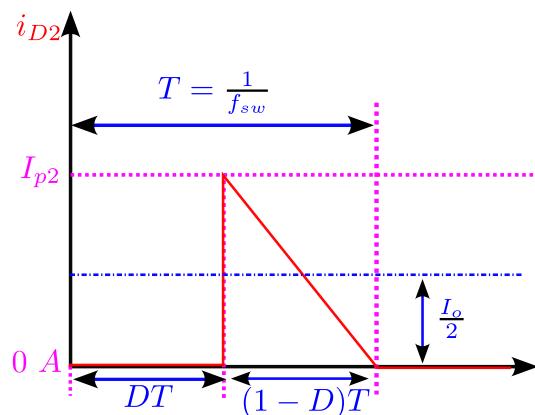
$$I_o = \frac{1}{2} \times (1 - D) \times I_{p1} = \frac{D(1 - D)}{2} \times \frac{V_{in}T}{L_{m1}}$$

For Converter B:

As the load is equally shared between the two parallel flyback converters, the average value of the diode current,  $i_{D2}$  must be equal to  $0.5 \times I_o$ . The expression for the peak value of magnetizing current  $i_{m2}$  can be written as

$$I_{p2} = \frac{V_{in}DT}{L_{m2}}$$

The waveform of the diode current  $i_{D2}$  is shown in the figure below



The expression for average value of  $i_{D2}$  can then be written as

$$\frac{I_o}{2} = \frac{1}{2} \times (1 - D) \times I_{p2} = \frac{D(1 - D)}{2} \times \frac{V_{in}T}{L_{m2}}$$

Thus, we have

$$\frac{D(1 - D)}{2} \times \frac{V_{in}T}{L_{m2}} = \frac{1}{2} \times \frac{D(1 - D)}{2} \times \frac{V_{in}T}{L_{m1}}$$

Thus, we can conclude that

$$L_{m2} = 2 \times L_{m1}$$

**Question 6:**

In continuation with Question 5, which of the following statement(s) is/are true for the output stage currents  $i_{oA}$  and  $i_{oB}$ .

Statement 1: Ripple frequency of  $i_{oB}$  is twice as that of the ripple frequency of  $i_{oA}$

Statement 2: Ripple frequency of  $i_{oB}$  is half as that of the ripple frequency of  $i_{oA}$

Statement 3: Peak ripple current of  $i_{oB}$  is one-third as that of the peak ripple current of  $i_{oA}$

Statement 4: Peak ripple current of  $i_{oB}$  is half as that of the peak ripple current of  $i_{oA}$

- (a) Only Statement 1 is correct
- (b) Statements 1 and 3 are correct
- (c) Statement 2 and 4 are correct
- (d) Only Statement 4 is correct

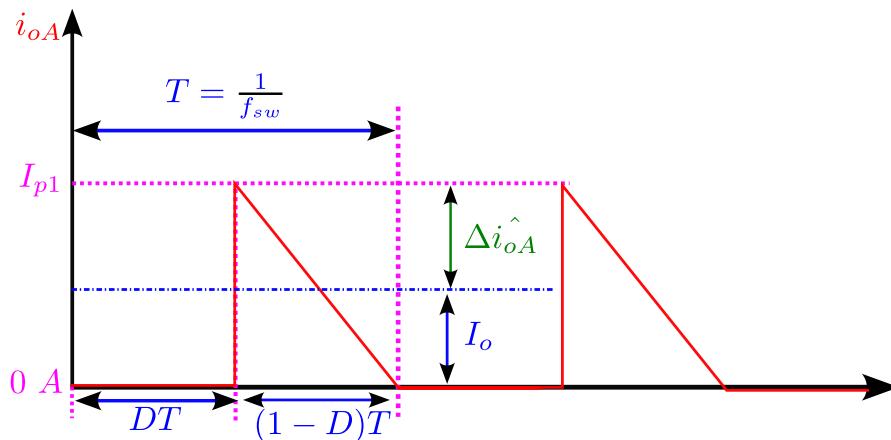
Solution: **Correct option is (b)**

For Converter A:

It can be concluded from the Fig. (a) of Question 5 that

$$i_D = i_{oA}$$

Thus, the waveform of the current  $i_{oA}$  is as shown in the figure below



The peak ripple current  $\Delta\hat{i}_{oA}$  can be calculated as

$$\Delta\hat{i}_{oA} = I_{p1} - I_o$$

The expressions for  $I_{p1}$  and  $I_o$  are already derived in the solution to Question 5. As mentioned in Question 5 the duty ratio,  $D = 0.5$ . Substituting the value of  $D = 0.5$  we can calculate  $\Delta\hat{i}_{oA}$  as

$$\Delta\hat{i}_{oA} = I_{p1} - I_o = \frac{3}{8} \times \frac{V_{in}T}{L_{m1}}$$

As seen from the waveform of  $i_{oA}$  the frequency of the output stage current  $i_{oA}$  is

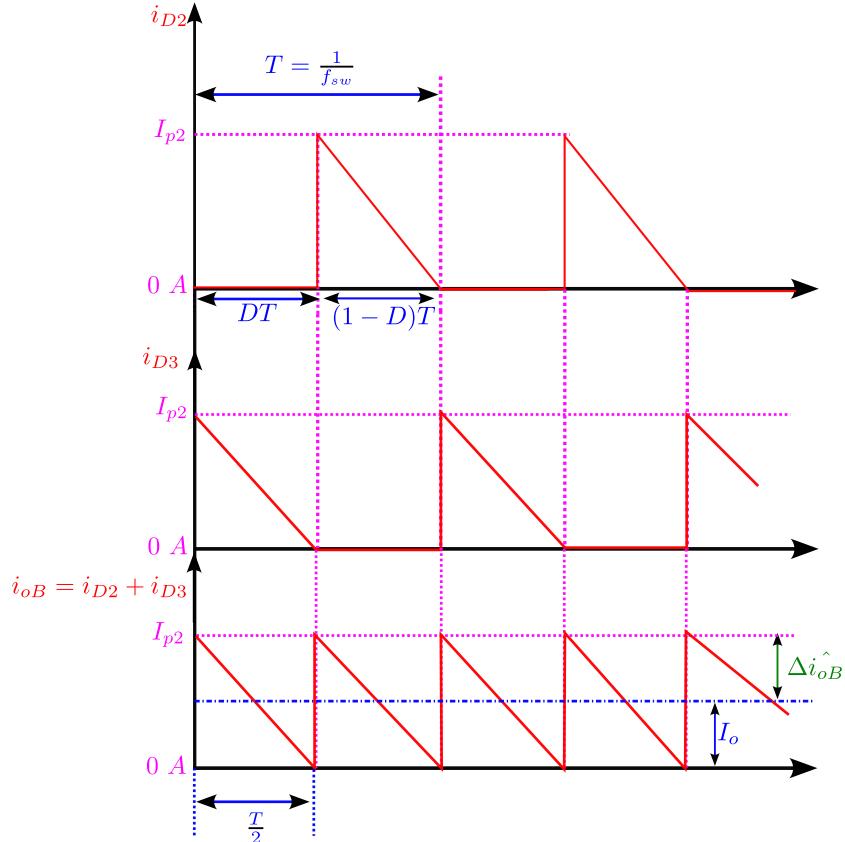
$$f_A = f_{sw} = \frac{1}{T}$$

For Converter B:

It can be concluded from the Fig. (c) of *Question 5* that

$$i_{oB} = i_{D2} + i_{D3}$$

The waveforms of  $i_{D2}$ ,  $i_{D3}$ , and  $i_{oB}$  is shown in the figure below



The peak ripple current  $\Delta i_{oB}$  can be calculated as

$$\Delta i_{oB} = I_{p2} - I_o$$

The expressions for  $I_{p2}$  and  $I_o$  are already derived in the solution to *Question 5*. As mentioned in *Question 5* the duty ratio,  $D = 0.5$ . Substituting the value of  $D = 0.5$  we can calculate  $\Delta i_{oB}$  as

$$\Delta i_{oB} = I_{p2} - I_o = \frac{1}{8} \times \frac{V_{in}T}{L_{m1}}$$

Thus, we have

$$\Delta i_{oB} = \frac{1}{3} \times \Delta i_{oA}$$

Again, as can be seen from the waveform of  $i_{oB}$ , the ripple frequency of  $i_{oB}$  is

$$f_B = \frac{2}{T} = 2f_{sw} = 2f_A$$

**Question 7:**

Consider two converters A and B. Converter A is a forward converter topology (shown in Fig. a) with demagnetizing winding. Converter B is a full bridge converter topology (shown in Fig. b). Both the converter has same values of input voltage source, turns ratio, switching frequency, output inductor and capacitor. The power switch of converter A is switched with a duty ratio twice that of converter B switches. What is the ratio of peak-to-peak inductor current ripple of converter A to that of converter B?

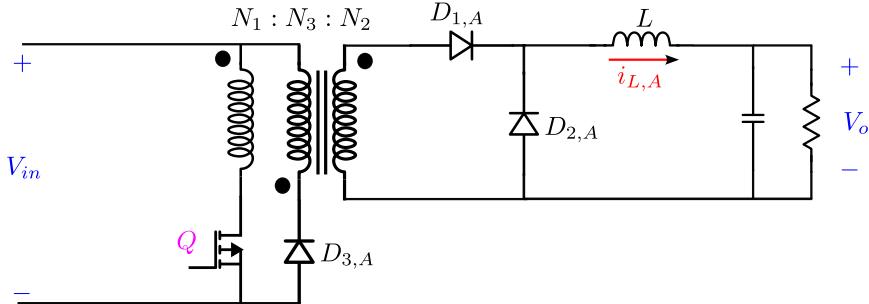


Fig. (a): Conveter A

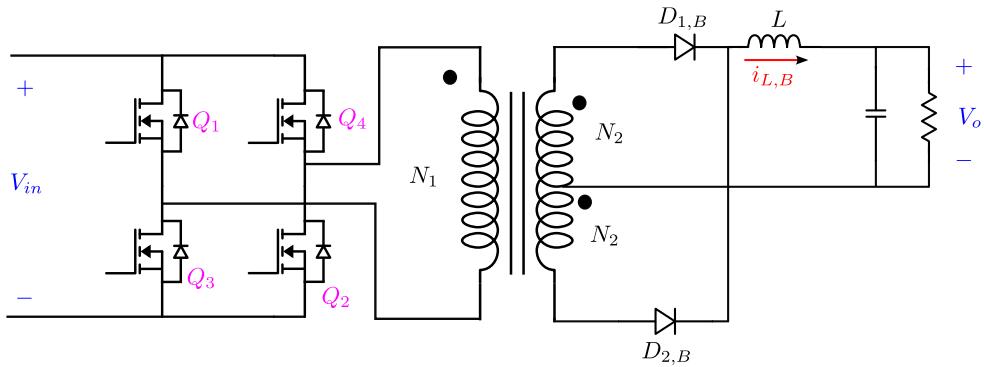


Fig. (b): Conveter B

Solution: Answer range (1.9-2)

For Converter A

The converter A is operating at a duty cycle given by

$$D_A = D$$

Thus, the output voltage of converter A is

$$V_o = \frac{N_2}{N_1} D_A V_{in} = \frac{N_2}{N_1} D V_{in}$$

During the period when switch  $Q$  is off, the voltage across the inductor is given by

$$v_{L,A} = -V_o = -L \frac{\Delta i_{L,A}}{(1-D)T}$$

Thus, the ripple inductor current in converter A can be expressed as

$$\Delta i_{L,A} = \frac{V_o(1-D)T}{L}$$

### For Converter B

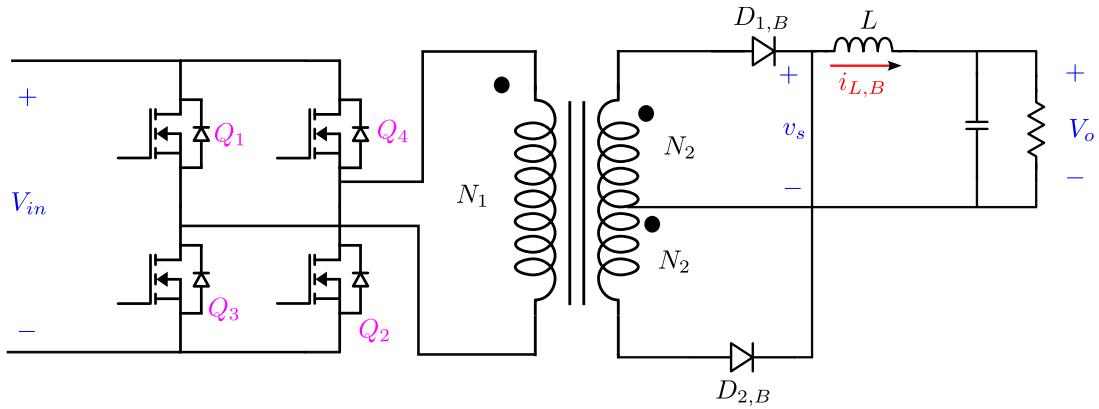
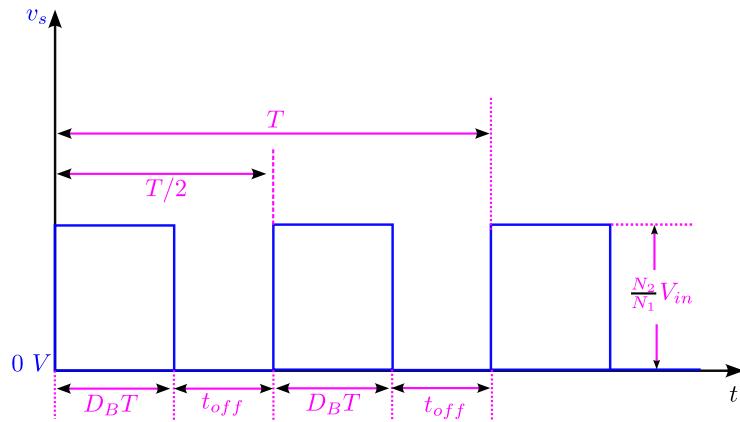


Fig. (b): Conveter B

The waveform for  $v_s$  will be as shown in the figure below



During the period  $t_{off}$  when both the diodes  $D_{1,B}$  and  $D_{2,B}$  are on the voltage across the inductor is

$$v_{L,B} = -V_o = -L \frac{\Delta i_{L,B}}{\left(\frac{T}{2} - D_B T\right)}$$

As has been given in the question

$$D_B = \frac{D_A}{2} = \frac{D}{2}$$

Thus, the equation becomes

$$V_o = L \frac{2\Delta i_{L,B}}{(1-D)T}$$

The expression for  $\Delta i_{L,B}$  is

$$\Delta i_{L,B} = \frac{V_o(1-D)T}{2L} = \frac{\Delta i_{L,A}}{2}$$

$$\frac{\Delta i_{L,A}}{\Delta i_{L,B}} = 2$$

*Question 8:*

*In continuation with Question 7, the Converter B is supplied from a unregulated DC voltage 100 to 150 V. A designer has switches of the voltage rating as given in the options. Which of the following voltage rating should the designer choose for safe operation of the converter.*

- (a) 25 V
- (b) 50 V
- (c) 100 V
- (d) 200 V

Solution: **Correct option is (d)**

The voltage appearing across an OFF switch in case of a full-bridge converter shown in *Question 7* is

$$V_{block} = V_{in}$$

The maximum voltage supplied by the unregulated power supply is

$$V_{in,max} = 150 \text{ V}$$

Taking a safety factor 1.3 a designed should choose a switch having a voltage blocking capability of 200 V.

*Question 9:*

*In continuation with Question 7 and 8, what should be the minimum voltage blocking capability of the diode  $D_{1,B}$  and  $D_{2,B}$  if the turns ratio of the centre-tapped transformer is 5 (2.5-0-2.5).*

- (a) 1000 V
- (b) 375 V
- (c) 750 V
- (d) 500 V

Solution: **Correct option is (c)**

The maximum voltage supplied by the unregulated power supply is

$$V_{in,max} = 150 \text{ V}$$

The voltage appearing across the diode  $D_{1,B}$  when the diode  $D_{2,B}$  is off is

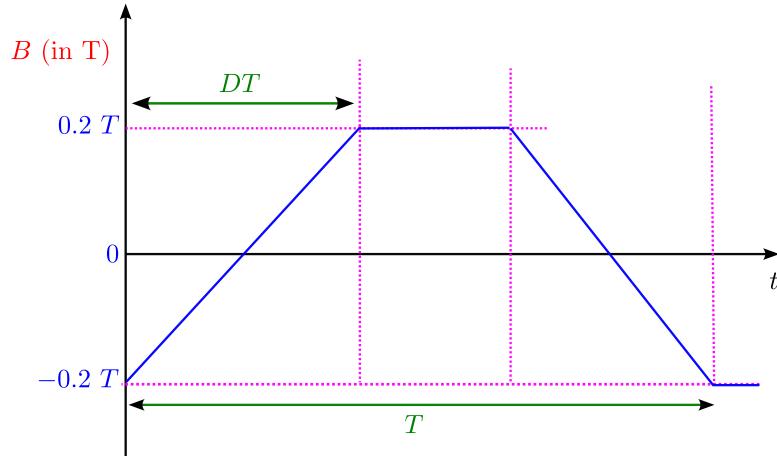
$$PIV = \frac{2N_2}{N_1} \times V_{in,max} = 5 \times 150 = 750 \text{ V}$$

*Question 10*

A full bridge converter has 1 turn primary and 100 turns secondary wound on a core with a  $25 \text{ mm}^2$  cross section. The core flux density is allowed to swing up to  $0.2 \text{ T}$ . The full bridge switches are switched at  $100 \text{ kHz}$  and  $50\%$  duty cycle. What is the output voltage of the converter (in Volts)?

Solution: Answer range (199-200)

The flux waveform for a full bridge converter is shown in the figure below



Now, by Faraday's Law we have

$$V_{in} = N_1 \frac{d\Phi}{dt} = N_1 A_c \frac{dB}{dt} = 1 \times 25 \times 10^{-6} \times \frac{0.4}{DT} = 25 \times 10^{-6} \times \frac{0.4 f_{sw}}{D} = 2 \text{ V}$$

The output voltage of the full bridge converter is given by

$$V_o = 2 \times \frac{N_2}{N_1} DV_{in} = 2 \times 100 \times 0.5 \times 2 = 200 \text{ V}$$

*Question 1:*

The schematic shown Fig. a represents a power BJT,  $Q_p$ , carrying collector current,  $I_o$ , of 15 A. A totem pole arrangement is used for driving  $Q_p$ . The base emitter drop of the power transistor,  $Q_p$ , and the drive transistors  $Q_{s1}$  and  $Q_{s2}$  are 0.8 V and 0.7 V respectively. The saturation current gain of all the BJTs is  $\beta_{sat} = 10$ . The gating signals are as shown in Fig. b.

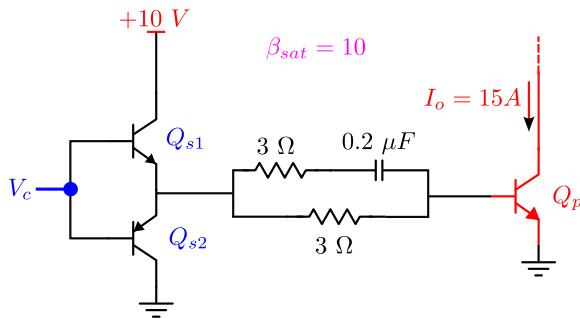


Fig. a

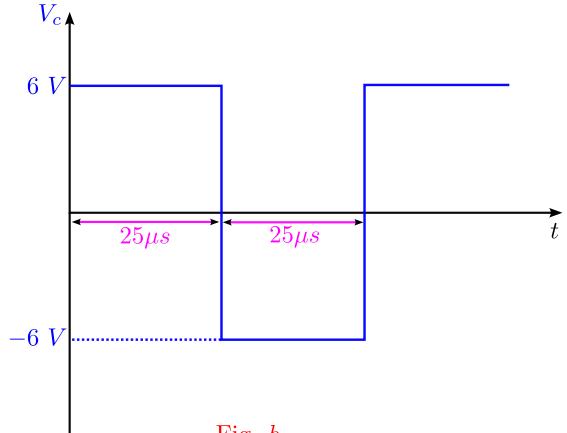


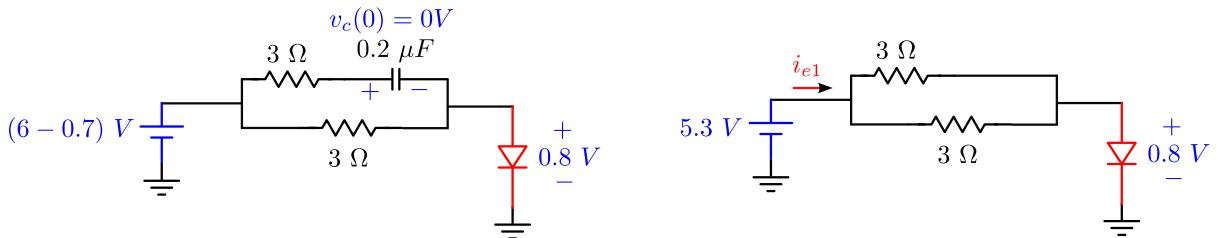
Fig. b

What will be the source and sink current of control input  $V_c$ . Assume the drive transistors to be in deep saturation.

- (a) 500 mA, 500mA
- (b) 500 mA, 928 mA
- (c) 928 mA, 500 mA
- (d) 928 mA, 928 mA

Solution: Correct option is (b)

To find the source current capability of the control input  $V_c$  we need to draw the equivalent circuit when  $V_c = 6V$ . During this period  $Q_{s1}$  is on. Thus, the equivalent circuit is as shown below



The capacitor is replaced by a short circuit as it is initially relaxed.

Thus, the emitter current of the switch  $Q_{s1}$ , represented as  $i_{e1}$  can be calculated as

$$i_{e1} = \frac{5.3 - 0.8}{1.5} A = 3 A$$

Now, if the designer chooses the drive transistor to be in deep saturation then

$$i_{e1} = i_{b1} + i_{c1} = i_{c1} \left( \frac{2}{\beta_{sat}} + 1 \right) = 1.2 \times i_{c1}$$

Thus, the collector current of the drive switch  $Q_{s1}$  is

$$i_{c1} = \frac{i_{e1}}{1.2} = 2.5 A$$

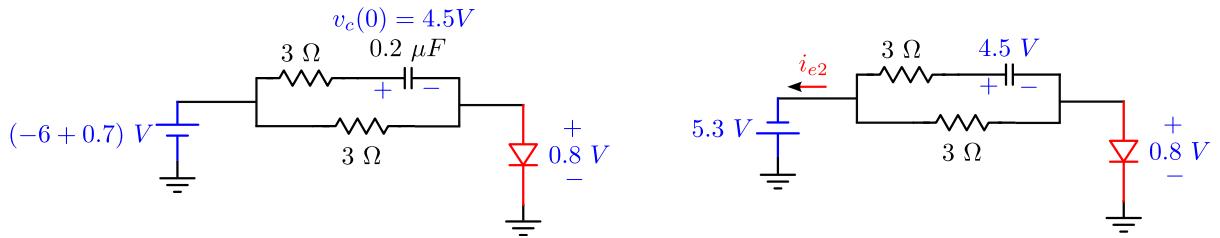
The base current of  $Q_{s1}$  is thus calculated as

$$i_{b1} = \frac{2i_{c1}}{\beta_{sat}} = 500 \text{ mA}$$

This current must be sourced from the control input  $V_c$ .

At the end of the positive half cycle of  $V_c$ , the capacitor is charged to a value  $v_c = 5.3 - 0.8 = 4.5 \text{ V}$ .

To find the sink current capability of the control input  $V_c$  we need to draw the equivalent circuit when  $V_c = -6\text{V}$ . During this period  $Q_{s2}$  is on. Thus, the equivalent circuit is as shown below



The stored charge in the depletion layer of the emitter base junction of the BJT is being removed during this period and hence the equivalent diode in the figure above is shown to carry current in the opposite direction.

Thus, the emitter current of the drive switch  $Q_{s2}$ , represented as  $i_{e2}$  can be calculated as

$$i_{e2} = \left( \frac{5.3 + 0.8}{3} + \frac{5.3 + 4.5 + 0.8}{3} \right) A = 5.567 \text{ A}$$

Thus, the collector current of drive switch  $Q_{s2}$  can be calculated as

$$i_{c2} = \frac{i_{e2}}{1.2} = 4.64 \text{ A}$$

The base current of  $Q_{s2}$  is thus calculated as

$$i_{b2} = \frac{2i_{c2}}{\beta_{sat}} = 928 \text{ mA}$$

This current must be sunked into the ground of the control input  $V_c$ .

*Question 2:*

*In continuation to Question 1, what will be the source and sink current of the drive power source.*

- (a) 2.5 A, 2.5 A
- (b) 4.64 A, 4.64 A
- (c) 4.64 A, 2.5 A
- (d) 2.5 A, 4.64 A

**Solution: Correct option is (d)**

We have already calculated the collector current flowing through the drive switch  $Q_{s1}$  during the positive half cycle of the control input  $V_c$  as given below

$$i_{c1} = \frac{i_{e1}}{1.2} = 2.5 \text{ A}$$

This current is being sourced from the drive power supply. Thus, the source current of the drive power supply is 2.5 A.

Similarly, during the negative half cycle of  $V_c$ , we have calculated the collector current flowing through the drive  $Q_{s2}$  as given below

$$i_{c2} = \frac{i_{e2}}{1.2} = 4.64 \text{ A}$$

This current must be sunk into the ground of the drive power supply. Thus, the sink current capability of the drive power supply must be 4.64 A.

*Question 3:*

A drive IC, shown in Fig. b, is capable of sinking and sourcing 1 A and is used to drive a MOSFET switch. The capacitance formed between the three terminals of the MOSFET switch and the threshold voltage is as below

$$C_{GS} = 1000 \text{ pF}, C_{DS} = 200 \text{ pF}, C_{GD} = 200 \text{ pF}, V_{th} = 4 \text{ V}$$

Find the value of  $R_g$  (in  $\Omega$ ) such that  $V_{GS}$  on turn-on reaches 10 V within 500 ns.

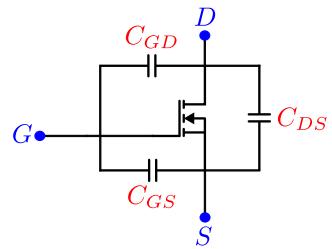


Fig. a

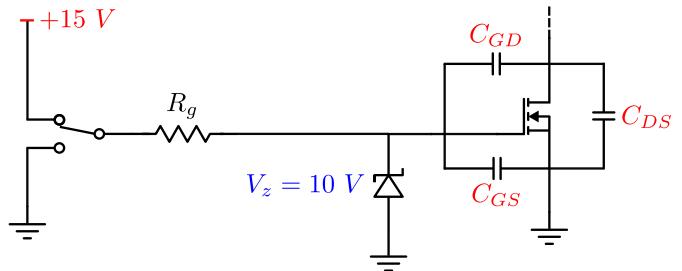
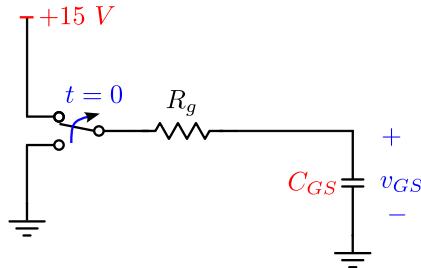


Fig. b

Solution: Answer range (454-456)

The equivalent circuit when the gate to source capacitance of the MOSFET is being charged is shown in the figure below



The equation for the voltage across the gate to source capacitance can be written as

$$v_{GS}(t) = 15 \left( 1 - e^{-\frac{t}{R_g C_{GS}}} \right)$$

$v_{GS}$  reaches 10 V in 500 ns, thus from the above equation we have

$$10 = 15 \left( 1 - e^{-\frac{500 \times 10^{-9}}{R_g C_{GS}}} \right)$$

Solving the above equation we have

$$R_g = \frac{500 \times 10^{-9}}{C_{GS} \ln(3)} = 455.12 \Omega$$

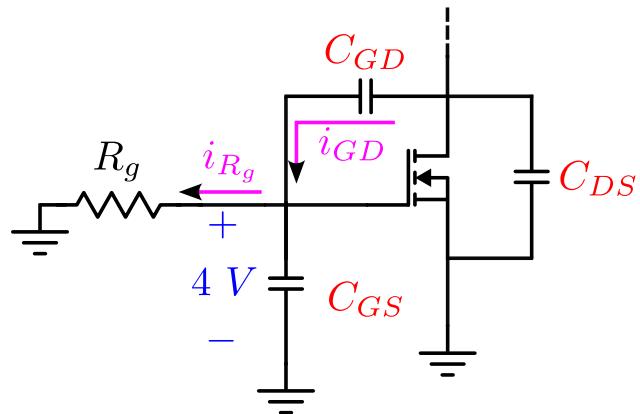
**Question 4:**

In continuation with Question 3, find the maximum off-time  $dV_{DS}/dt$  noise margin (in V/ $\mu$ s) that the MOSFET can withstand with the value of  $R_g$  calculated in Question 3.

Solution: Answer range (43-45)

We know that, the MOSFET starts conducting when  $V_{GS}$  is  $\geq V_{th}$

To find the maximum  $dV_{DS}/dt$ , let us consider a limiting condition where the gate to source capacitance is already charged to  $V_{th} = 4$  V and stays put at  $V_{th}$ . The equivalent circuit will then appear as shown in the figure below



As we are considering a condition where the gate to source voltage,  $v_{GS}$ , is fixed at 4 V, no current will be flowing through the capacitor  $C_{GS}$  as  $\frac{dv_{GS}}{dt} = 0$ .

Thus, applying KCL we can write,

$$C_{GD} \frac{dv_{GD}}{dt} = \frac{4}{R_g}$$

Where,  $v_{GD}$  is the gate to drain voltage. Now, as we have considered a case where  $v_{GS}$  stays put at 4 V

$$\frac{dv_{GD}}{dt} = \frac{dv_{DS}}{dt}$$

Since  $v_{DS} = v_{GD} + v_{GS}$ ,

Thus, the maximum value of  $dV_{DS}/dt$  that the MOSFET can withstand during its off-time is

$$\frac{dv_{DS}}{dt} = \frac{4}{R_g C_{GD}} = 43.94 \text{ V}/\mu\text{s}$$

**Question 5:**

The drive circuit shown in Fig. a is used to control the power transistor switch  $Q_p$ . The device  $Q_p$  requires appropriate continuous positive base current during ON time and transient negative base current of at least 1.5 A for at least 2  $\mu s$  during OFF time. The nature of base current during off time is shown in Fig. b. Evaluate the value of  $R_1$  (in  $\Omega$ ). (Assume the power transistor to be in deep saturation and  $V_{BE,sat} = 0V$ ).

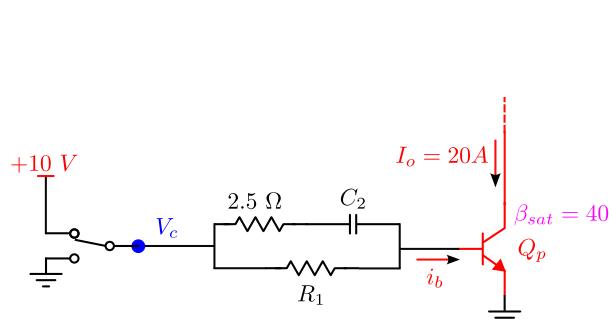


Fig. a

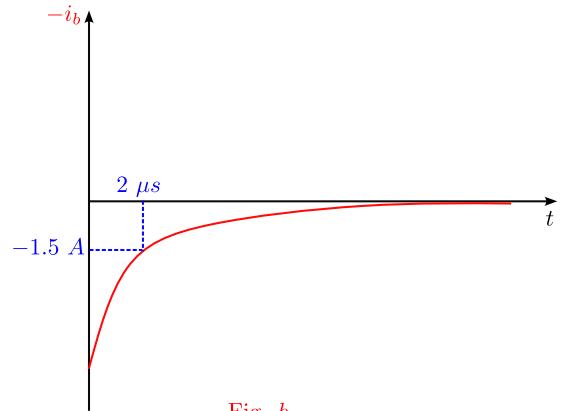


Fig. b

Solution: Answer range (10-12)

The transistor is carrying a collector current,  $I_c = 20 A$

As the power transistor is in deep saturation the base current can be calculated as

$$I_b = \frac{2 \times I_c}{\beta_{sat}} = 1 A$$

This is the least value of base current that must always be supplied to the base of  $Q_p$ .

Once the capacitor  $C_2$  is fully charged no current flows through  $2.5 \Omega$ . Thus, 1 A current will be flowing through  $R_1$ . Thus, the value of  $R_1$  can be calculated as

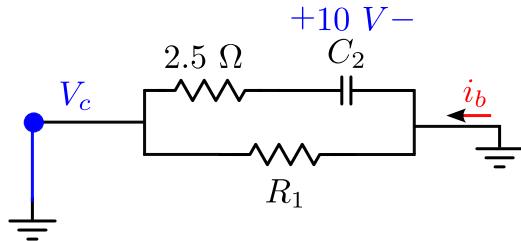
$$R_1 = \frac{V_c}{I_b} = 10 \Omega$$

**Question 6**

In continuation with Question 5, evaluate the value of  $C_2$  (in  $\mu F$ ).

Solution: Answer range (0.8-0.9)

At the start of the off period the capacitor is charged to 10 V. Thus, the equivalent circuit can be drawn as



The direction of the base current  $i_b$  during off period is as indicated in the figure above. The equation for  $i_b$  can then be written as

$$i_b(t) = \frac{10}{2.5} e^{-\frac{t}{2.5 \times C_2}}$$

As mentioned in Question 5,  $i_b(t)$  should be at least 1.5 A for 2  $\mu s$ , thus the waveform of  $i_b(t)$  should be as shown in Fig. b of Question 5. Thus, equating the values we get

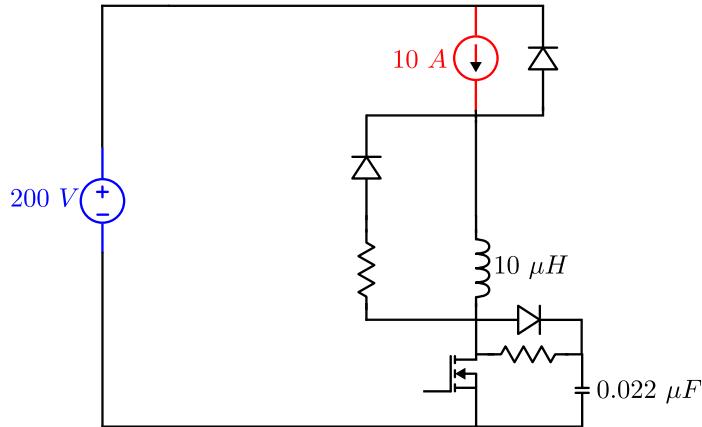
$$1.5 = \frac{10}{2.5} e^{-\frac{2 \times 10^{-6}}{2.5 \times C_2}}$$

Thus, the value of  $C_2$  can be calculated as

$$C_2 = \frac{2 \times 10^{-6}}{2.5 \times \ln \frac{4}{1.5}} = 0.8156 \mu F$$

**Question 7:**

The circuit shown below is a chopper operating at 10 kHz. Evaluate the switching losses in the snubber of the circuit (in Watts).



Solution: Answer range : (9.3-9.5)

Turn on snubber:

Energy stored in the inductor of turn on snubber circuit is

$$E_{on-snub} = \frac{1}{2} \times 10 \times 10^{-6} \times 10^2 = 0.5 \text{ mJ}$$

Thus, the power dissipated by the turn-on snubber circuit is

$$P_{on-snub} = E_{on-snub} \times f = 5W$$

This power will be dissipated in the resistor of the turn-on snubber circuit when the MOSFET is turned off.

Turn off snubber:

The voltage across the MOSFET when it is turned off is 200 V.

Energy stored in the capacitor of turn off snubber circuit is

$$E_{off-snub} = \frac{1}{2} \times 0.022 \times 10^{-6} \times 200^2 = 0.44 \text{ mJ}$$

Thus, the power dissipated by the turn-off snubber circuit is

$$P_{off-snub} = E_{off-snub} \times f = 4.4 W$$

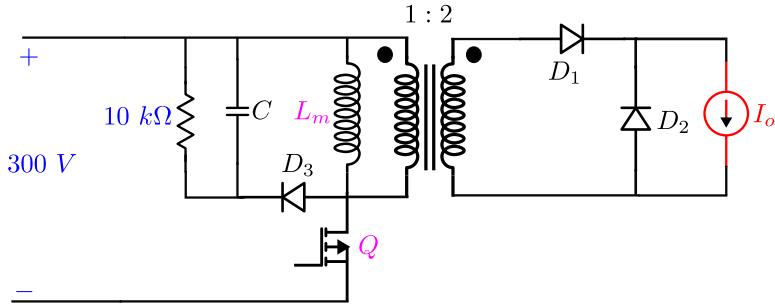
This power will be dissipated in the resistor of the turn-off snubber circuit when the MOSFET is turned on.

Thus, total power loss in the snubber circuit is

$$P_{snub} = P_{on-snub} + P_{off-snub} = 9.4 W$$

**Question 8:**

The circuit shown below is a forward converter operating with a duty ratio of 50% and a switching frequency of 40 kHz. The magnetizing inductance ( $L_m$ ) of the isolation transformer is found to be 20 mH. Evaluate the losses in the snubber circuit in watts and rms value of the capacitor voltage.



- (a) 15 W, Not possible to calculate capacitor voltage due to data insufficiency.
- (b) 18 W, 300 V
- (c) 14.06 W, 300 V
- (d) 14.06 W, 374.96 V

Solution: Correct option is (d)

The peak value of the magnetizing current when the MOSFET  $Q$  is on can be calculated as

$$I_m = \frac{V_{in}DT}{L_m} = 0.1875 \text{ A}$$

Thus, the energy stored in the magnetizing inductor can be calculated as

$$E_m = \frac{1}{2} \times L_m \times I_m^2 = 351.56 \mu\text{J}$$

This power needs to be dissipated in the snubber resistor every cycle to reset the flux in the core. Thus, the power dissipated every cycle is

$$P_{snub} = 351.56 \times 10^{-6} \times f = 14.06 \text{ W}$$

The power is dissipated in the resistor and thus we can write

$$P_{snub} = \frac{V_{C,rms}^2}{R}$$

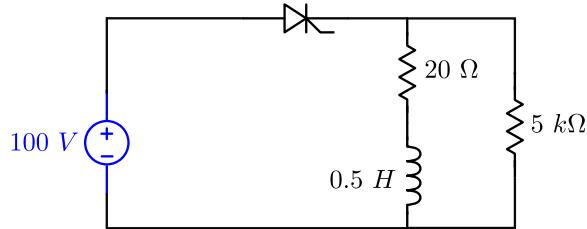
Thus, rms value of the capacitor voltage can be calculated as

$$V_{C,rms} = \sqrt{P_{snub} \times R} = 374.96 \text{ V}$$

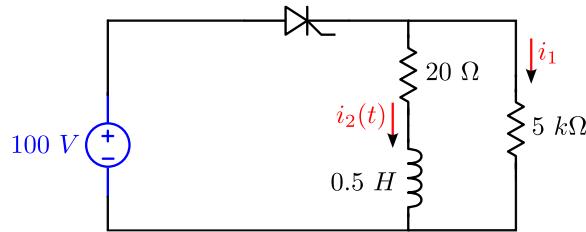
*Question 9:*

A thyristor having a turn on time of 5  $\mu s$ , latching current of 50 mA and a holding current of 40 mA is triggered by a short duration pulse and is used in the circuit shown below. The minimum pulse width required to turn the thyristor on will be

- (a) 251  $\mu s$
- (b) 150  $\mu s$
- (c) 100  $\mu s$
- (d) 5  $\mu s$



**Solution:** Correct option is (b).



When positive pulse is applied to the gate of the thyristor, current through the thyristor starts increasing. Now, we can calculate  $i_1$  as

$$i_1 = \frac{100}{5k} = 20 \text{ mA}$$

Now, the current through thyristor should reach the value of latching current when positive pulse is applied to the gate of thyristor. Thus,  $i_2$  must reach the value of 30 mA when gating signal is positive. The equation for the current  $i_2(t)$  can be written as

$$i_2(t) = 5 \left( 1 - e^{-\frac{R}{L}t} \right) = 5 \left( 1 - e^{-\frac{20}{0.5}t} \right) = 5(1 - e^{-40t})$$

Now, the time required for  $i_2(t)$  to reach 30 mA can be calculated by solving the following equation

$$30 \times 10^{-3} = 5(1 - e^{-40t})$$

Thus, we can calculate the time required as

$$t = 150 \mu s$$

*Question 10*

The circuit schematic given in Fig. a shows a step-down chopper with no snubber circuit connected across the switches. The diode has a stored inductance of  $5 \text{ nH}$  and a device capacitance of  $100 \text{ pF}$ . The diode current waveform is shown in Fig. b. Find the peak voltage that appears across the diode, when the switch Q is turned on.

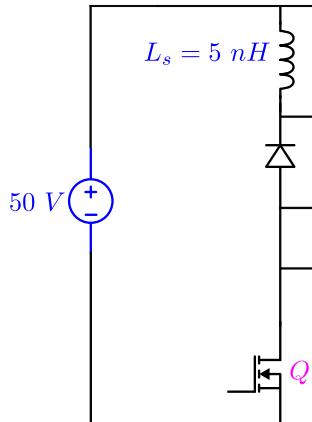


Fig. a

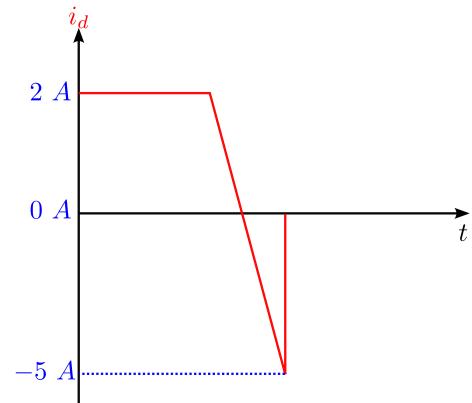


Fig. b

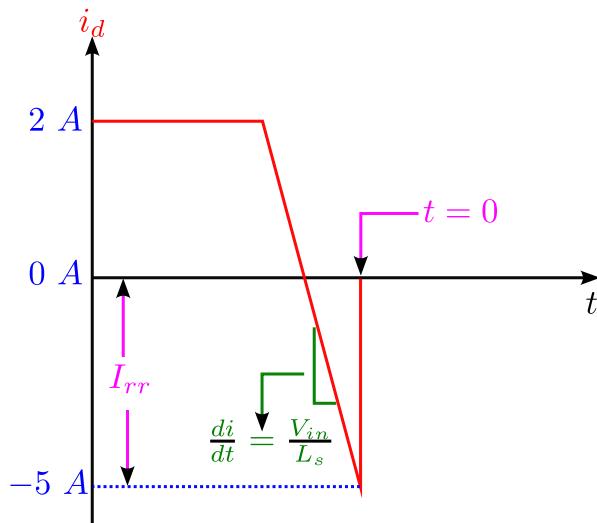
- (a) 100.24 V
- (b) 151.24 V
- (c) 211 V
- (d) 111.24 V

Solution: **Correct option is (d)**

From Fig. b of the question we can conclude that the diode snaps off abruptly when the current through the diode reaches its reverse recovery current

$$I_{rr} = 5 \text{ A}$$

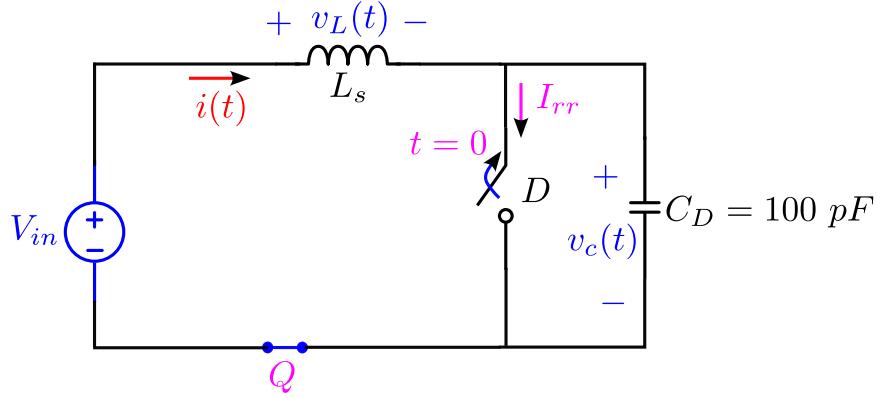
We will consider this instant as our time origin for our subsequent analysis.



Thus, at  $t = 0$ , the diode snaps off and the MOSFET is conducting. For analysing the circuit for  $t > 0$ , we thus have the following initial conditions

$$i(t = 0) = I_{rr} \quad \text{and} \quad \frac{di}{dt}(t = 0) = \frac{V_{in}}{L}$$

The equivalent circuit for  $t \geq 0$  s can then be drawn as



The differential equation governing the stray inductor current can be written as

$$L_s \frac{d^2 i}{dt^2} + \frac{i}{C_D} = 0$$

Taking Laplace transform we can write

$$L_s \left( s^2 I(s) - s I_{rr} - \frac{V_{in}}{L_s} \right) + \frac{I(s)}{C_D} = 0$$

Solving for  $I(s)$  we get

$$I(s) = I_{rr} \frac{s}{s^2 + \frac{1}{L_s C_D}} + V_{in} \times \sqrt{\frac{C_D}{L_s}} \times \frac{1}{s^2 + \frac{1}{L_s C_D}}$$

Taking inverse Laplace transform we can write

$$i(t) = I_{rr} \cos(\omega_o t) + \frac{V_{in}}{Z_o} \sin(\omega_o t)$$

Where,

$$\omega_o = \frac{1}{\sqrt{L_s C_D}} \quad \text{and} \quad Z_o = \sqrt{\frac{L_s}{C_D}}$$

Thus, the voltage across the stray inductance can be calculated as

$$v_L(t) = V_{in} \cos(\omega_o t) - I_{rr} \sqrt{\frac{L_s}{C_D}} \sin(\omega_o t)$$

Thus, the equation for voltage across the diode is

$$v_c(t) = V_{in} - V_{in} \cos(\omega_o t) + I_{rr} \sqrt{\frac{L_s}{C_D}} \sin(\omega_o t)$$

Substituting the corresponding values, we can write

$$v_c(t) = 50 - 50 \cos(\omega_o t) + 35.35 \sin(\omega_o t)$$

The maximum value of the above expression is

$$V_{pk} = 50 + \sqrt{50^2 + 35.35^2} = 111.24 V$$