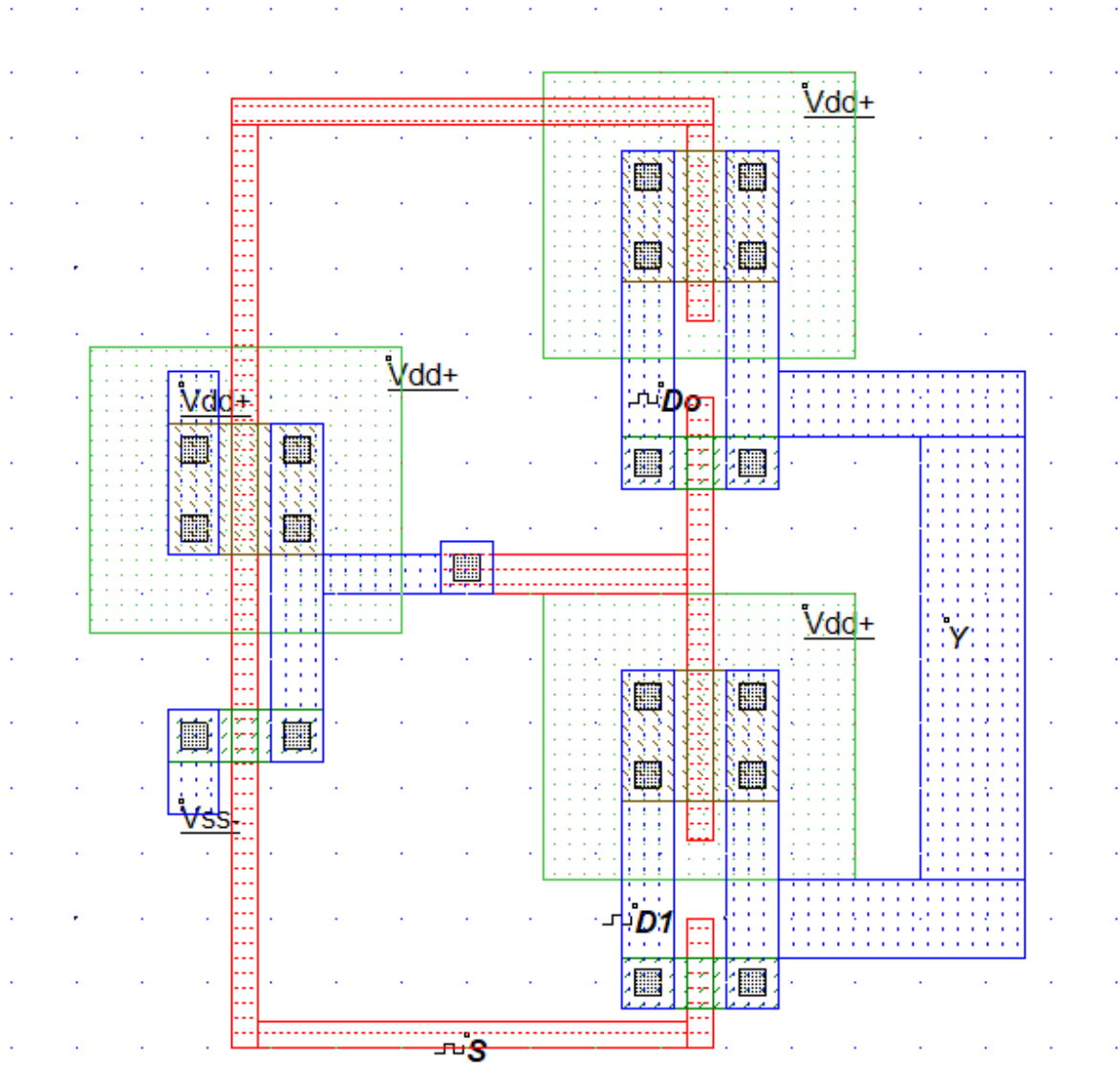
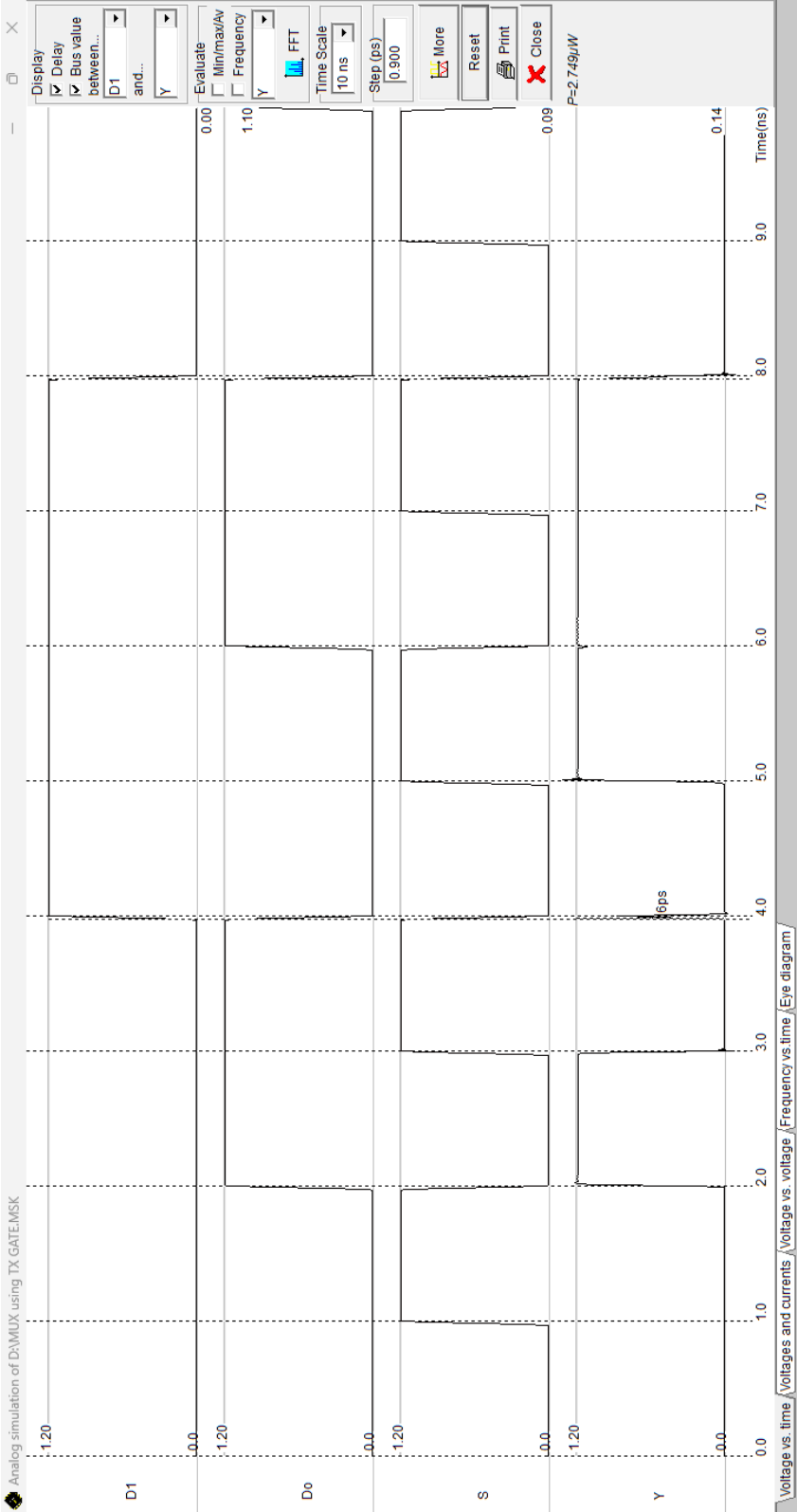


**2:1 MUX USING TRANSMISSION GATES**



## 2:1 MUX USING CMOS NAND GATES

