

A project Report

*ECE 1002 (Fundamental of Electrical And
Electronic Engineering)*

Submitted by

PRATHAPANI SATWIKHA

(20BCD7160)



VIT-AP
UNIVERSITY

VIT-AP University ,

Inavolu , Amaravathi ,

Andhra Pradesh-522 237, India .

Index :

EXPT NO.	EXPERIMENT NAME	DATE
1.	Analysis of resistance using colour code	16/01/2021
2.	Verification of ohm's law	19/01/2021
3.	Verification of KCL and KVL	19/01/2021
4.	Verification of current and voltage division rule	20/01/2021
5.	Verification of voltage current power relations for star-delta connected loads	21/01/2021
6.	Calculation of two port network parameters	23/01/2021
7.	Study of characteristics of semiconductor diode transistors	23/01/2021
8.	Design and simulation of various rectifier circuits	27/01/2021
9.	Design and implementation of MOSFET Voltage amplifier	28/01/2021
10.	Application of Thevenin's theorem	28/01/2021

EXPERIMENT NO. : 1

Objectives:

- 1.To learn Resistor colour code .
- 2.To determine the stated value of a resistor by interpreting the colour code indicated on the resistor .
- 3.To verify series and parallel combination of R, C using voltage and current division rule .

Software Used : NI Multisim

Theory :

a) Resistor Colour code :

- 1 . Hold a resistor in your hand . The section with more number of band should be on left side . After the gap, on right side should be one/two band indicating tolerance or temperature co-efficient .
- 2 . Write on paper in capital letters i.e. , BOGY(GAP)YS, the Colour starting from left to right .
3. Replace the colors with numbers that will be the value of resistor resistance i.e., $035 \times 10^4 \pm 3\%$.Cross verification can be done using digital multi-meter .

b) Series and parallel combination of R and C

- 1 . Pick three resistors rated at $R_1=1k\Omega$, $R_2=2k\Omega$, and $R_3=3k\Omega$. Measure their values in the using multimeter .
- 2 . Construct , one at a time , arrangements shown in Fig 2(a) and Fig.2(b) on bread board . Set the supply to 20V .
- 3 . For each arrangement , measure the indicated variables .
- 4 . Repeat the same experiment with three different value of C . Use

a function generator as AC power supply . Measure the RMS value of voltage and

current, using multimeter. To verify series and parallel connection of C and note

down absolute value of reading .

Circuit diagram(s) : Resistor comes in 4, 5 or 6-bands. A 6-band resistor is shown in Fig. 1.

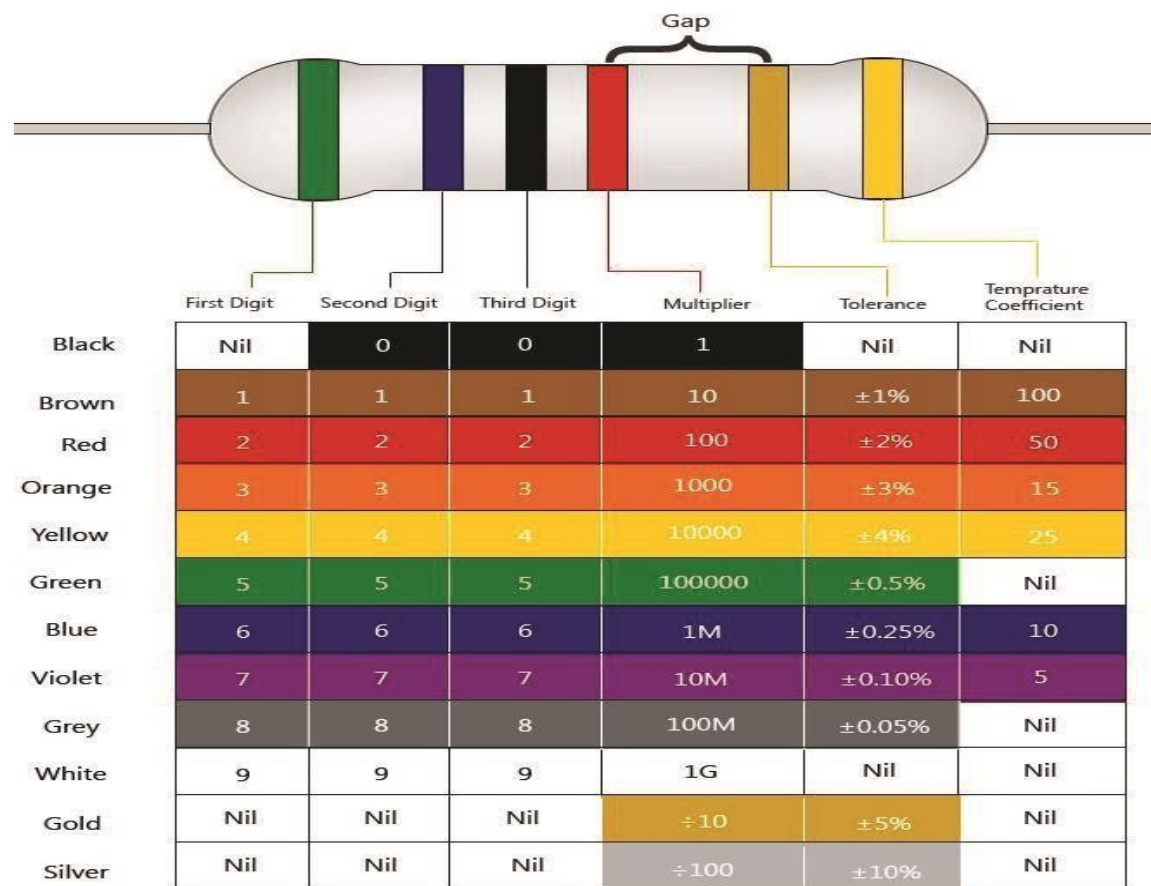


Figure 1: Colour code for a resistor.

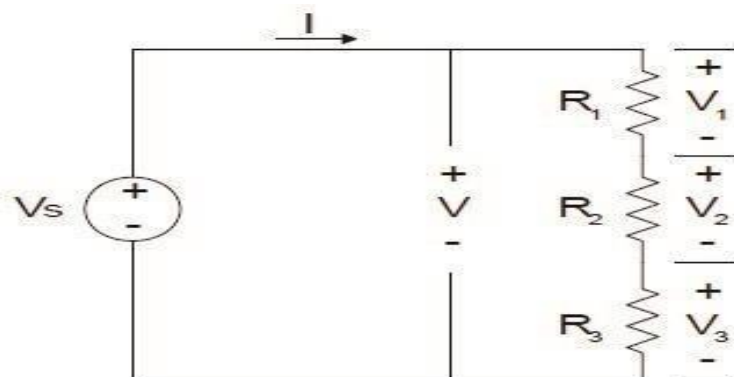


Figure 2a: Series combination of resistors.

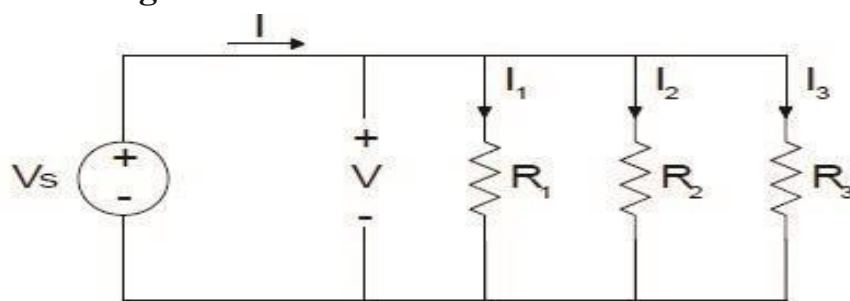


Figure 2b: Parallel combination of resistors.

Results & Observations :

	Resistance Value	Tolerance
	22×10^2	$\pm 5\%$
	56×10^4	$\pm 10\%$
	47×10^3	$\pm 10\%$
	10×10^1	$\pm 5\%$

EXPERIMENT NO. : 2

Objective : To Verify the Ohm's Law

Software used : NI Multisim

Theory :

Ohm's law states that “ at a constant temperature, the electrical current flowing through a conductor is directly proportional to the voltage applied across it, and also inversely proportional to the resistance ” .

Mathematically can be written as :

$$V \propto I ;$$

$$I = V/R ;$$

$$V = IR$$

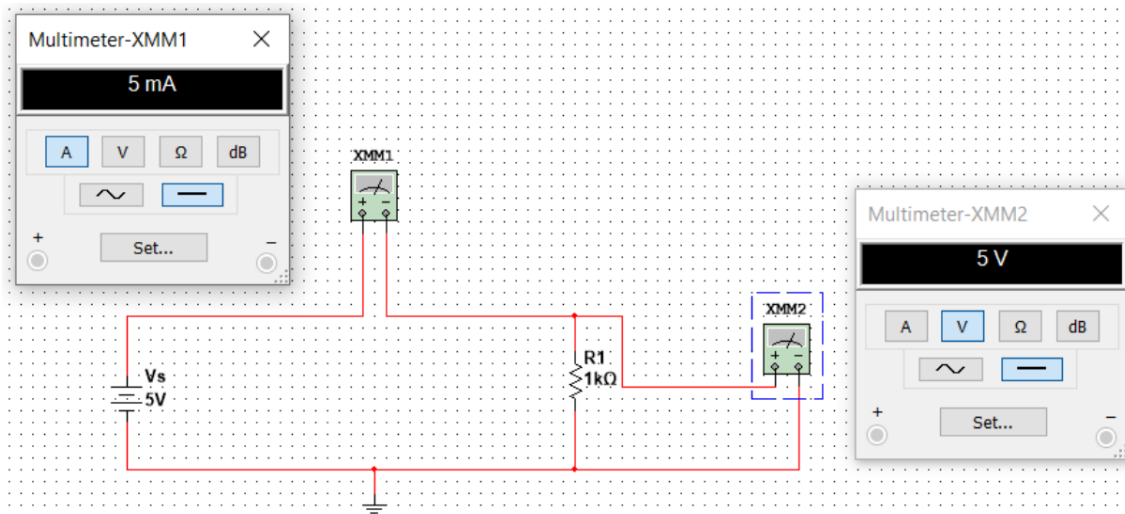
Where ,

V = Voltage measured across the conductor

R = Resistance of the conductor

I = Current through the conductor

CIRCUIT DIAGRAM :



Results & Observations :

THEORITICAL**MUTISIM**

S.NO.	Vs	R(ohm)	I	Vout	I	Vout
1.	5V	1K	5mA	5V	5mA	5V
2.	8V	3K	2.667mA	8.001V	2.667mA	8V
3.	12V	8K	1.5mA	12V	1.5mA	12V
4.	16V	9K	1.778mA	16.002V	1.778mA	16V
5.	18V	12K	1.5mA	18V	1.5mA	18V

EXPERIMENT NO. : 3

Objective : To Verify KCL And KVL Equations

Software used : NI Multisim

Theory :

Junction is a point where three or more components of a circuit meet .

Kirchhoff's Current Law states that “ The sum of the currents flowing towards the junction is equal to the sum of the currents flowing away from the junction ” .

In another way we can say that “ The algebraic sum of currents at a junction is zero ” .

$$\text{i.e. } \sum I = 0 .$$

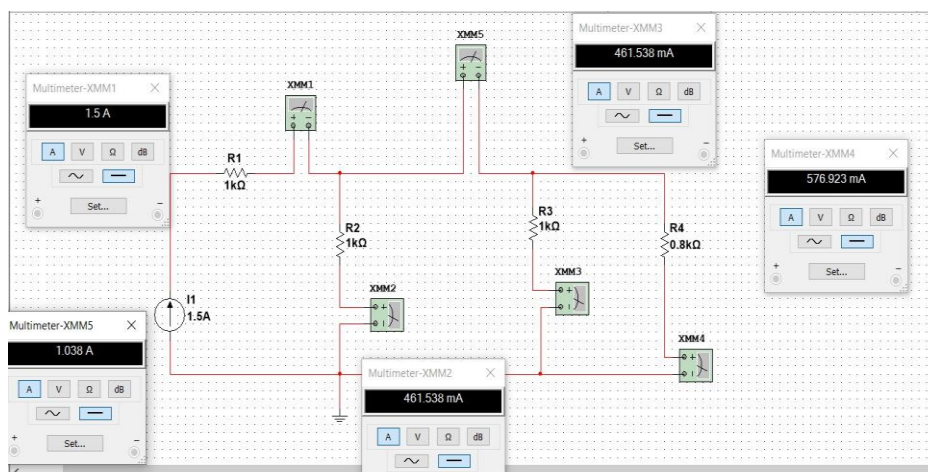
Kirchhoff's Voltage Law states that “The algebraic sum of all voltages around any closed loop in a circuit is equal to zero”.

$$\text{i.e. } \sum V = 0 .$$

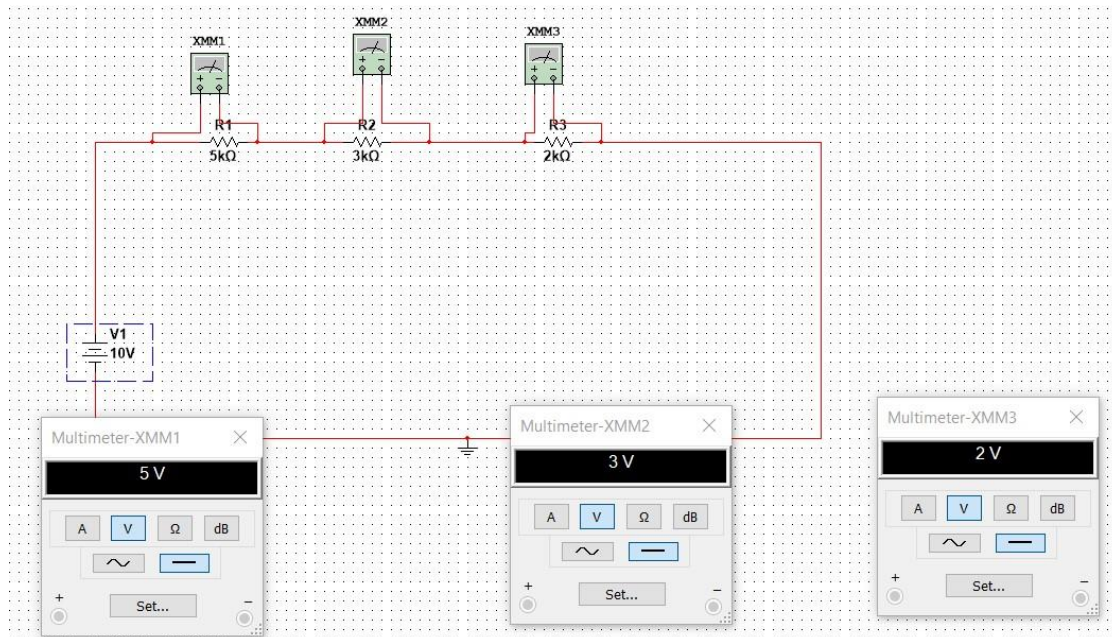
In another way we can say that “The sum of all the potential differences around the loop must be equal to zero .

CIRCUIT DIAGRAM :

1) KCL



2) KVL



RESULTS AND OBSERVATIONS :

1) Experimental Result :

$$i_2 = 1.038 \text{ A}$$

Current across R2, i.e. i_3 is 461.538mA

Current across R3, i.e. i_4 is 461.538mA

Current across R4, i.e. i_5 is 576.923mA

Theoretical Result :

Given:

$$R_2 = 1000 \Omega \quad \text{current } (I_1) = 1.5 \text{ A}$$

$$R_3 = 1000 \Omega$$

$$R_4 = 800 \Omega$$

Resistors R_3, R_4 are connected in parallel

$$\frac{1}{R_{eq34}} = \frac{1}{1000} + \frac{1}{800} = \frac{9}{4000}$$

$$\Rightarrow R_{eq34} = \frac{4000}{9} = 444.44 \Omega$$

$$\Rightarrow R_{eq13} = 444.44 \Omega$$

$$I_3 = \frac{1.5 \times R_{eq34}}{R_2 + R_{eq34}} = \frac{1.5 \times 444.44}{1000 + 444.44} = 0.461 \text{ A}$$

$$I_4 = \frac{1.5 \times R_{eq13}}{R_2 + R_{eq13}} = \frac{1.5 \times 444.44}{1000 + 444.44} = 0.461 \text{ A}$$

$$I_5 = 1.5 - (I_3 + I_4) = 0.576 \text{ A}$$

2) Experimental Result :

The voltage across $R_1 = 5k \text{ ohm}$ is $5V$

The voltage across $R_2 = 3k \text{ ohm}$ is $3V$

The voltage across $R_3 = 2k \text{ ohm}$ is $2V$

Theoretical Result :

Handwritten calculations for a series circuit:

$$V_1 = 10V$$
$$R_1 = 5k\Omega$$
$$R_2 = 3k\Omega$$
$$R_3 = 2k\Omega$$

Resistors are connected in series

$$\Rightarrow R_{eq} = (5k + 3k + 2k)\Omega = 10k\Omega$$
$$I = \frac{V}{R_{eq}} = \frac{10}{10 \times 10^3} = 10^{-3} A$$
$$V_1 = I \cdot R_1 = 5 \times 10^{-3} \times 10^3 = 5V$$
$$V_2 = I \cdot R_2 = 3 \times 10^{-3} \times 10^3 = 3V$$
$$V_3 = I \cdot R_3 = 2 \times 10^{-3} \times 10^3 = 2V$$

EXPERIMENT NO. : 4

Objective : To verify the Voltage and Current division Principle .

Software used : NI Multisim

Theory :

Voltage division rule states that “The voltage across any resistor in a series connection of resistors is equal to the ratio of the value of the resistor divided by the total resistance of the circuit ” .

$$V_{out} = (V_s * R_1) / (R_1 + R_2)$$

$$V_{out} = (V_s * R_2) / (R_1 + R_2)$$

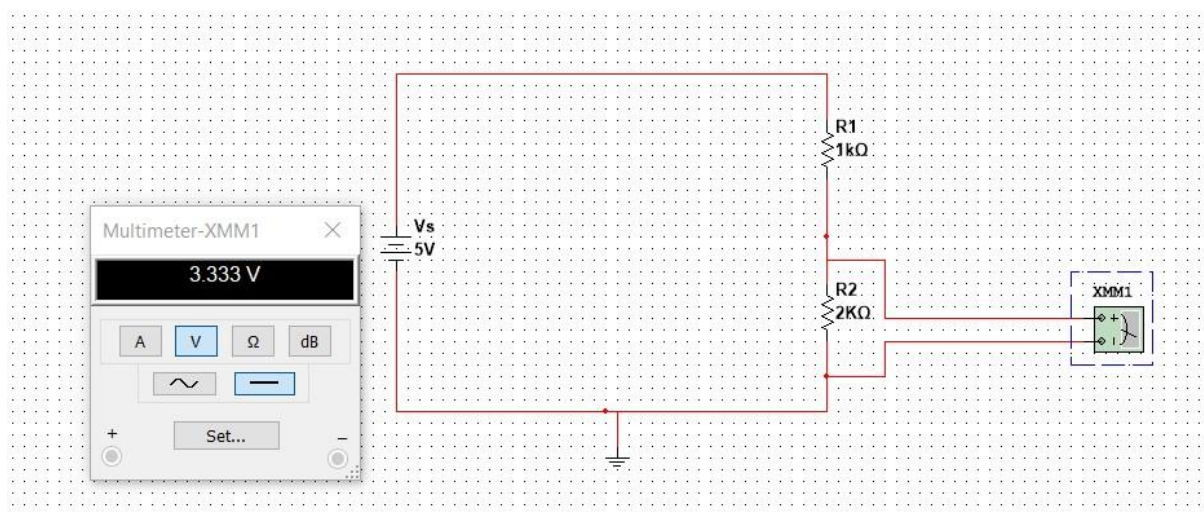
Current division rule states that “The current in any parallel branches of the circuit is equal to the ratio of opposite branch resistance to total resistance , multiplied by total current . The current division rule determines the current across the circuit impedance ” .

$$I_1 = (I_s * R_1) / (R_1 + R_2)$$

$$I_2 = (I_s * R_2) / (R_1 + R_2)$$

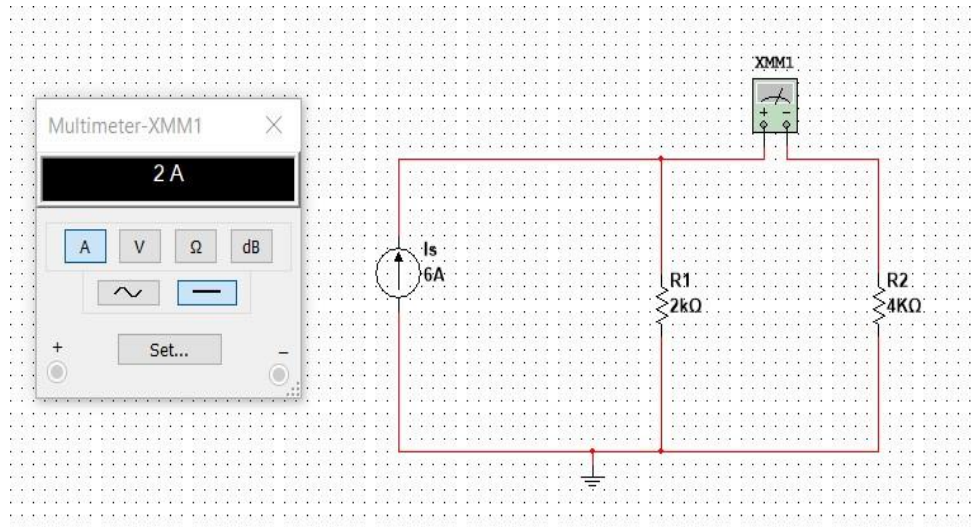
Circuit Diagram :

Voltage Division Rule :

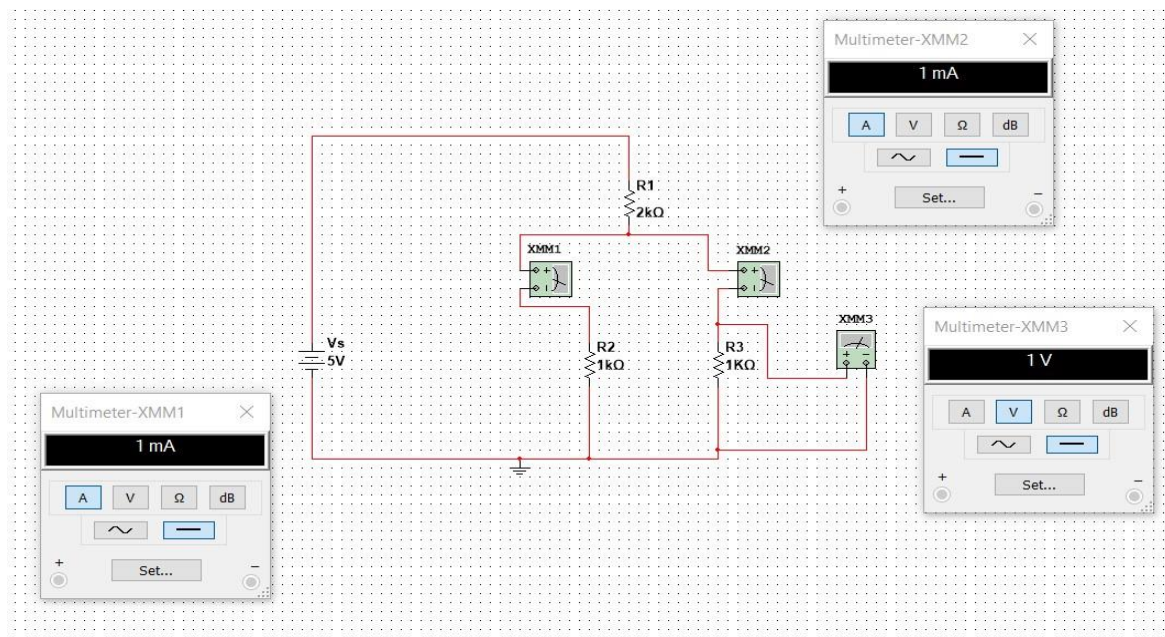


Circuit – 1

Current Division Rule :



Circuit - 2



Circuit - 3

RESULTS AND OBSERVATIONS :

For Voltage Division Rule :

Circuit - 1 :

S.NO.	Vs(V olt)	R1(ohm)	R2(ohm)	THEORITIC AL Vout	MULTISI M Vout
1.	5	1K	2K	3.333V	3.333V
2.	5	2K	3K	3V	3V
3.	5	2.5K	3.1K	2.767V	2.768V
4.	5	4K	3.2K	2.222V	2.222V
5.	10	6K	4.5K	4.285V	4.286V

For Current Division Rule :

Circuit – 2 :

S.NO.	Is(Ampe re)	R1(ohm)	R2(ohm)	THEORITIC AL Iout	MULTI SIM Iout
1.	6	2k	4k	2A	2A
2.	3	2K	4K	1A	1A
3.	5	1.2K	2.5K	1.621A	1.622A
4.	8	1.6K	1.4K	4.266A	4.267A
5.	6	1.8K	1.6K	3.176A	3.176A

Circuit – 3 :

Multisim values							
S.NO.	Vs	R1(ohm)	R2(ohm)	R3(ohm)	I1	I2	Vout
1.	5V	2K	1K	1K	1mA	1mA	1V
2.	6V	1K	2K	2K	1.5mA	1.5mA	3V
3.	8V	2K	2K	1K	2mA	1mA	2V

EXPERIMENT NO. : 5

Objective : To verify the voltage, current, power relations for star and delta connected loads.

Software used : NI Multisim.

Theory :

Voltages and Currents in Y-Connection :

The voltage induced in each winding is called the phase voltage and current in each winding is likewise known as phase current. However, the voltage available between any pair of terminals is called line voltage (V_L) and the current flowing in each line is called line current (I_L).

Line Voltages and Phase Voltages :

The p.d. between line 1 and 2 is $V_{RY} = E_R - E_Y$. Hence, V_{RY} is found by compounding E_R and E_Y reversed. Obviously, the angle between E_R and E_Y reversed is 60° . Hence if $E_R = E_Y = E_B = \text{say } E_{ph}$ -the phase e.m.f. , then

$$V_{RY} = 2 \times E_{ph} \times \cos(60^\circ/2) = \sqrt{3}E_{ph}$$

$$\text{Similarly, } V_{YB} = E_Y - E_B = \sqrt{3}E_{ph} \text{ and } V_{BR} = E_B - E_R = \sqrt{3}E_{ph}$$

Now $V_{RY} = V_{YB} = V_{BR} = \text{line voltage, say } V_L$.

Hence, in star connection $V_L = \sqrt{3}E_{ph}$.

Line Currents and Phase Currents :

Line current in each line is the same as the current in the phase winding to which the line is connected.

Current in line 1 = I_R ; Current in line 2 = I_Y ; Current in line 3 = I_B

Since $I_R = I_Y = I_B = \text{say, } I_{ph}$ – the phase current

$$\therefore \text{line current } I_L = I_{ph}.$$

Power :

The total active or true power in the circuit is the sum of the three phase powers.

$$\text{Total active power} = 3 \times \text{phase power or } P = 3 \times V_{ph} I_{ph} \cos\phi$$

$$P = \sqrt{3} V_L I_L \cos\phi$$

Delta (Δ) or Mesh Connection :

If the system is balanced then sum of the three voltages round the closed mesh is zero.

This type of connection is also referred to as 3-phase, 3-wire system.

Line Voltages and Phase Voltages :

The voltage between lines 1 and 2 as V_{RY} and that between lines 2 and 3 as V_{YB} , we find that V_{RY} lead V_{YB} by 120° . Similarly, V_{YB} leads V_{BR} by 120° .

Let $V_{RY} = V_{YB} = V_{BR} = \text{line voltage } V_L$. Then, it is seen that $V_L = V_{ph}$.

Line Currents and Phase Currents :

Current in each line is the vector difference of the two phase currents flowing line.

Current in line No. 1 is found by compounding I_R and I_B reversed

$$I_1 = 2 \times I_{ph} \times \cos(60^\circ/2) = \sqrt{3} I_{ph}$$

$$I_2 = I_B - I_Y = \sqrt{3} I_{ph} I_3$$

$$= I_B - I_Y = \sqrt{3} I_{ph}$$

Since all the line currents are equal in magnitude i.e.

$$I_1 = I_2 = I_3 = I_L$$

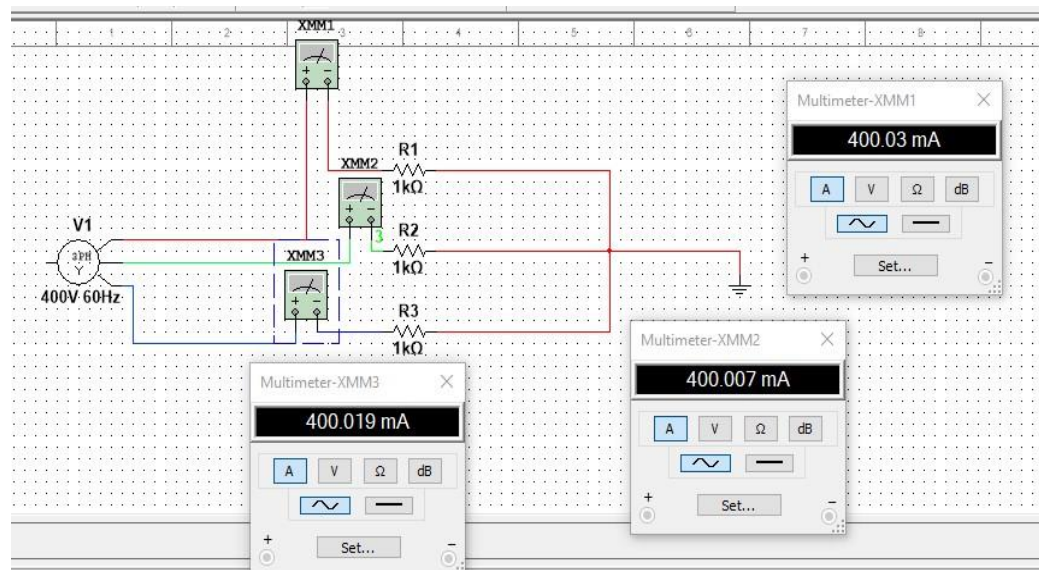
$$\therefore I_L = \sqrt{3} I_{ph}$$

Power :

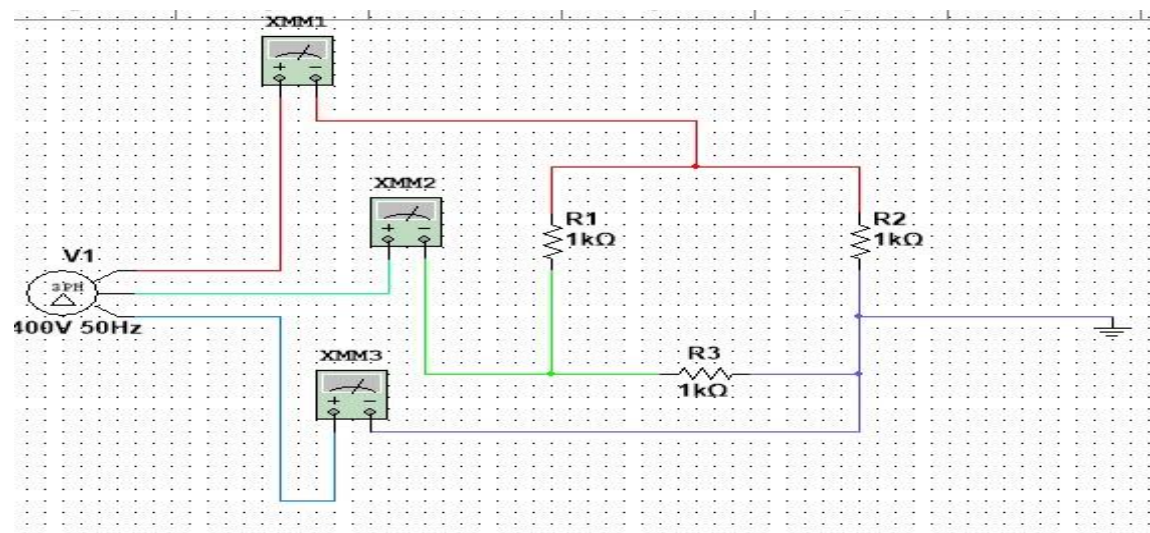
$$\text{Total power} = 3 \times V_{ph} I_{ph} \cos\phi$$

Circuit Diagram :

STAR :



DELTA :



RESULTS & OBSERVATIONS :

STAR :

Parameters	Multisim	Theoretical
V_{RY}	692.872V	692.8V
V_{YB}	692.872V	692.8V
V_{BR}	692.872V	692.8V
I_R	400.03mA	400 mA
I_Y	400.07 mA	400 mA
I_B	400.019 mA	400 mA
P₁	240.037W	240.0285W
P₂	240.037W	240.0285W
P = P₁ + P₂	480.074W	480.057W

DELTA :

Parameters	Multisim	Theoretical
V_{RY}	400V	400V
V_{YB}	400V	400V
V_{BR}	400V	400V
I_R	692.861mA	692.820mA
I_Y	692.872mA	692.820mA
I_B	692.848mA	692.820mA
P₁	240.037W	239.9995W
P₂	240.037W	239.9995W
P = P₁ + P₂	480.074W	479.999W

EXPERIMENT NO.-6

Objective :

- To understand the analysis of a two-port network
- To understand the behavior of a two-port network using parametric analysis.
- To learn the measurement conditions and procedure for two-port analysis.

• **Software Used :** NI Multisim

• Theory :

The electrical network with two pairs of terminals is a two-port network . The network inside the box can contain resistors, inductors, capacitors, transformers, transistors and in general any linear circuit device, including depending devices but no independent sources are allowed. The behavior of a linear two-port network is described by impedance (Z), admittance (Y), transmission (ABCD), or hybrid (h) parameter .

Z - parameters :

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

Parameter	Condition	Name
$Z_{11} = V_1/I_1$	$I_2 = 0$	Input Impedance
$Z_{21} = V_2/I_1$	$I_2 = 0$	Transfer Impedance
$Z_{12} = V_1/I_2$	$I_1 = 0$	Transfer Impedance
$Z_{22} = V_2/I_2$	$I_1 = 0$	Output Impedance

Y-parameters :

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

Parameter	Condition	Name
$Y_{11} = I_1/V_1$	$V_2 = 0$	Input admittance
$Y_{21} = I_2/V_1$	$V_2 = 0$	Transfer admittance
$Y_{12} = I_1/V_2$	$V_1 = 0$	Transfer admittance
$Y_{22} = I_2/V_2$	$V_1 = 0$	Output admittance

H-parameters :

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2$$

Parameter	Condition	Name
$h_{11} = V_1/I_1$	$V_2 = 0$	SS input admittance
$h_{21} = I_2/I_1$	$V_2 = 0$	SS forward current gain
$h_{12} = V_1/V_2$	$I_1 = 0$	OS reverse voltage gain
$h_{22} = I_2/V_2$	$I_1 = 0$	OS output admittance

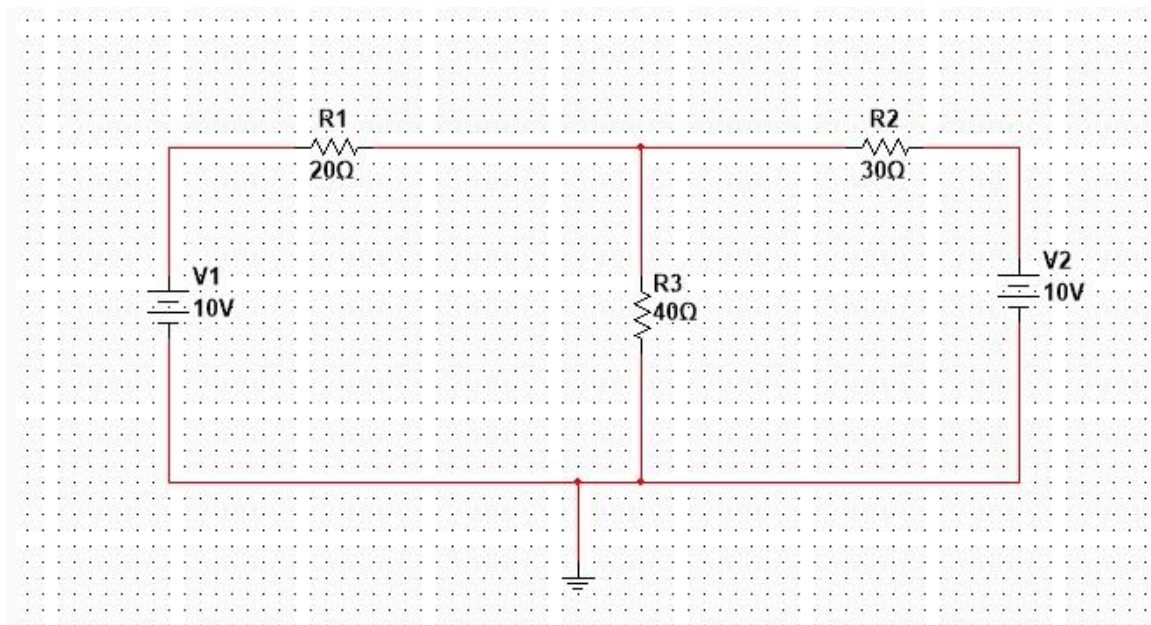
ABCD-parameters :

$$V_1 = AV_2 - BI_2$$

$$I_1 = CV_2 - DI_2$$

Parameter	Condition	Name
$A = V_1/V_2$	$I_2 = 0$	OC voltage ratio
$B = V_1/-I_2$	$V_2 = 0$	OC transfer admittance
$C = I_1/V_2$	$I_2 = 0$	-SC transfer impedance
$D = I_1/-I_2$	$V_2 = 0$	-SC current ratio

Circuit Diagram :



RESULTS & OBSERVATIONS :

Parameter	Calculated Value	Measured value
Z_{11}	60Ω	$59.998\ \Omega$
Z_{21}	$40\ \Omega$	$40.001\ \Omega$
Z_{12}	$40\ \Omega$	$39.998\ \Omega$
Z_{22}	$70\ \Omega$	$70\ \Omega$
Y_{11}	$0.0269\ \text{mho}$	$0.0269\ \text{mho}$
Y_{21}	$0.0153\ \text{mho}$	$0.01538\ \text{mho}$
Y_{12}	$0.0153\ \text{mho}$	$0.01538\ \text{mho}$
Y_{22}	$0.023\ \text{mho}$	$0.023\ \text{mho}$
h_{11}	$37.142\ \Omega$	$37.14\ \Omega$
h_{21}	0.571	0.57
h_{12}	0.571	0.571
h_{22}	$0.0142\ \text{mho}$	$0.0142\ \text{mho}$
A	1.5	1.499
B	$-65\ \Omega$	$-65\ \Omega$
C	$0.025\ \text{mho}$	$0.0249\ \text{mho}$
D	-1.75	-1.75

EXPERIMENT NO. -7

Objective : To study the input and output characteristics of semiconductor diodes

Software Used : NI Multisim

Theory :

A semiconductor diode is a combination of p and n type semiconductors which in forward bias at which the flow of current during the PN Junction begins increasing rapidly is known as **cut-in voltage** . After achieving cutting voltage the increase in current is almost exponential . A diode in reverse bias conducts negligible amount of current in the order of micro amperes .

$$I = I_0 (e^{(V/(\eta V T))} - 1)$$

Where ,

I = current flowing through the diode

I_0 = reverse saturation current,

q = charge on the electron,

V = voltage applied across the diode,

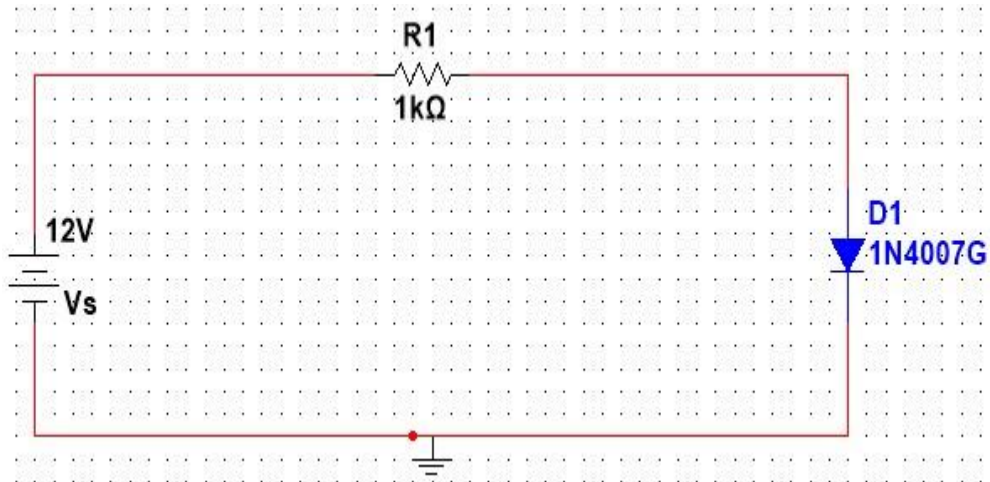
η = ideality factor (Ge = 1 and Si = 2) .

T is the absolute temperature in Kelvin.

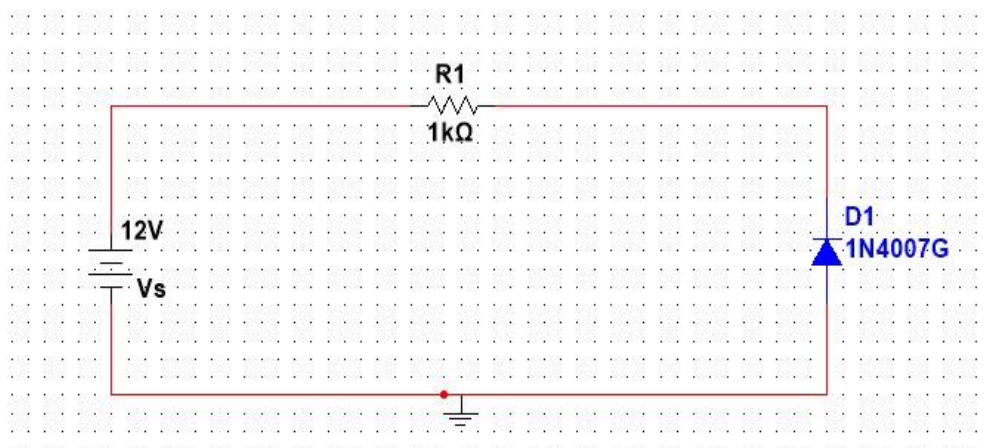
The configuration in which the emitter is connected between the collector and base is known as a common emitter configuration. The input circuit is connected between emitter and base , and the output circuit is taken from the collector and emitter .

Circuit Diagram :

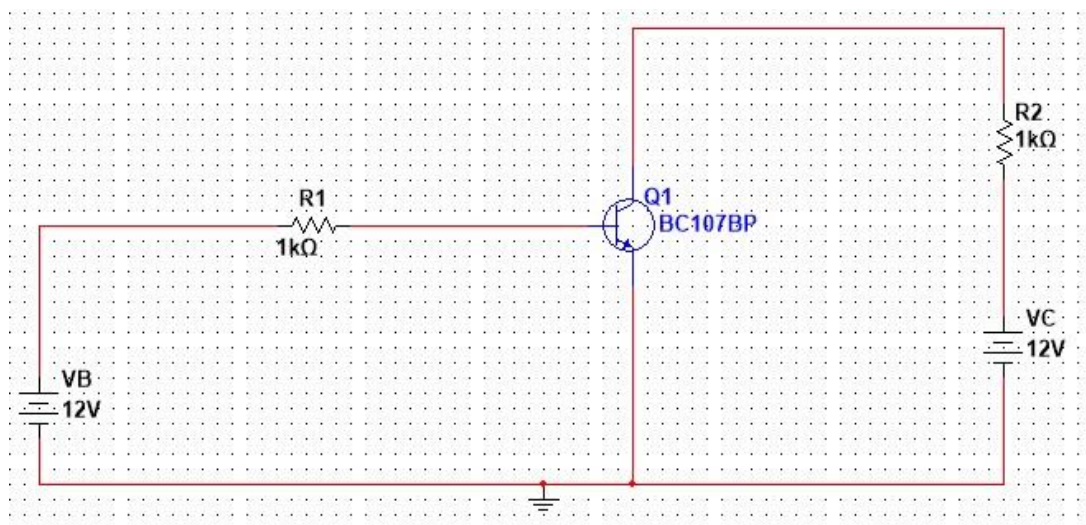
1 . Diode in Forward Bias :



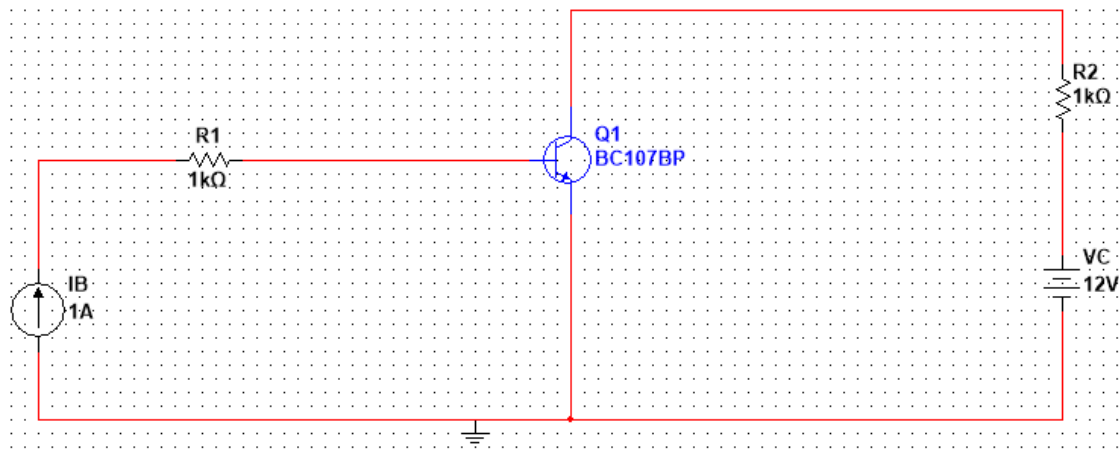
2. Diode in Reverse Bias :



3. Common Emitter Input Configuration :



4 .Common Emitter Output Configuration :

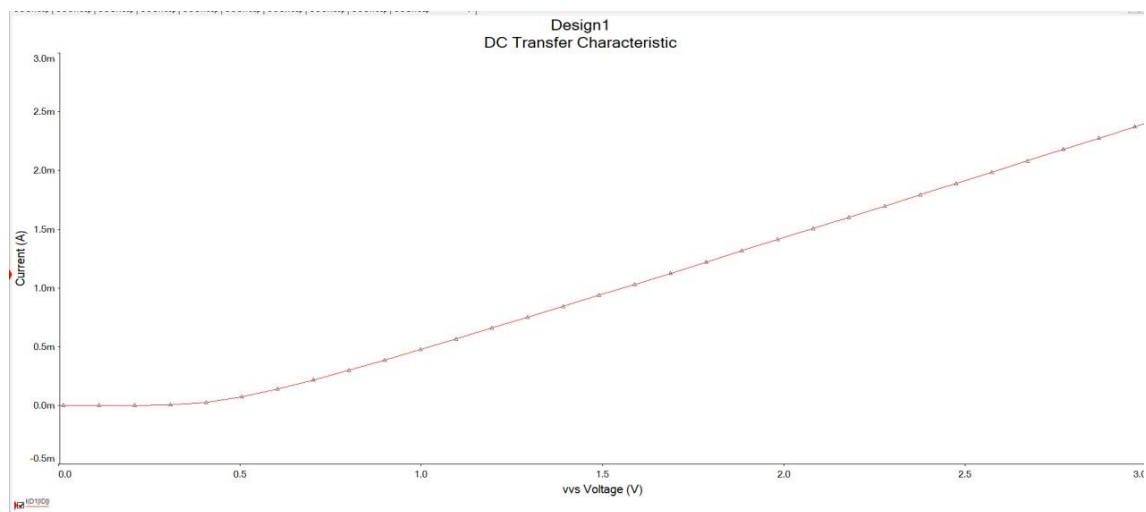


Results & Observations :

1 . Diode is in Forward Bias :

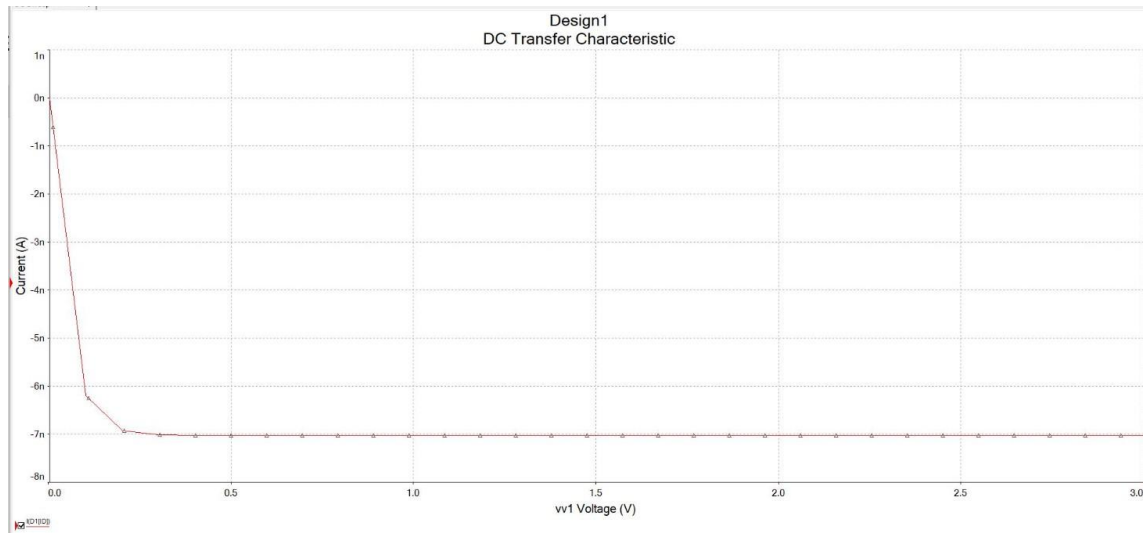
The Cutting Voltage for the diode is 0.3 V .

Therefore the diode is a Germanium Diode

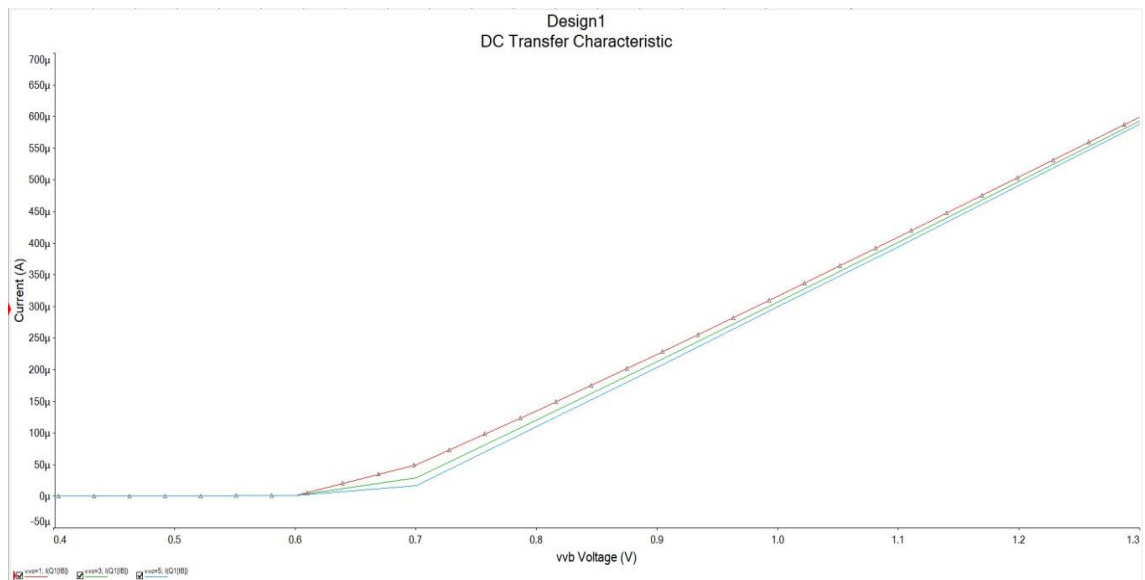


2 . Diode is in Reverse Bias :

The leakage current is negligible or zero .

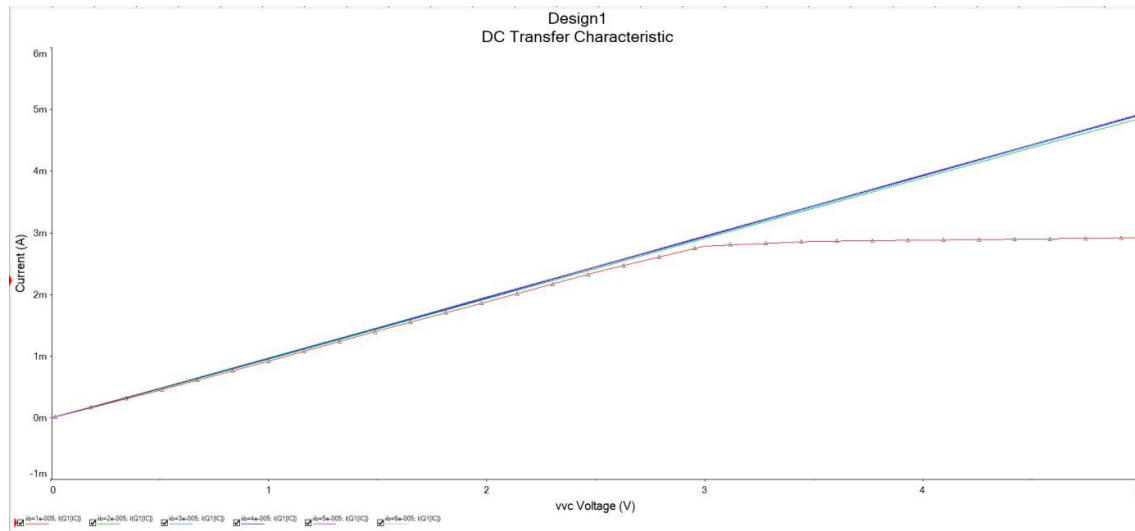


3. Common Emitter Configuration Input Characteristics :



	Voltage (V_c)		
	1V	3V	5V
Cutting Voltage (V_γ)	0.500V	0.506V	0.510V

4. Common Emitter Configuration Output Characteristics :



	Base Current (I_B)		
	10 μA	30 μA	50 μA
Collector Current (I_C)	2.77mA	8.74mA	14.46mA

EXPERIMENT NO. – 8

Objective : To design and simulate the half wave rectifier and full wave rectifier.

Software used : NI

Multisim

Theory :

A rectifier is a circuit that converts the Alternating Current (AC) input power into a Direct Current (DC) output power.

Half wave rectifiers use one diode, while a full wave rectifier uses multiple diodes.

“ The power diode in a half-wave rectifier circuit passes just one half of each complete sine wave of the AC supply to convert it into a DC supply. Then this type of circuit is called a “ **Half-wave rectifier** ”, because it passes only half of the incoming AC power supply ” .

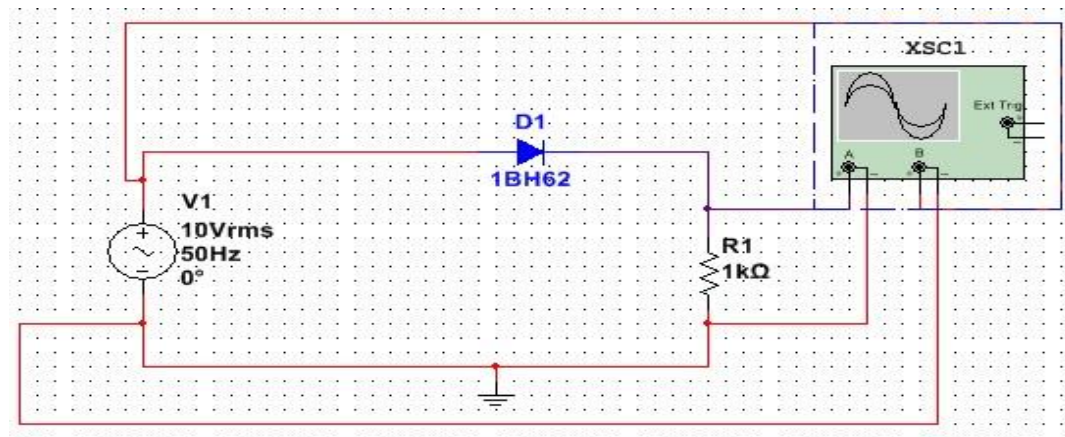
During each “ positive ” half cycle of the AC sine wave, the diode is forward biased as the anode is positive concerning the cathode resulting in current flowing through the diode. During each “ negative ” half cycle of the AC sinusoidal input waveform, the diode is reverse biased as the anode is negative concerning the cathode. Therefore, NO current flows through the diode or circuit .

“ **Full-wave rectifier** rectifies the negative component of the input voltage to a positive voltage then converts it into DC current utilizing a diode **bridge** configuration ” .

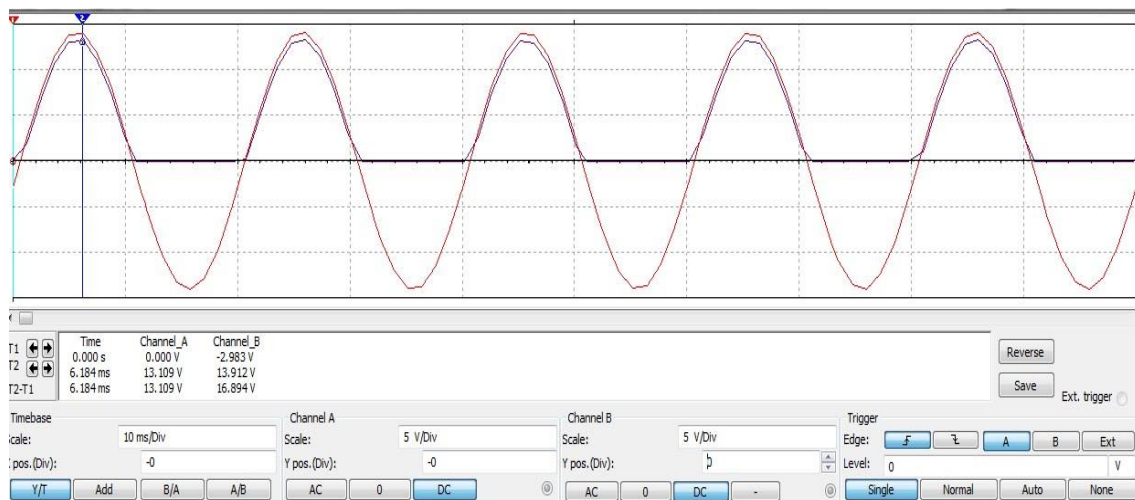
“ **Bridge rectifier** can be defined as a type of full-wave rectifier that uses four or more diodes in a bridge circuit configuration to efficiently convert alternating (AC) current to a direct (DC) current ” .

Circuit Diagram :

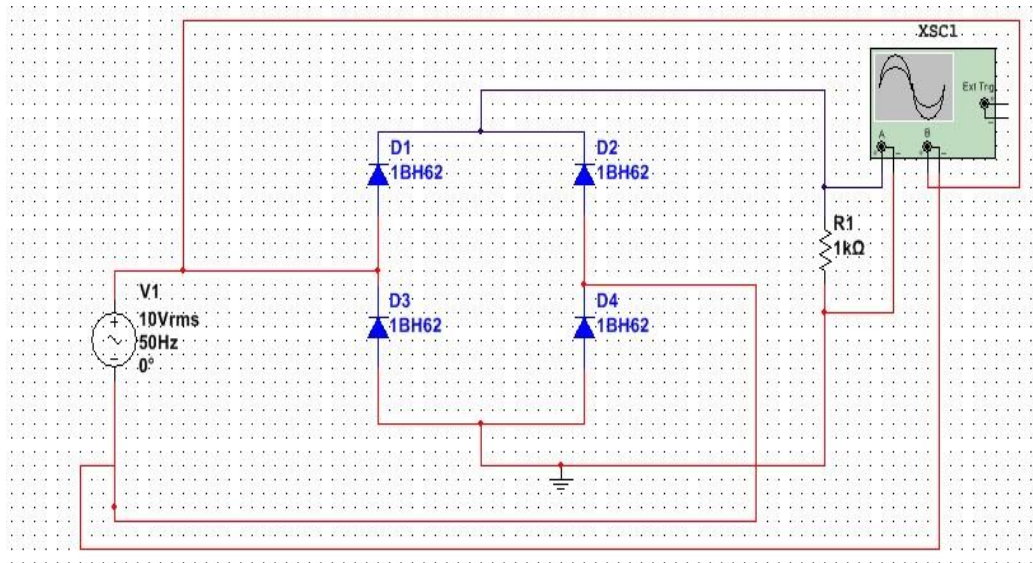
1 . Half Wave Rectifier :



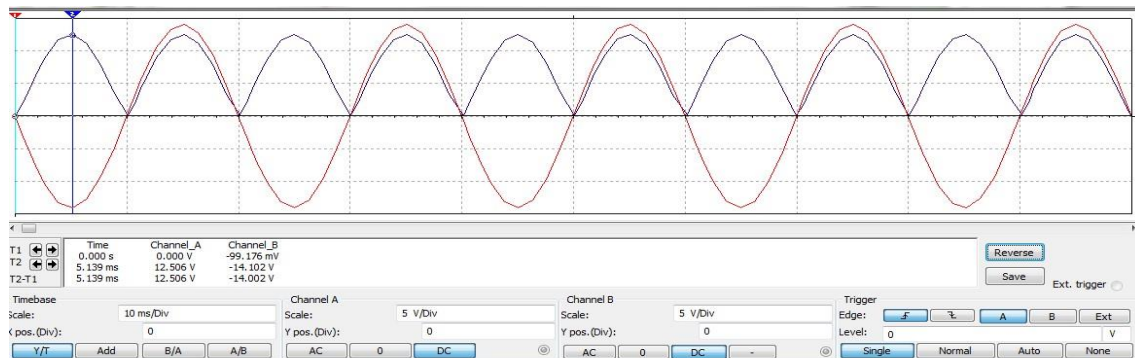
Graph :



2. Full Wave Rectifier :



Graph :



Results & observations :

Theoretical values :

Half Wave Rectifier:-

$$V_{rms} = \frac{V_m}{2} \quad [\text{Given } V_{rms} = 10]$$

$$V_{rms} = \frac{V_m}{2} \Rightarrow 10 = \frac{V_m}{2}$$

$$\boxed{V_m = 20V}$$

$$V_{DC} = \frac{V_m}{\pi} = \frac{20}{\pi} = \frac{20}{3.14} = 6.36$$

$$\boxed{V_{DC} = 6.36V}$$

$$\text{Ripple factor } (r) = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{10}{6.36}\right)^2 - 1}$$

$$= \sqrt{2.471 - 1}$$

$$\boxed{r = 1.2} \Rightarrow \boxed{\gamma = 1.2}$$

Full wave Rectifier:-

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad [\text{Given } V_{rms} = 10]$$

$$V_m = \sqrt{2} \times V_{rms}$$

$$= 1.414 \times 10 \Rightarrow \boxed{V_m = 14.14}$$

$$V_{DC} = \frac{2V_m}{\pi} = \frac{2 \times 14.14}{3.14} = \frac{28.28}{3.14} = 9.006$$

$$\boxed{V_{DC} = 9.006V}$$

$$\text{Ripple factor } (r) = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{10}{9.006}\right)^2 - 1}$$

$$= \sqrt{1.2 - 1}$$

$$= \sqrt{0.2}$$

$$\boxed{\gamma = 0.48}$$

	Vm		Vrms		VDC		γ	
Halfwave Recti fier	Theore tical	Multi sim	Theore tical	Multi sim	Theore tical	Multi sim	Theore tical	Mult i sim
	20V	13.18 1V	10V	6.590V	6.36V	4.195 V	1.2V	1.21 15 V
Fullwave Recti fier	Theore tical	Multi sim	Theore tical	Multi sim	Theore tical	Multi sim	Theore tical	Mult i sim
	14.14V	12.50 6V	10V	8.84V	9.006V	7.961 V	0.48V	0.48 3 V

EXPERIMENT NO. : 9

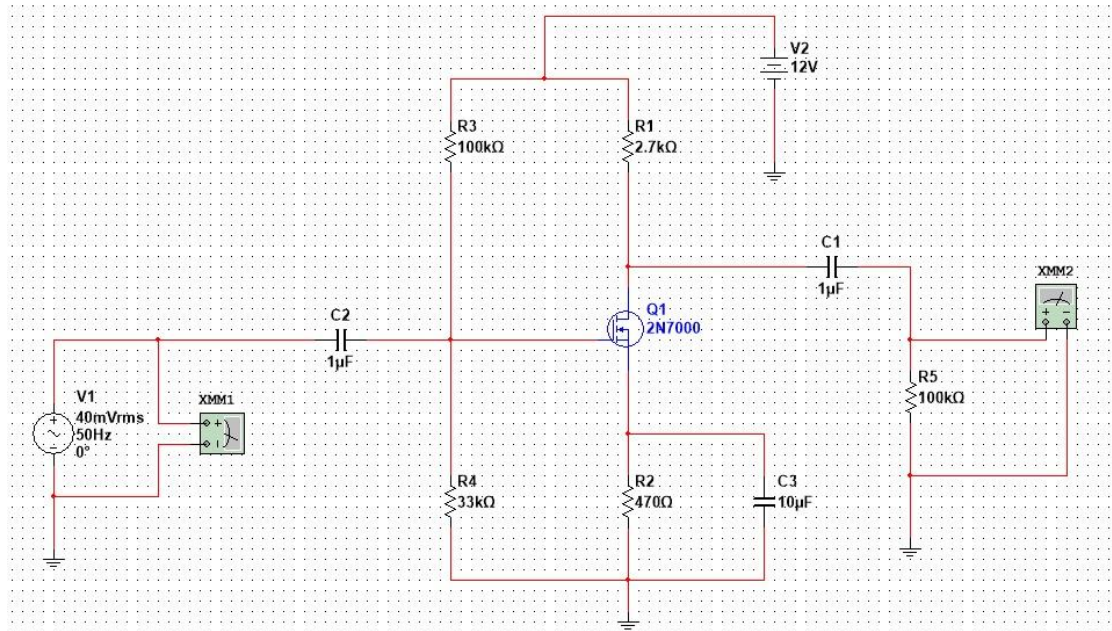
Objective : To study the MOSFET amplifier working in common source configuration with given specifications.

Software Used : NI MULTISIM

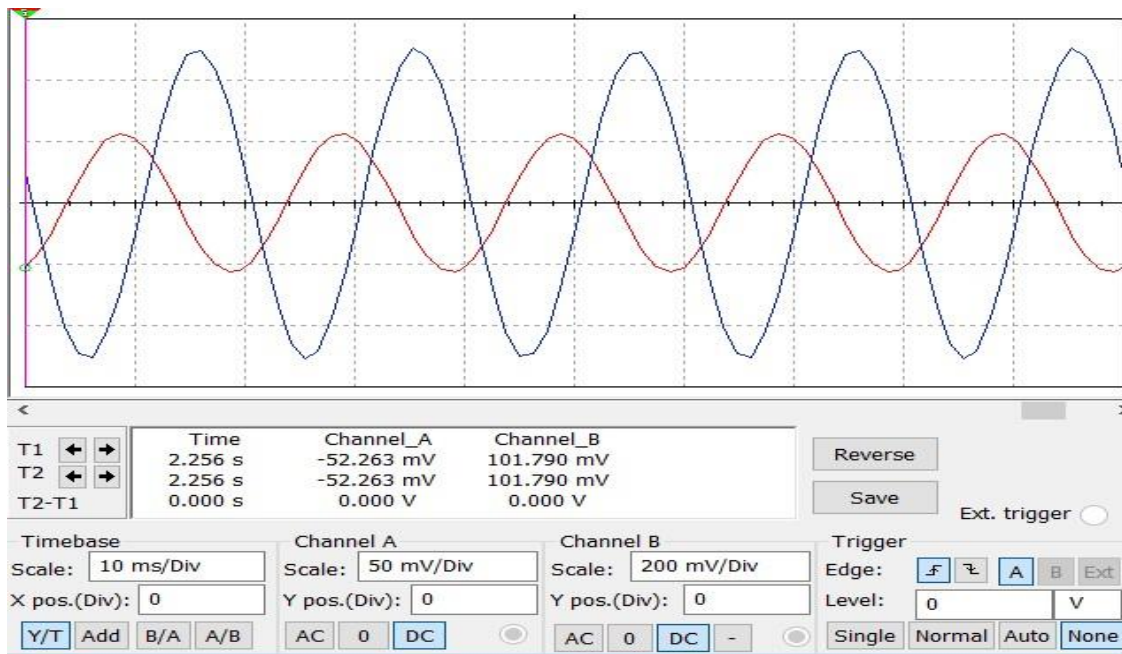
Theory :

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary n channel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology. Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown below. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by the bias resistors R1 and R2). Normally the value of the bias resistors is chosen as high as possible. However, too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the active region of the characteristics.

Circuit Diagram:



Results & Observations :



Input voltage V_i (mV)	Output voltage V_o (mV)	Voltage gain V_o/V_i
40.016	355.725	8.88956

50.016	442.937	8.85590
--------	---------	---------

The MOSFET successfully works as a voltage amplifier. we can say that MOSFET gives a gain of voltage 8.8volts that is nearly 9volts.

EXPERIMENT NO. : 10

Objective : To Verify Thevenin's theorem.

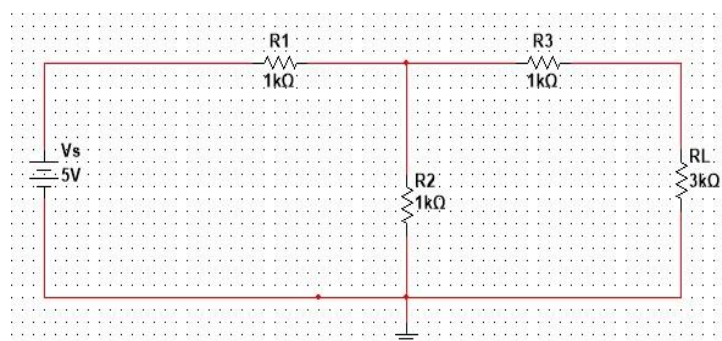
Software Used : NI Multisim

Theory :

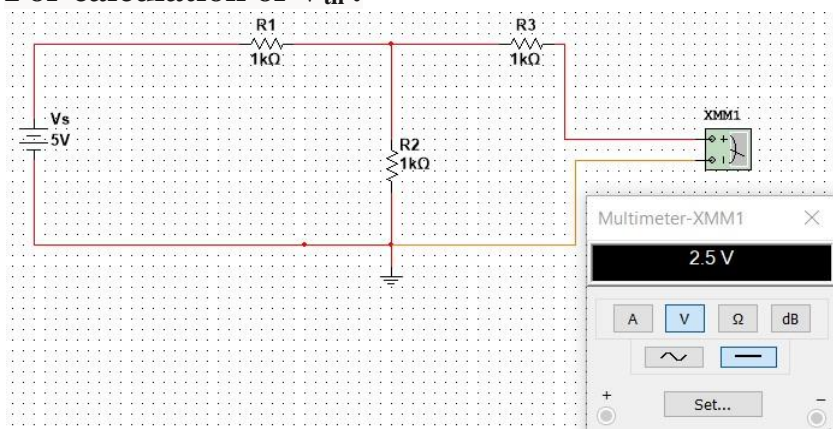
Any linear, bilateral network having a number of voltage, current sources and resistances can be replaced by a simple equivalent circuit consisting of a single voltage source in series with a resistance, where the value of the voltage source is equal to the open circuit voltage and the resistance is the equivalent resistance measured between the open circuit terminals with all energy sources replaced by their ideal internal resistances.

- “ **Thevenin's Theorem** states that any complicated network across its load terminals can be substituted by a voltage source (V_{TH}) with one resistance (R_{TH}) in series ” .
- This theorem helps in the study of the variation of current in a particular branch when the resistance of the branch is varied while the remaining network remains the same.

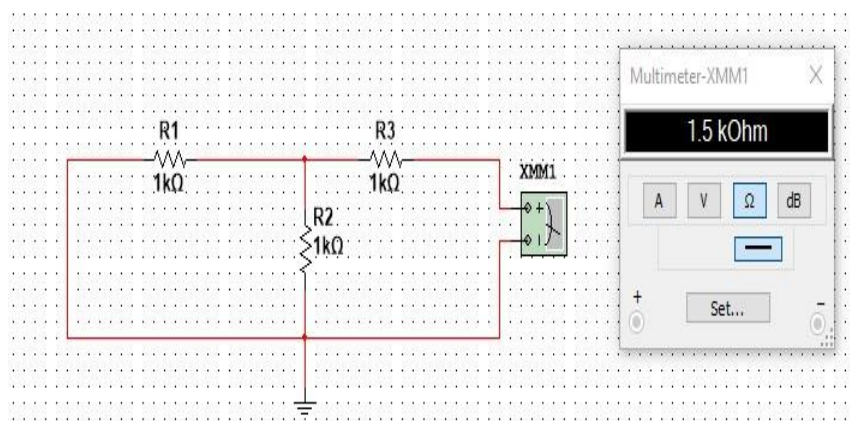
CIRCUIT DIAGRAM :



For calculation of V_{th} :



For calculation of R_{th} :



RESULTS & OBSERVATIONS :

Source Voltage(Vs)	R_1 (Ohm)	R_2 (Ohm)	R_3 (Ohm)	V_{th} (Theoretical value)	V_{th} (Multisim value)	R_{th} (Theoretical)	R_{th} (Multisim) (Ohm)
5V	1K	1K	1K	2.5V	2.5V	1.50K	1.50K
5.5V	2K	1.5K	1.2K	2.357V	2.357V	2.057K	2.057K
6.2V	1.3K	1.5K	1.2K	3.321V	3.321V	1.896K	1.896K
7.1V	1.3K	3K	2.2K	4.953V	4.953V	3.107K	3.107K
8V	1.4K	3.2K	2.4K	5.565V	5.565V	3.374K	3.374K