Architecture of Parallel Computers

Program 3

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1. INTRODUCTION

In computer architecture, distributed shared memory (DSM) is a form of memory architecture where the (physically separate) memories can be addressed as one (logically shared) address space. Here, the term shared does not mean that there is a single centralized memory but shared essentially means that the address space is shared (same physical address on two processors refers to the same location in memory).

A distributed-memory system (often called a multicomputer) consists of multiple independent processing nodes with local memory modules, which is connected by a general interconnection network. A distributed shared memory system implements the shared-memory-model on a physically distributed memory system.

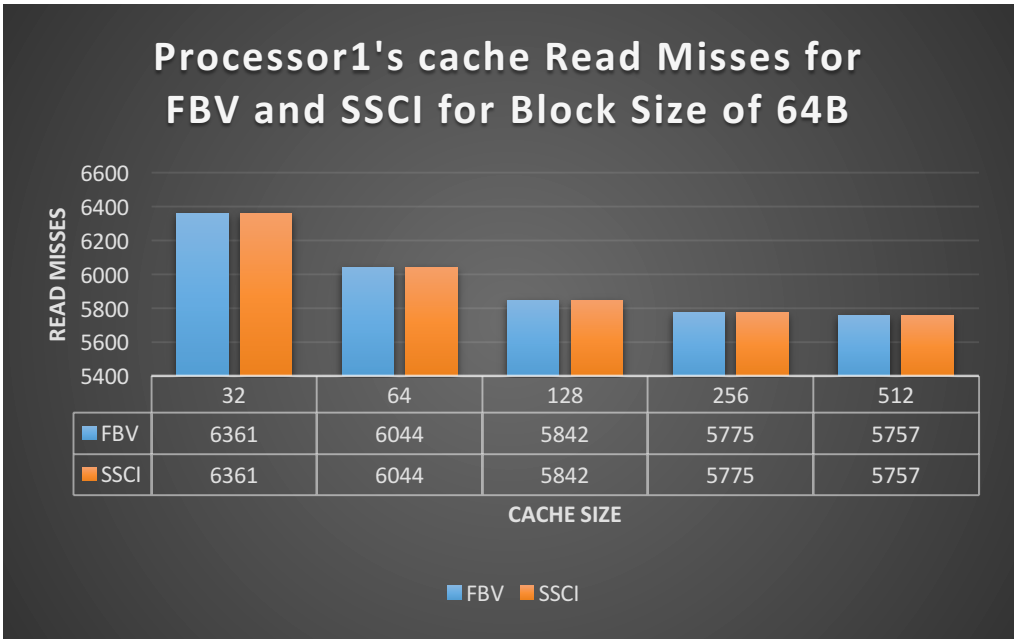
In this project we simulate the performance of a DSM system with 4 processors using MESI protocol and a Directory. Directory can be Full Bit Vector (FBV) directory or Simplified Scalable Coherent Interface (SSCI) directory. All the processors have their own cache class, which is handled by Cache class. MESI class handles MESI protocol. There is a base Directory class that is derived by FBV and SSCI class which handle directory related data.

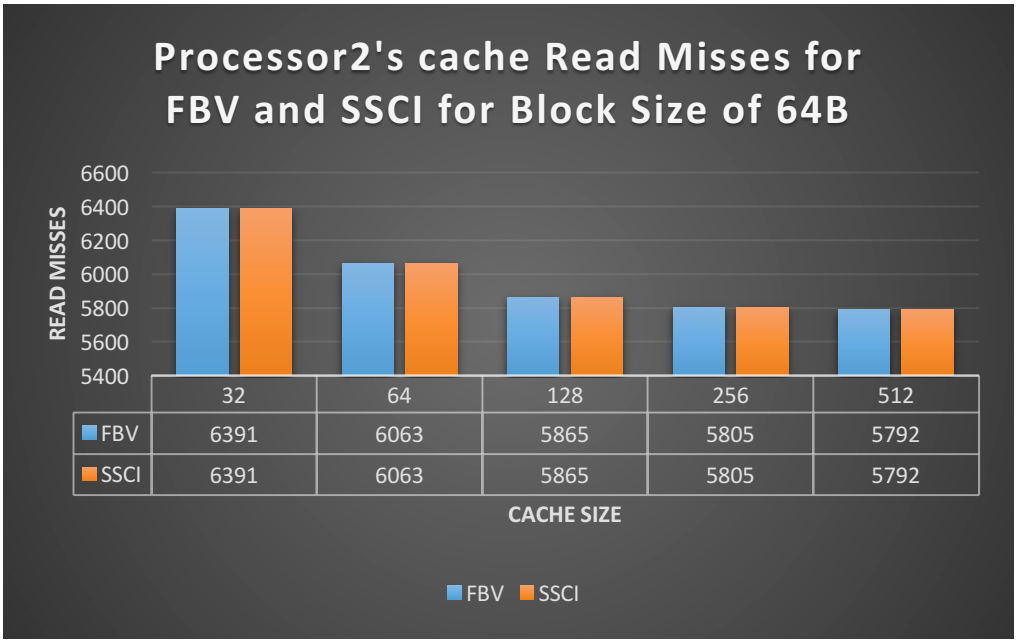
The project deals with important parameters like SignalRd, SignalRdX, Invalidations, Interventions etc. to evaluate the performance of the DSM system based on the different cache block size, cache size etc.

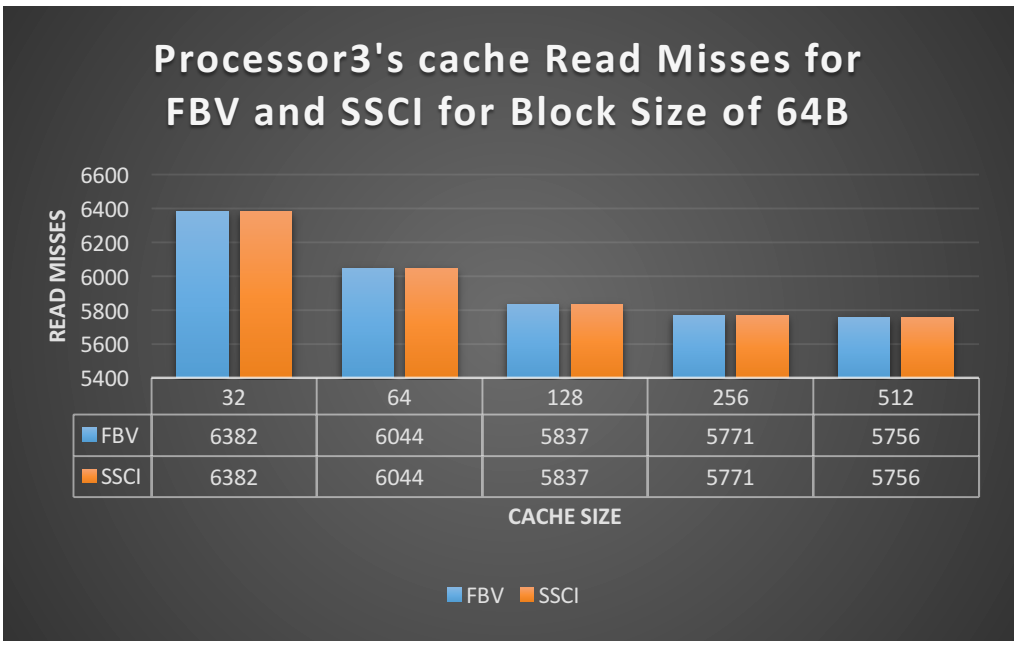
2. REPORT

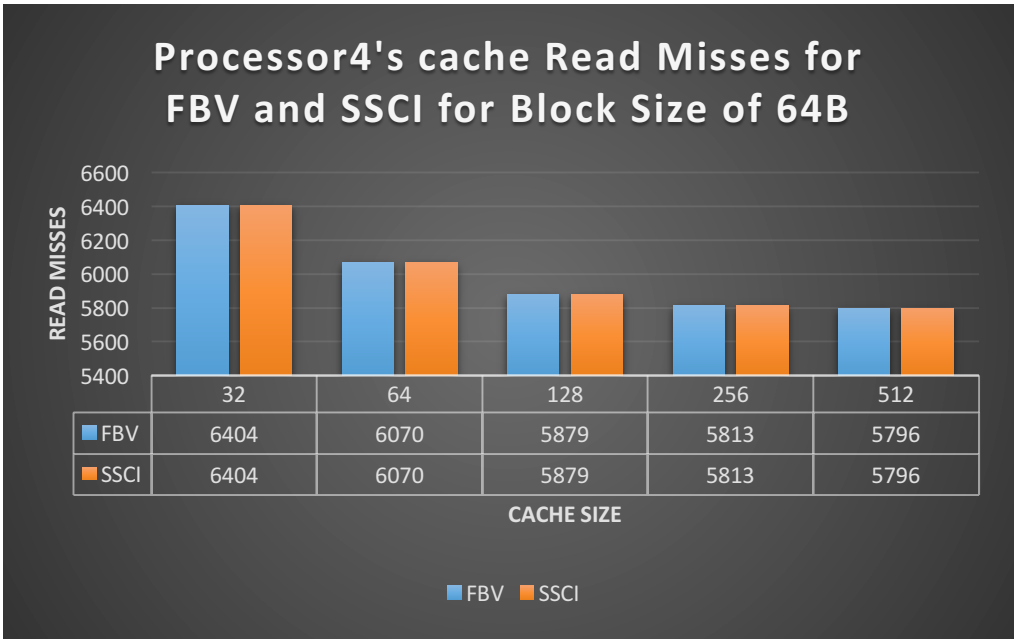
2.1 Effect of Cache Size on Read misses

As we can see, the general trend is number of read misses reduce with increase in cache size. This is due to reduced capacity misses with the increase in the cache size.



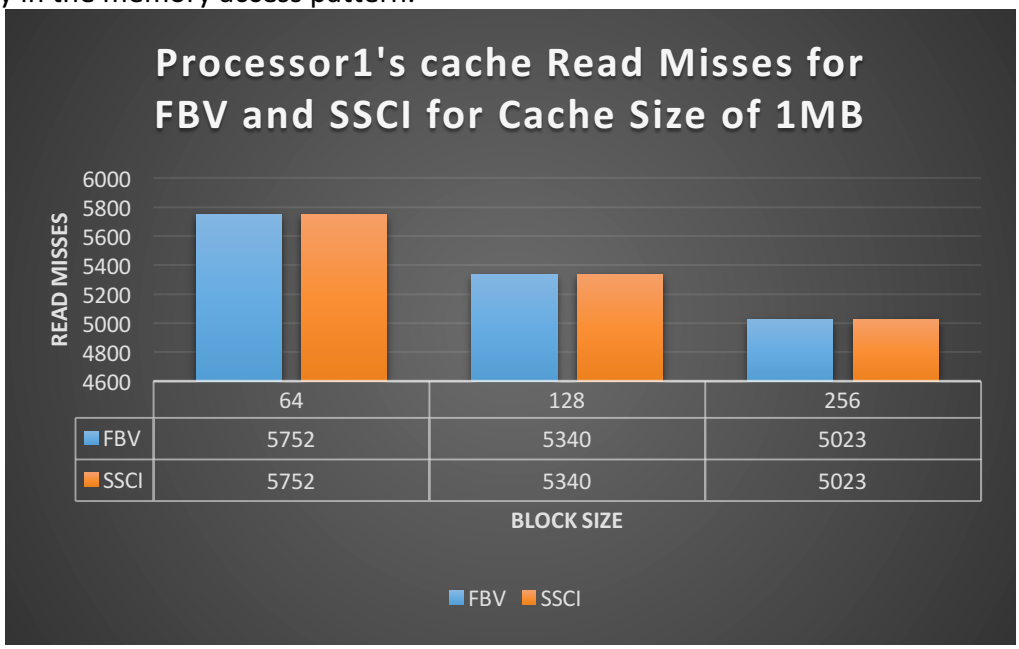


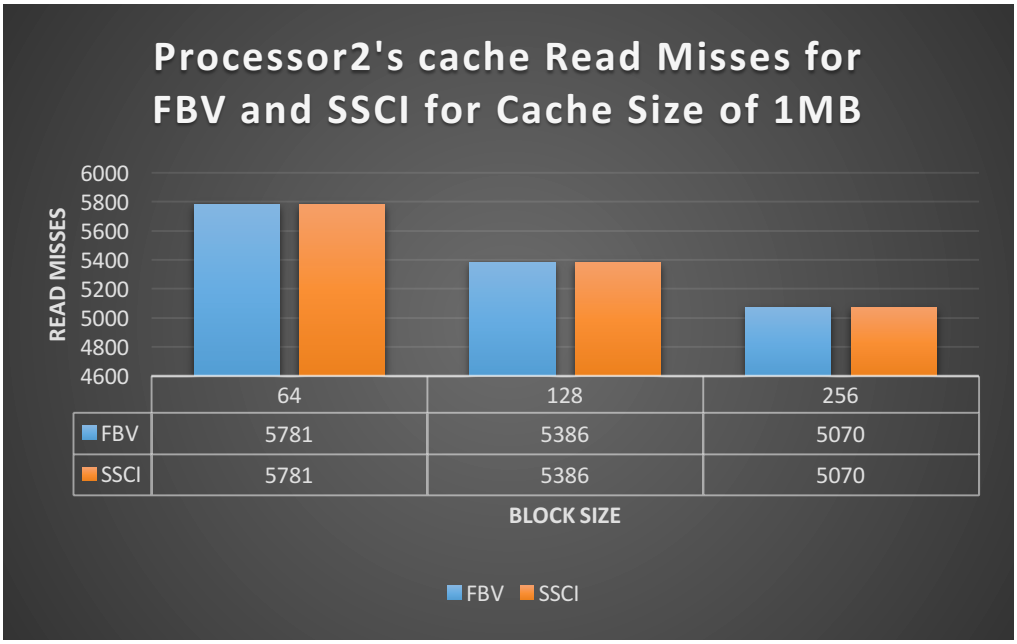

Processor3's cache Read Misses for FBV and SSCI for Block Size of 64B
READ MISSES
6600
6400
6200
6000
5800
5600
5400
32 64 128 256 512
FBV 6382 6044 5837 5771 5756
SSCI 6382 6044 5837 5771 5756
CACHE SIZE
FBV SSCI

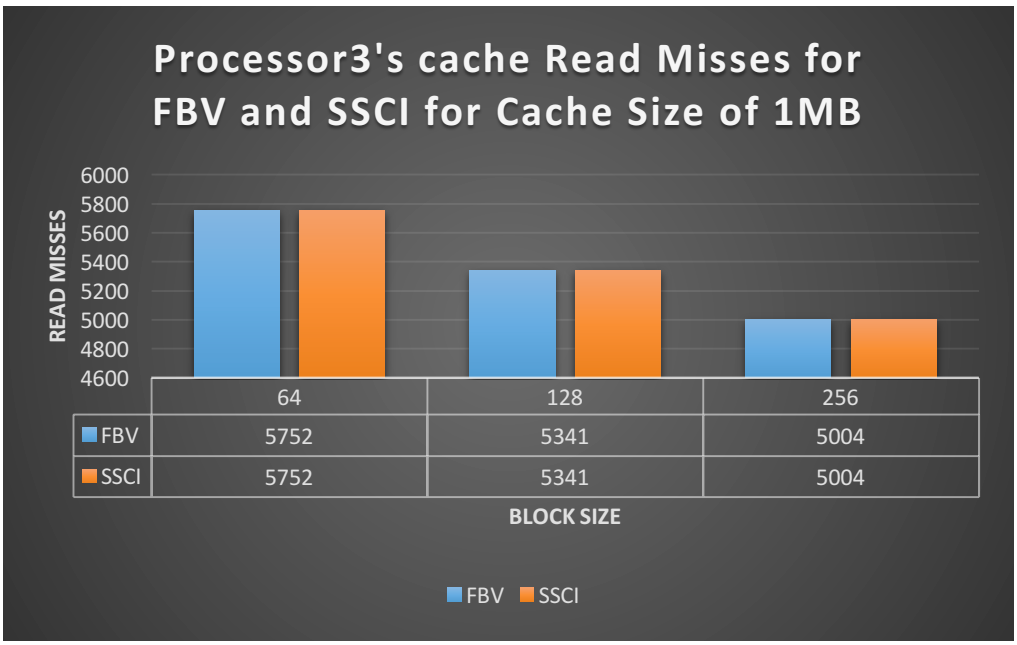

Processor4's cache Read Misses for FBV and SSCI for Block Size of 64B
READ MISSES
6600
6400
6200
6000
5800
5600
5400
32 64 128 256 512
FBV 6404 6070 5879 5813 5796
SSCI 6404 6070 5879 5813 5796
CACHE SIZE
FBV SSCI

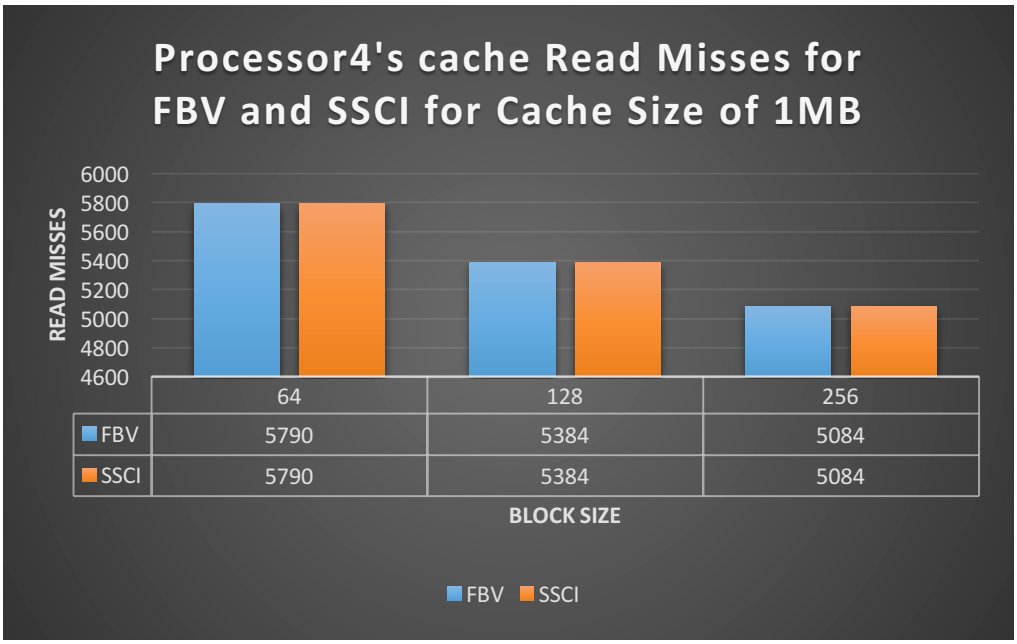
2.2 Effect of Block Size on Read misses

As we can see, the read misses are reduced with increase in block size. This is due to lot of locality in the memory access pattern.



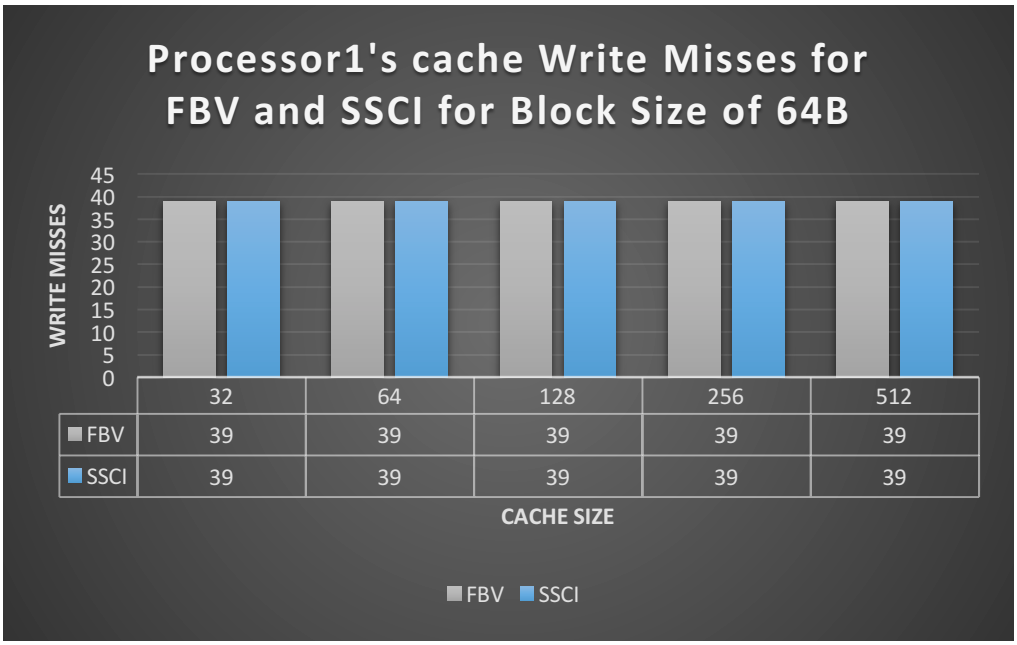


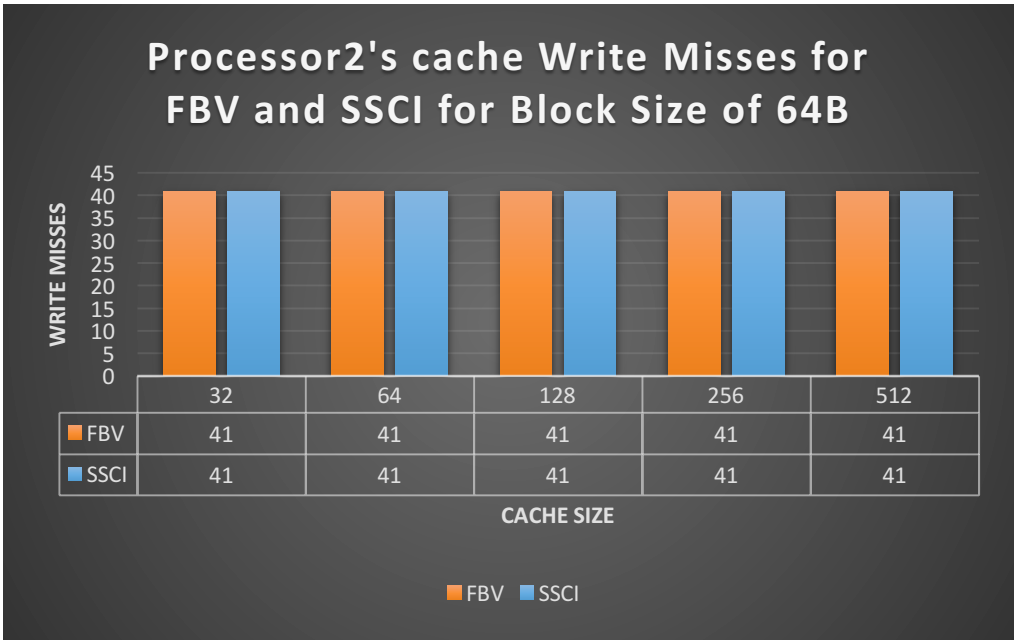

Processor3's cache Read Misses for FBV and SSCI for Cache Size of 1MB
READ MISSES
6000
5800
5600
5400
5200
5000
4800
4600
64
128
256
FBV
5752
5341
5004
SSCI
5752
5341
5004
BLOCK SIZE
FBV
SSCI

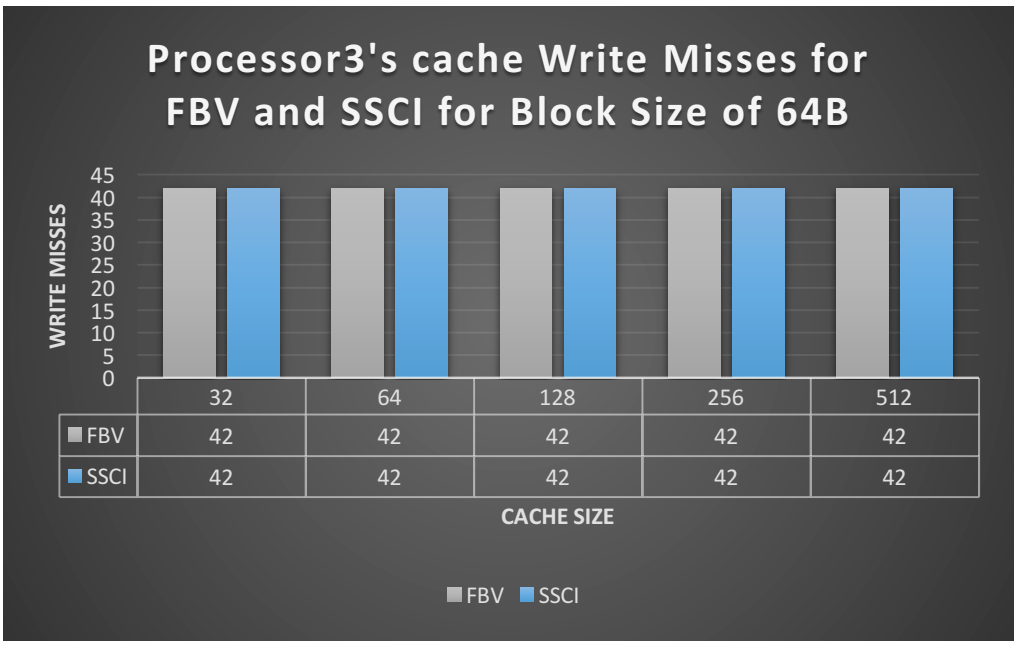

Processor4's cache Read Misses for FBV and SSCI for Cache Size of 1MB
READ MISSES
6000
5800
5600
5400
5200
5000
4800
4600
64
128
256
FBV
5790
5384
5084
SSCI
5790
5384
5084
BLOCK SIZE
FBV
SSCI

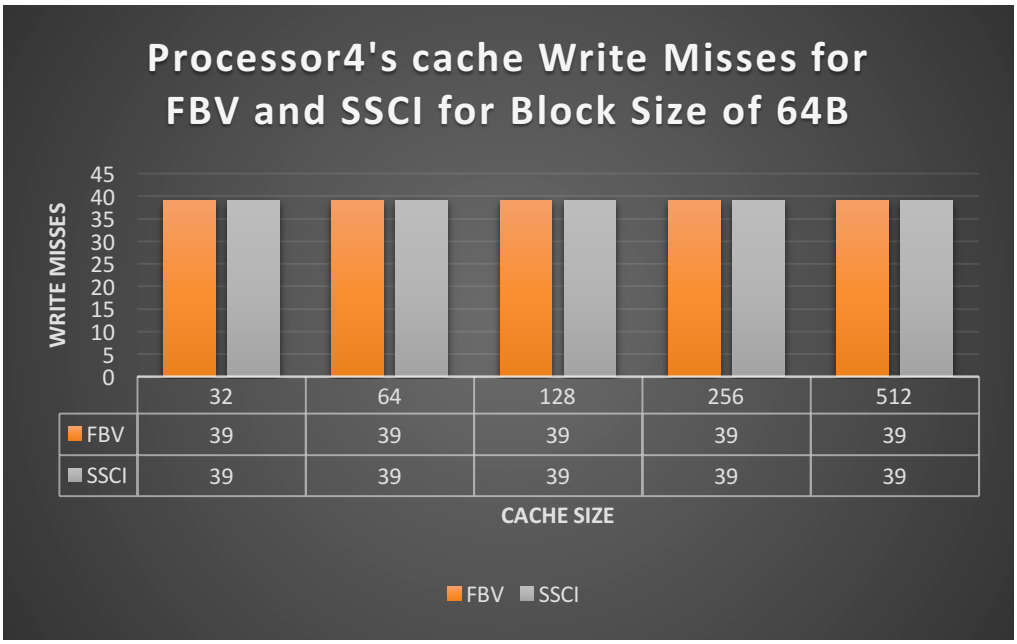
2.3 Effect of Cache Size on Write Misses

Number of write misses seems to not have any effect for the given trace file. The expected effect should be decrease in the write misses.



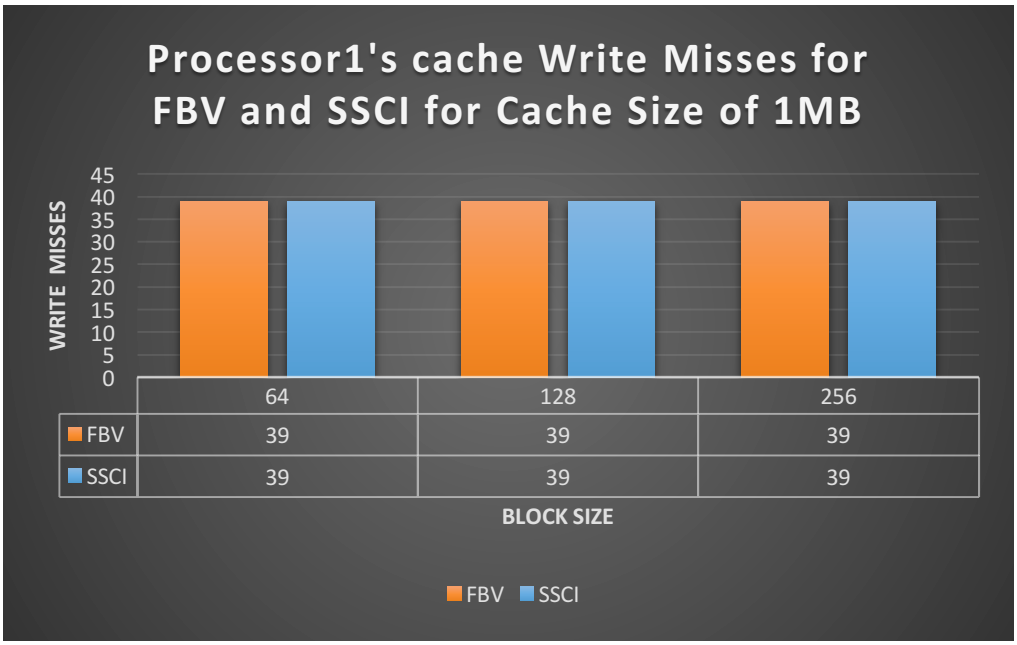


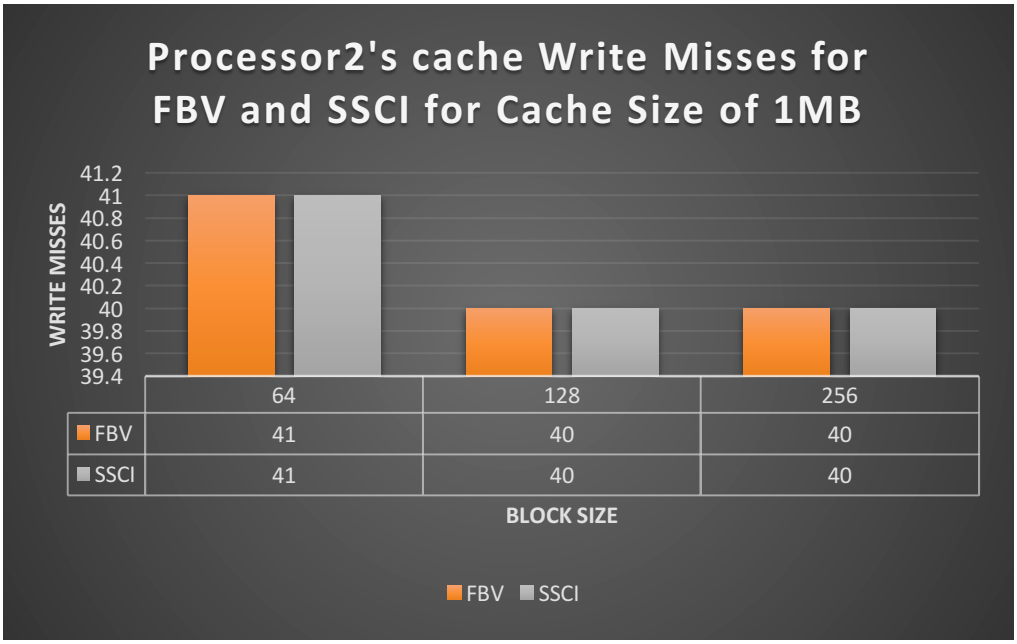

Processor3's cache Write Misses for FBV and SSCI for Block Size of 64B
WRITE MISSES
45
40
35
30
25
20
15
10
5
0
32 64 128 256 512
FBV 42 42 42 42 42
SSCI 42 42 42 42 42
CACHE SIZE
FBV SSCI

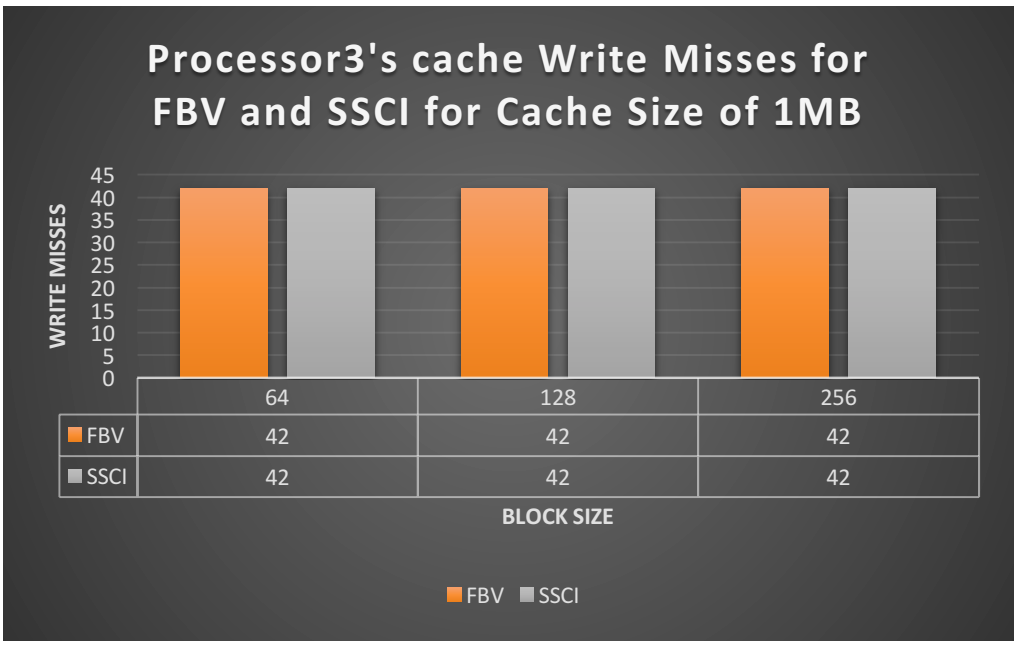

Processor4's cache Write Misses for FBV and SSCI for Block Size of 64B
WRITE MISSES
45
40
35
30
25
20
15
10
5
0
32 64 128 256 512
FBV 39 39 39 39 39
SSCI 39 39 39 39 39
CACHE SIZE
FBV SSCI

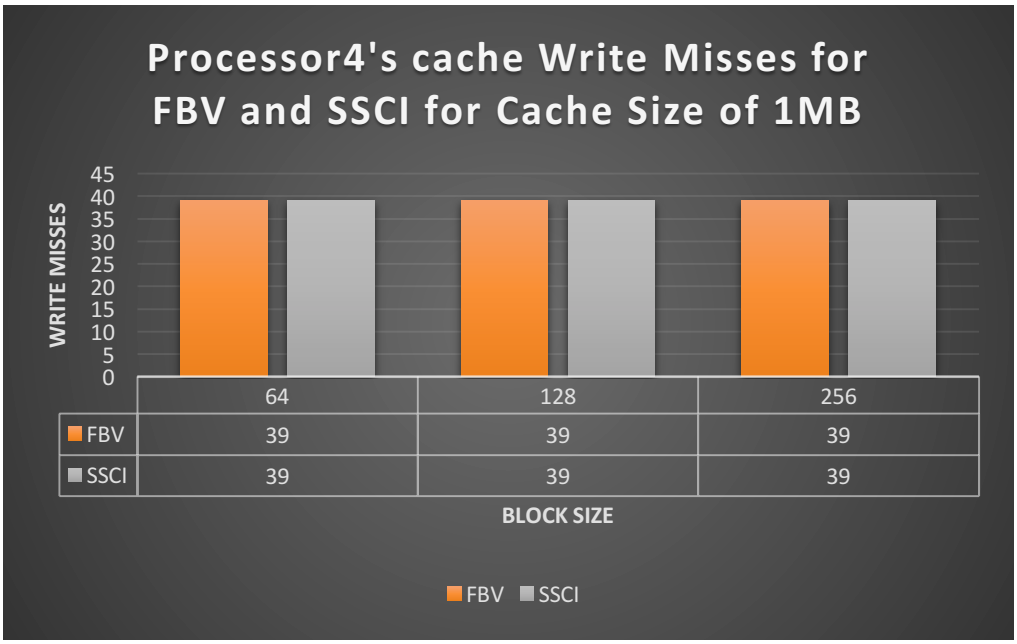
2.4 Effect of Block Size on Write misses

Block size seem to have no effect on write misses for the given trace file.



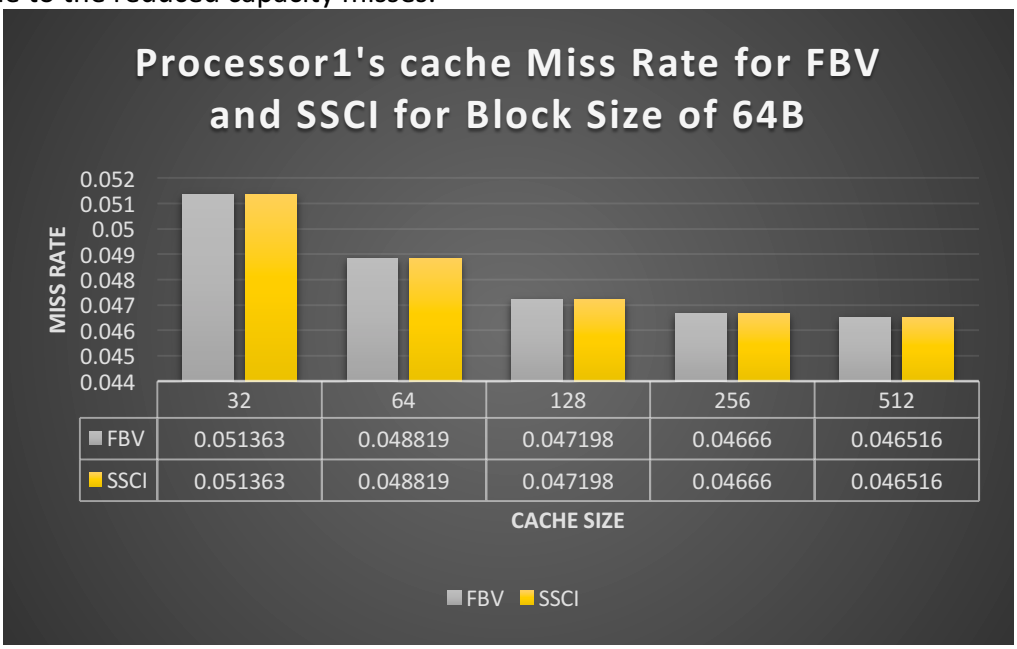



Processor3's cache Write Misses for FBV and SSCI for Cache Size of 1MB
WRITE MISSES
45
40
35
30
25
20
15
10
5
0
64
128
256
FBV
42
42
42
SSCI
42
42
42
BLOCK SIZE
FBV
SSCI

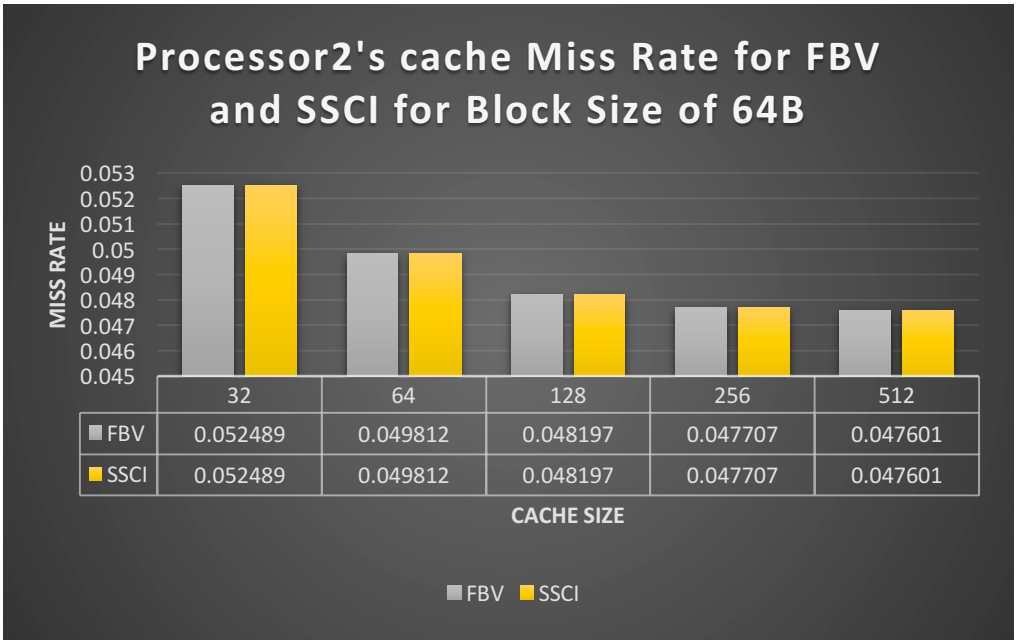

Processor4's cache Write Misses for FBV and SSCI for Cache Size of 1MB
WRITE MISSES
45
40
35
30
25
20
15
10
5
0
64
128
256
FBV
39
39
39
SSCI
39
39
39
BLOCK SIZE
FBV
SSCI

2.5 Effect of Cache Size on Total Miss Rate

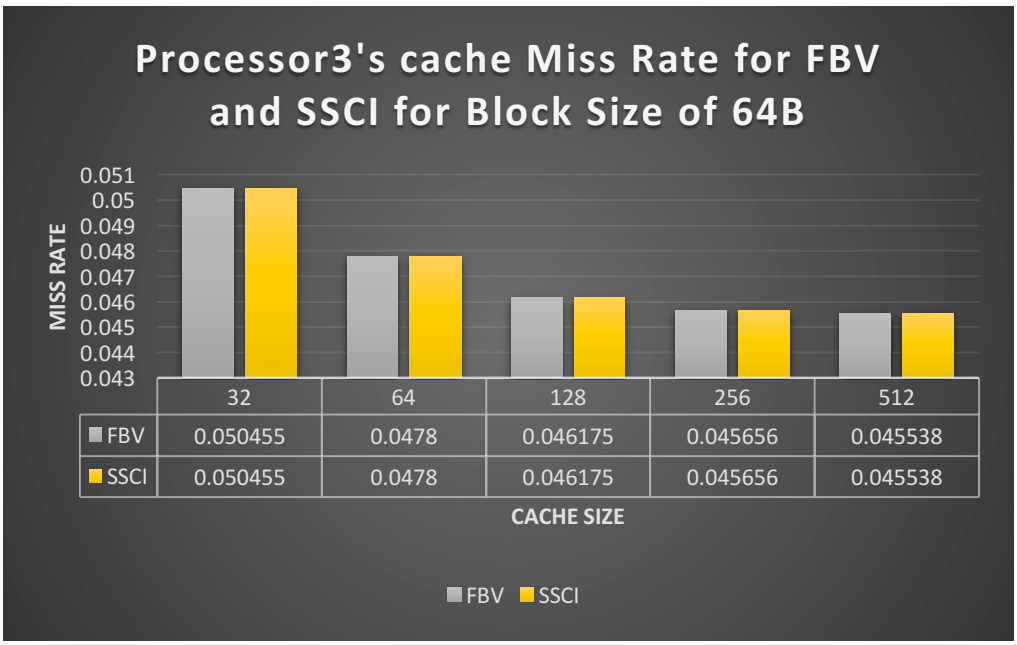
The general trend we can see is, miss rate decreasing with increase in the cache size. This is due to the reduced capacity misses.

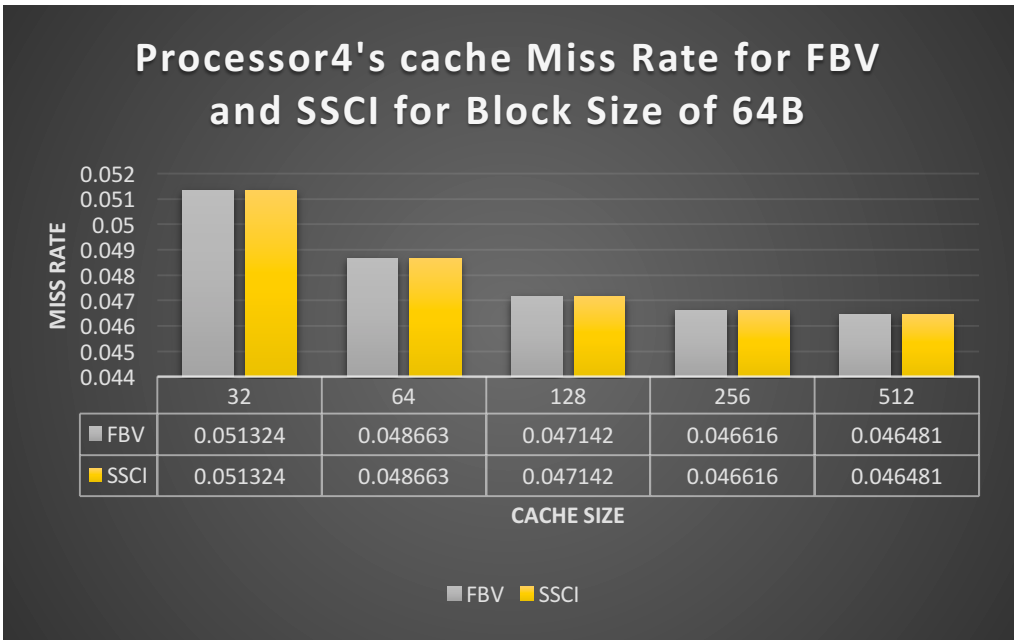


	32	64	128	256	512
FBV	0.051363	0.048819	0.047198	0.04666	0.046516
SSCI	0.051363	0.048819	0.047198	0.04666	0.046516



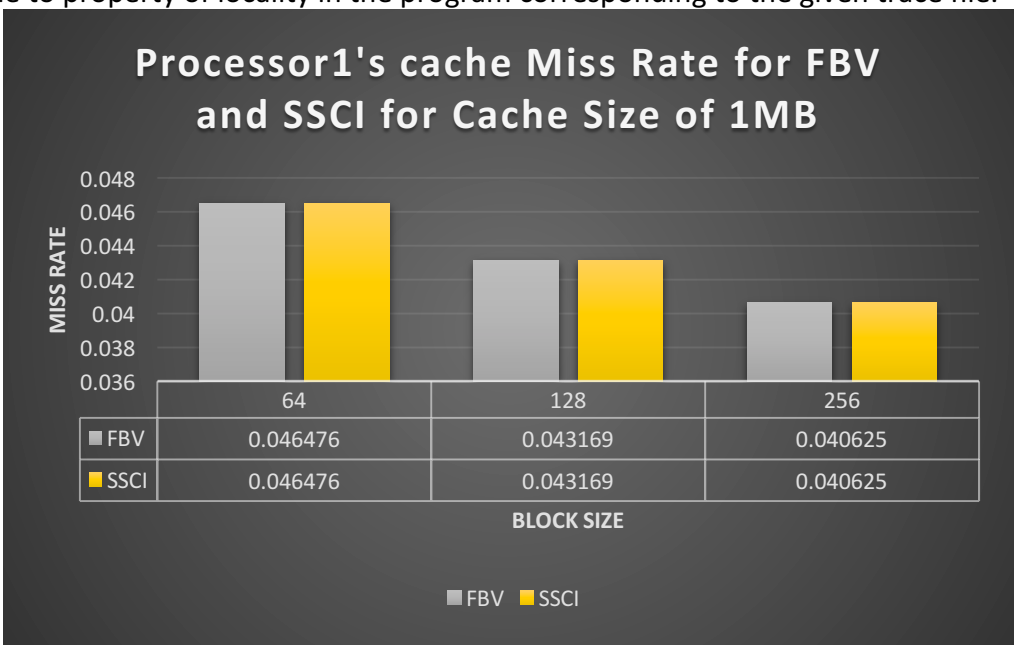
	32	64	128	256	512
FBV	0.052489	0.049812	0.048197	0.047707	0.047601
SSCI	0.052489	0.049812	0.048197	0.047707	0.047601

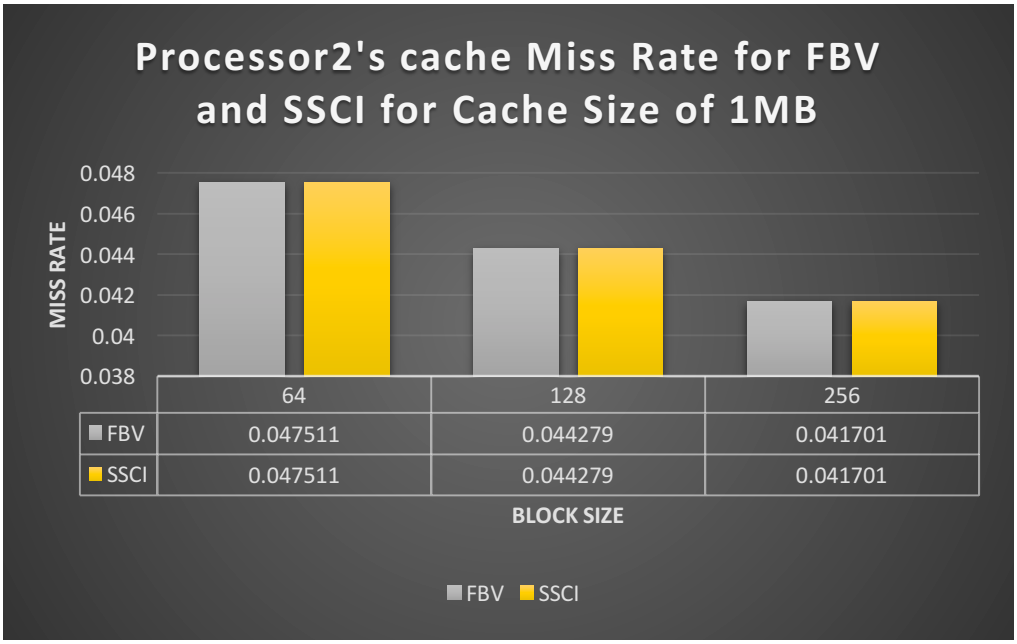

Processor3's cache Miss Rate for FBV and SSCI for Block Size of 64B
MISS RATE
0.051
0.05
0.049
0.048
0.047
0.046
0.045
0.044
0.043
32 64 128 256 512
FBV 0.050455 0.0478 0.046175 0.045656 0.045538
SSCI 0.050455 0.0478 0.046175 0.045656 0.045538
CACHE SIZE
FBV SSCI

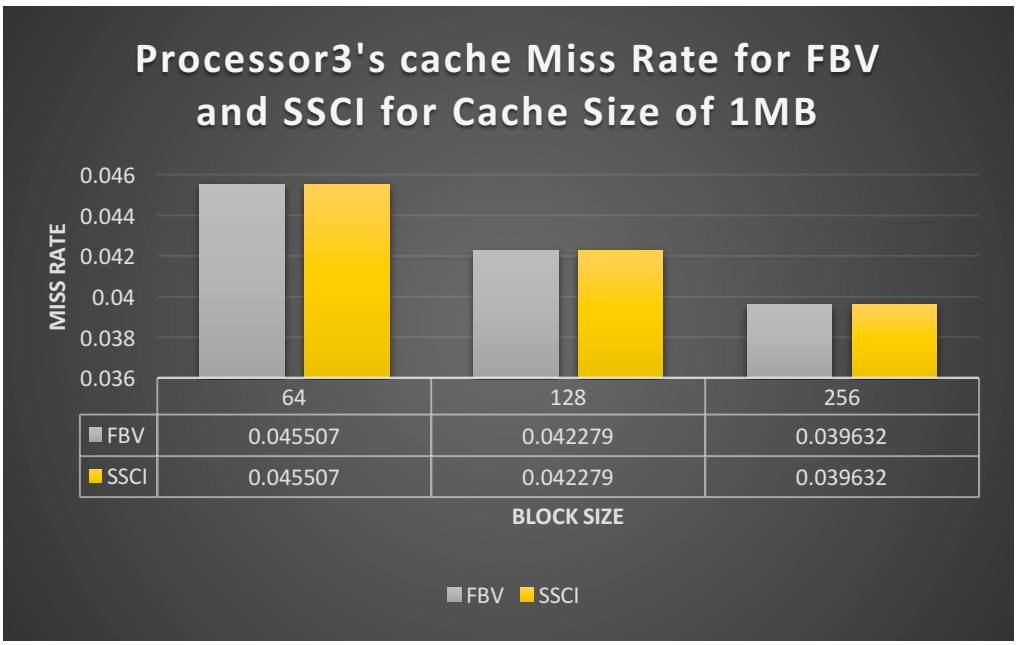

Processor4's cache Miss Rate for FBV and SSCI for Block Size of 64B
MISS RATE
0.052
0.051
0.05
0.049
0.048
0.047
0.046
0.045
0.044
32 64 128 256 512
FBV 0.051324 0.048663 0.047142 0.046616 0.046481
SSCI 0.051324 0.048663 0.047142 0.046616 0.046481
CACHE SIZE
FBV SSCI

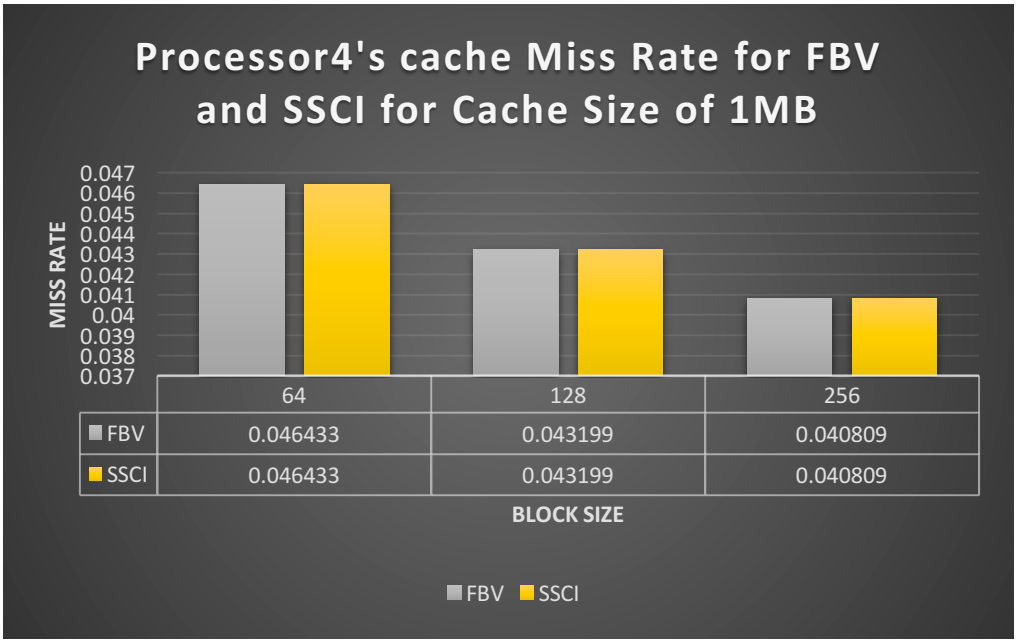
2.6 Effect of Block Size on Total Miss Rate

The trend we can observe here is decrease in the miss rate with increase in the block size. This is due to property of locality in the program corresponding to the given trace file.



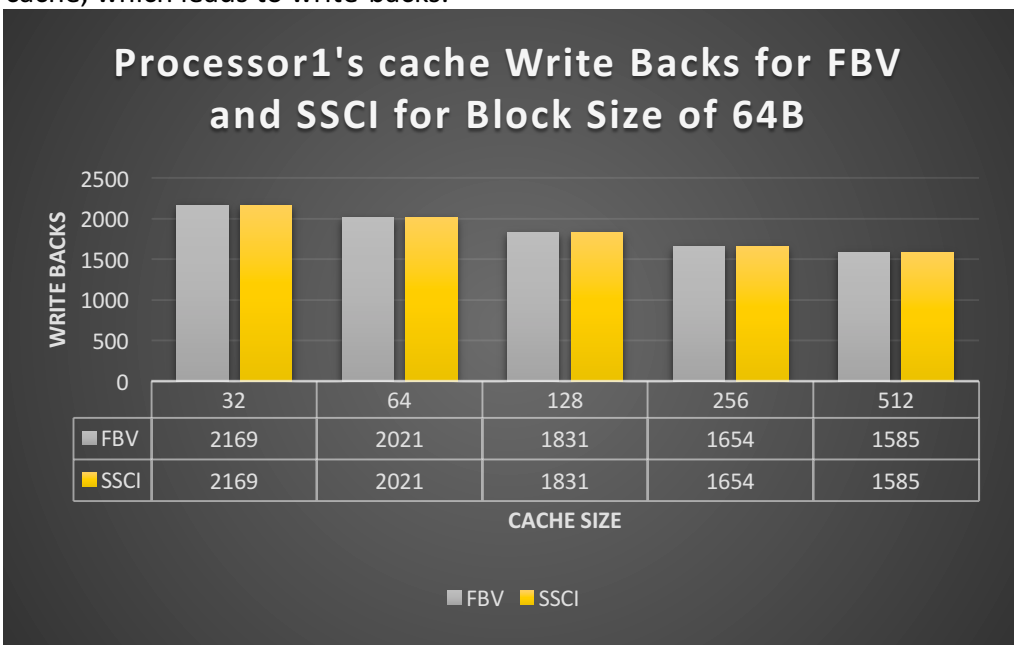


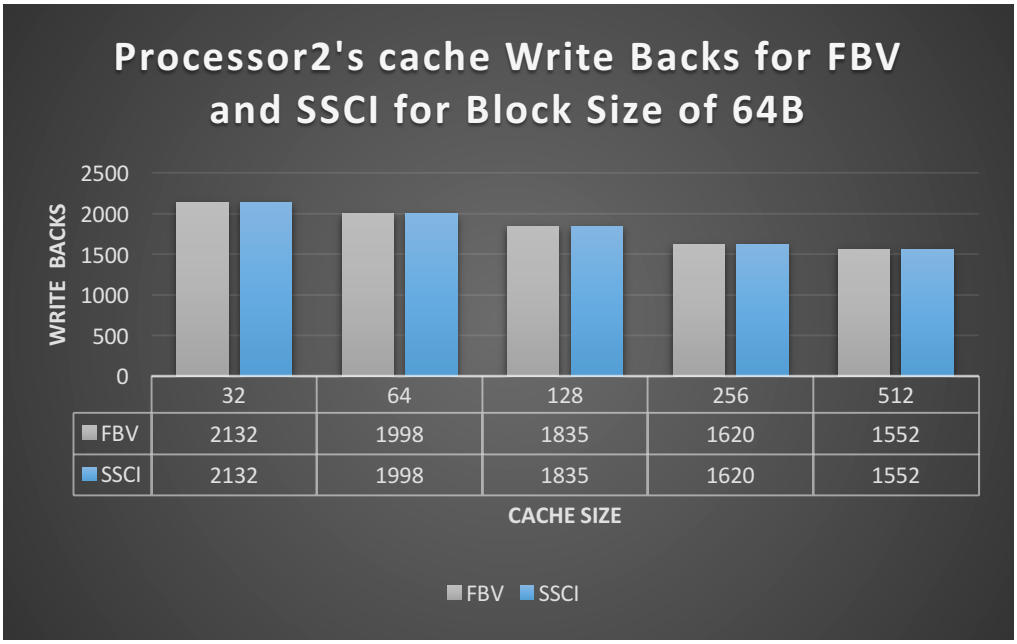

Processor3's cache Miss Rate for FBV and SSCI for Cache Size of 1MB
MISS RATE
0.046
0.044
0.042
0.04
0.038
0.036
64
128
256
FBV
0.045507
0.042279
0.039632
SSCI
0.045507
0.042279
0.039632
BLOCK SIZE
FBV
SSCI

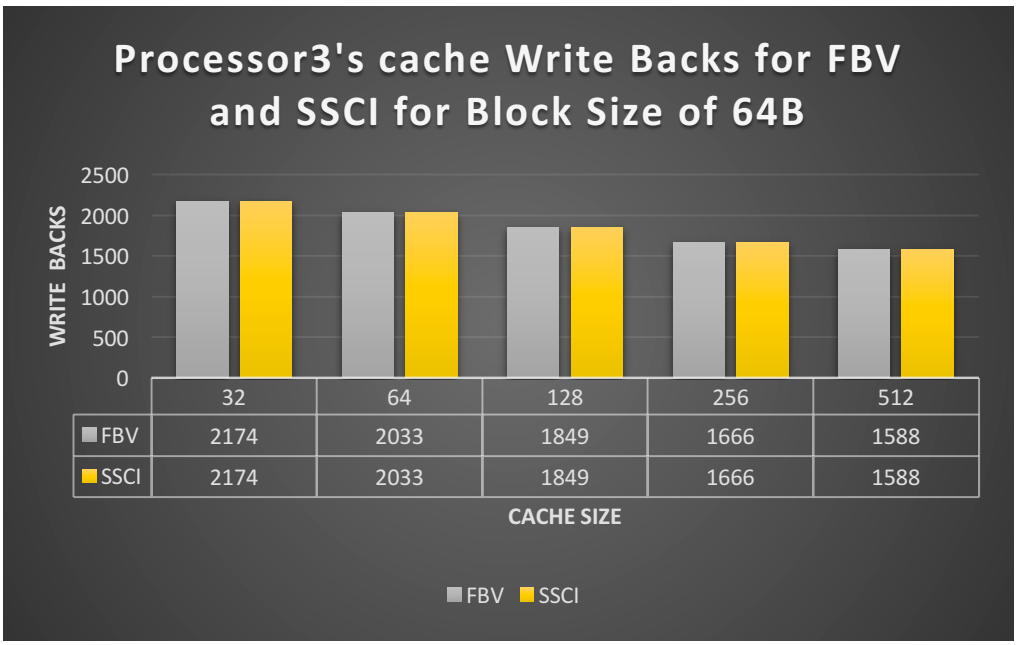

Processor4's cache Miss Rate for FBV and SSCI for Cache Size of 1MB
MISS RATE
0.047
0.046
0.045
0.044
0.043
0.042
0.041
0.04
0.039
0.038
0.037
64
128
256
FBV
0.046433
0.043199
0.040809
SSCI
0.046433
0.043199
0.040809
BLOCK SIZE
FBV
SSCI

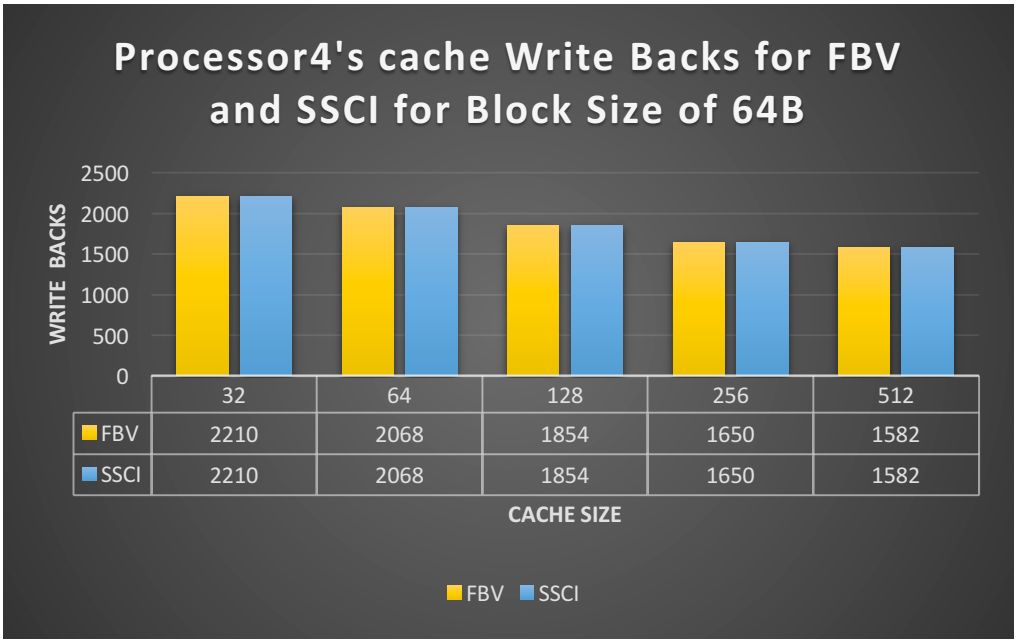
2.7 Effect of Cache Size on number of Writebacks

Here, the write-backs are reducing with increased cache size. This is due to fewer evictions from the cache, which leads to write-backs.



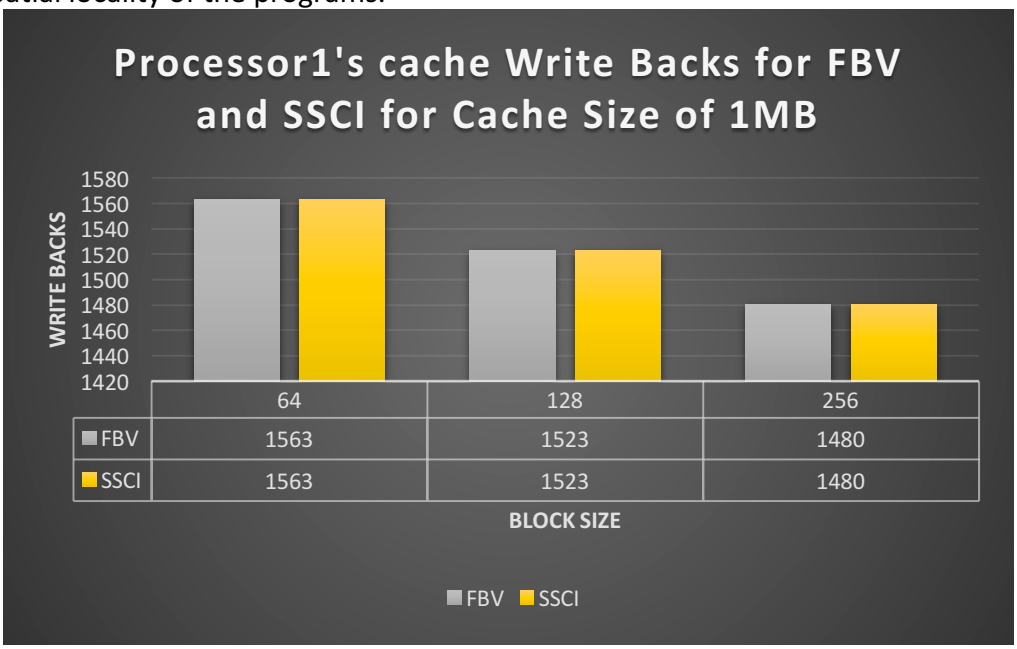


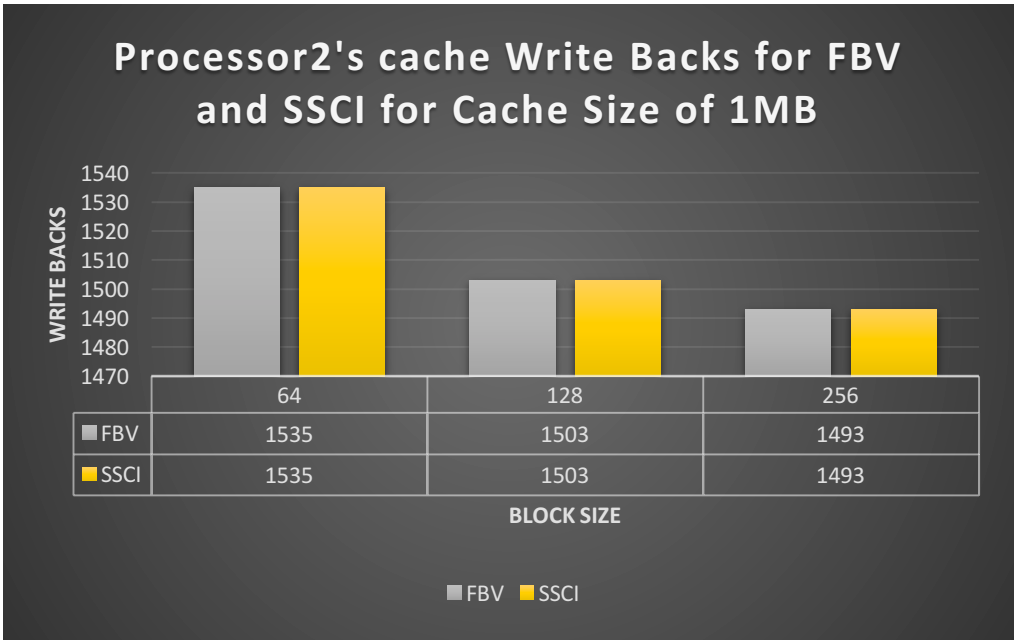

Processor3's cache Write Backs for FBV and SSCI for Block Size of 64B
WRITE BACKS
2500
2000
1500
1000
500
0
32 64 128 256 512
FBV 2174 2033 1849 1666 1588
SSCI 2174 2033 1849 1666 1588
CACHE SIZE
FBV SSCI

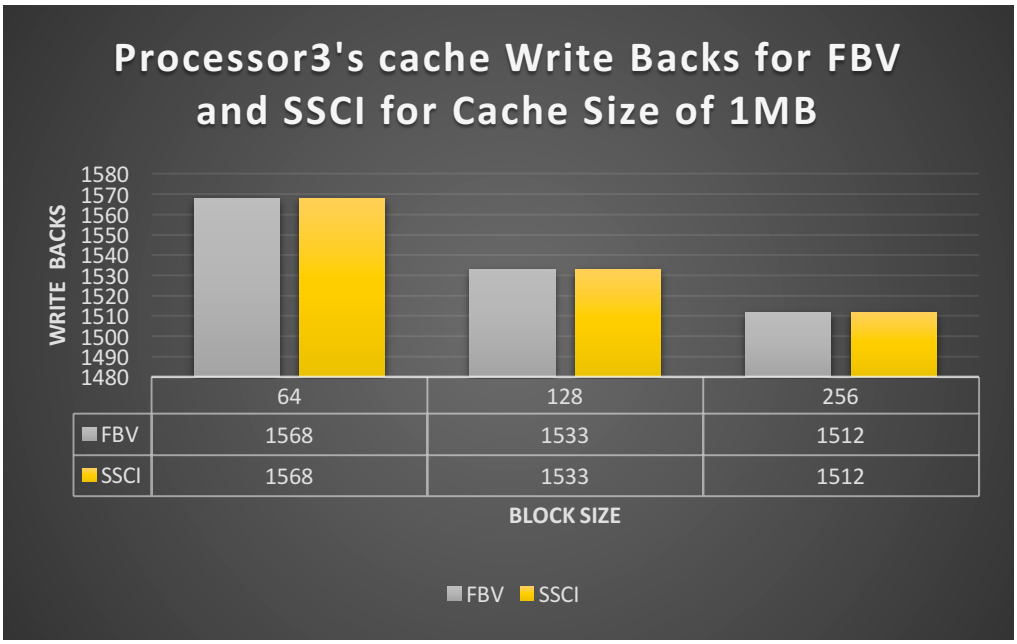

Processor4's cache Write Backs for FBV and SSCI for Block Size of 64B
WRITE BACKS
2500
2000
1500
1000
500
0
32 64 128 256 512
FBV 2210 2068 1854 1650 1582
SSCI 2210 2068 1854 1650 1582
CACHE SIZE
FBV SSCI

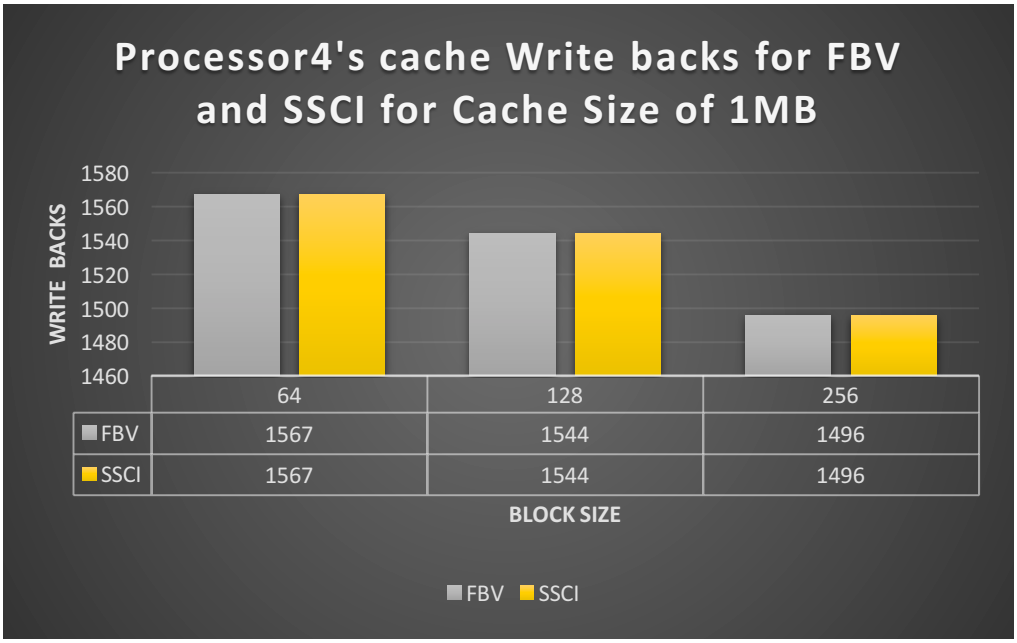
2.8 Effect of Block Size on number of Writebacks

The trend we observe is decrease in write-backs with increase in the block size. This is due to spatial locality of the programs.



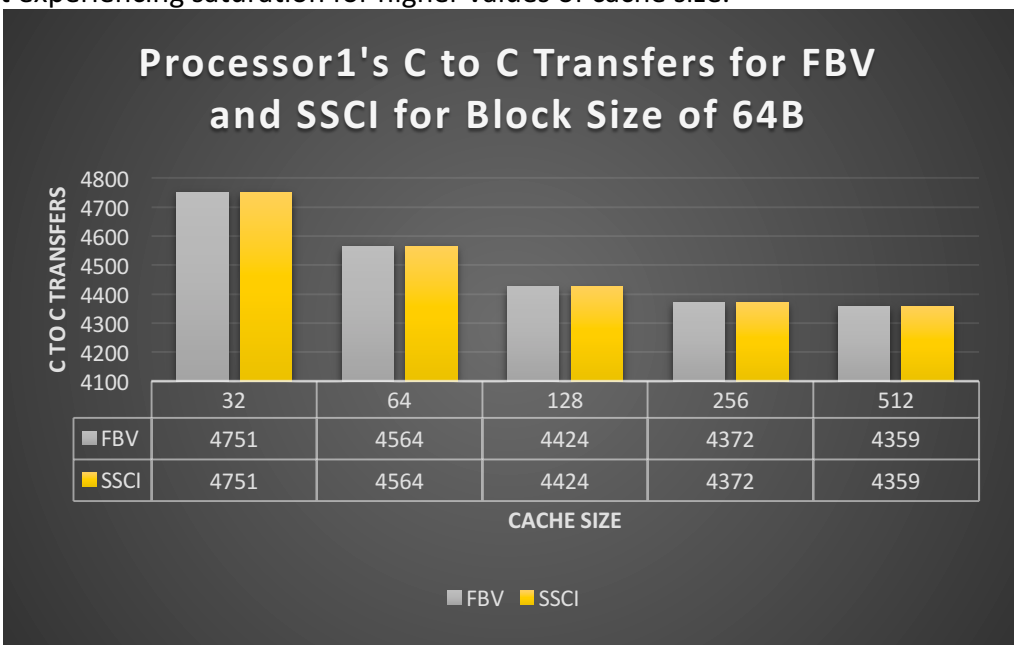


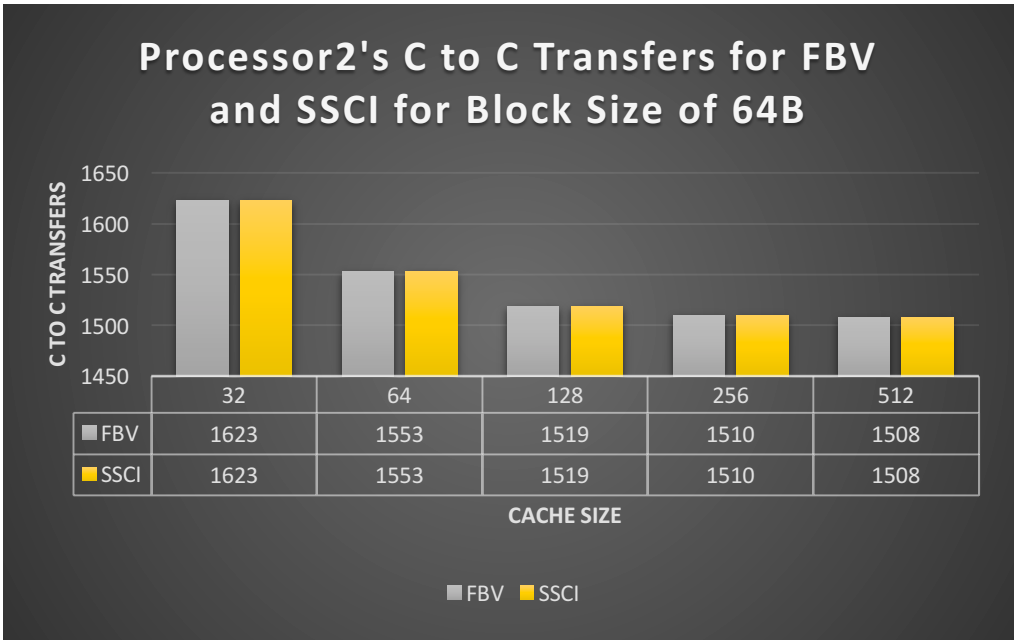

Processor3's cache Write Backs for FBV and SSCI for Cache Size of 1MB
WRITE BACKS
1580
1570
1560
1550
1540
1530
1520
1510
1500
1490
1480
64
128
256
FBV
1568
1533
1512
SSCI
1568
1533
1512
BLOCK SIZE
FBV
SSCI

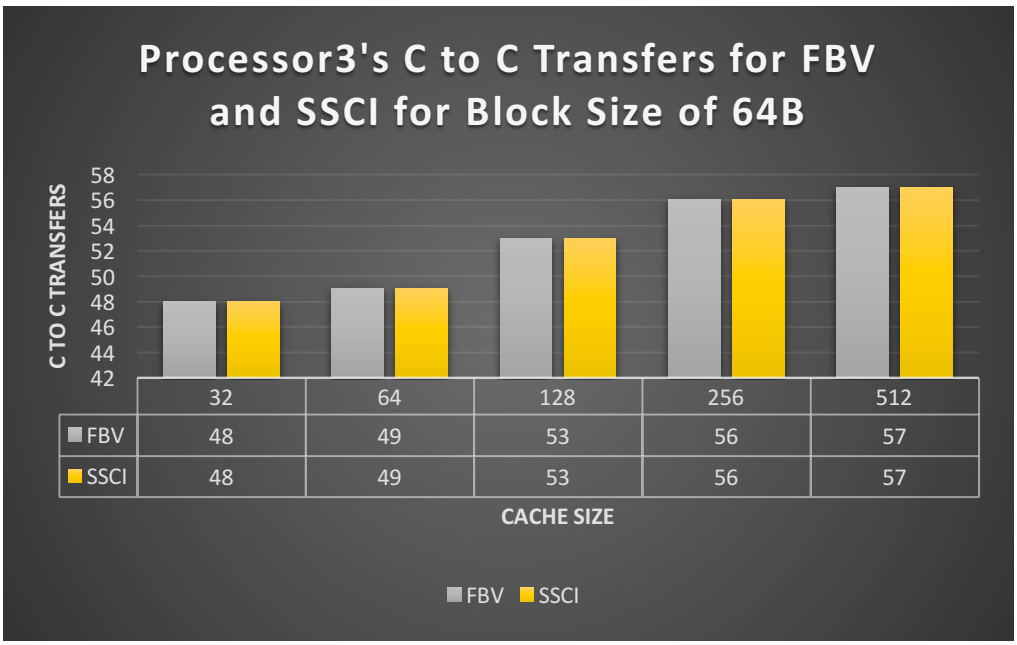

Processor4's cache Write backs for FBV and SSCI for Cache Size of 1MB
WRITE BACKS
1580
1560
1540
1520
1500
1480
1460
64
128
256
FBV
1567
1544
1496
SSCI
1567
1544
1496
BLOCK SIZE
FBV
SSCI

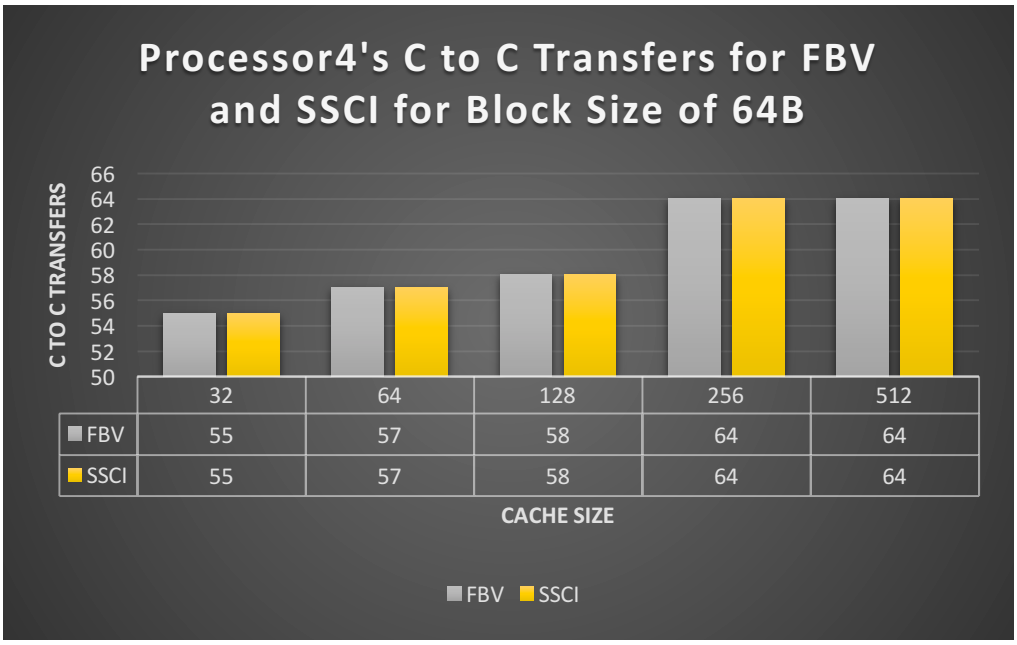
2.9 Effect of Cache Size on Cache to Cache transfers

Caches to cache transfers are decreasing with increase in the cache size. But we can see the effect experiencing saturation for higher values of cache size.



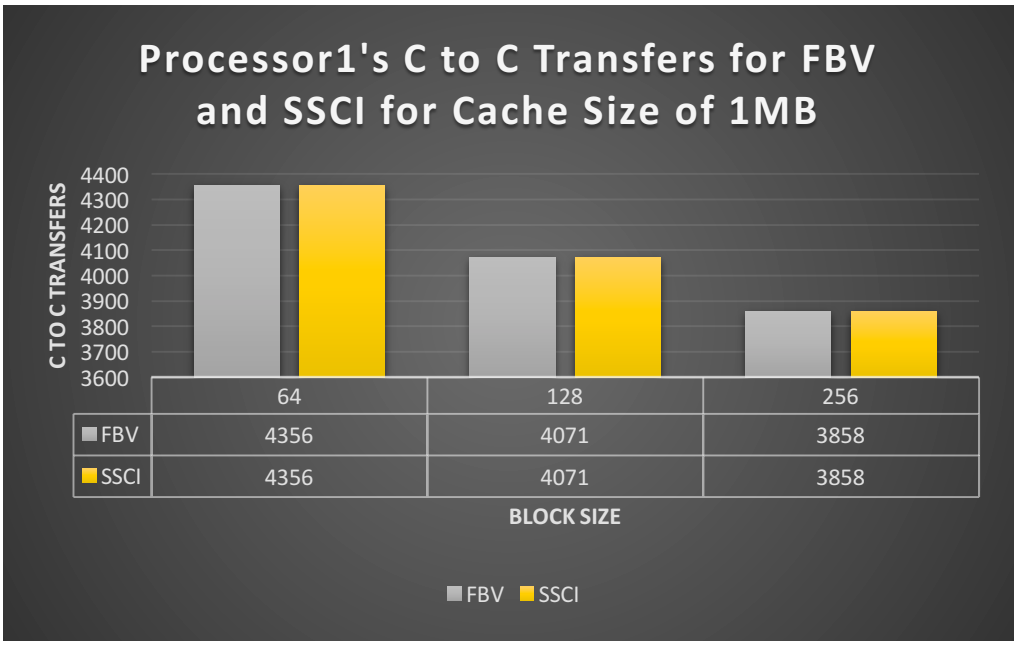


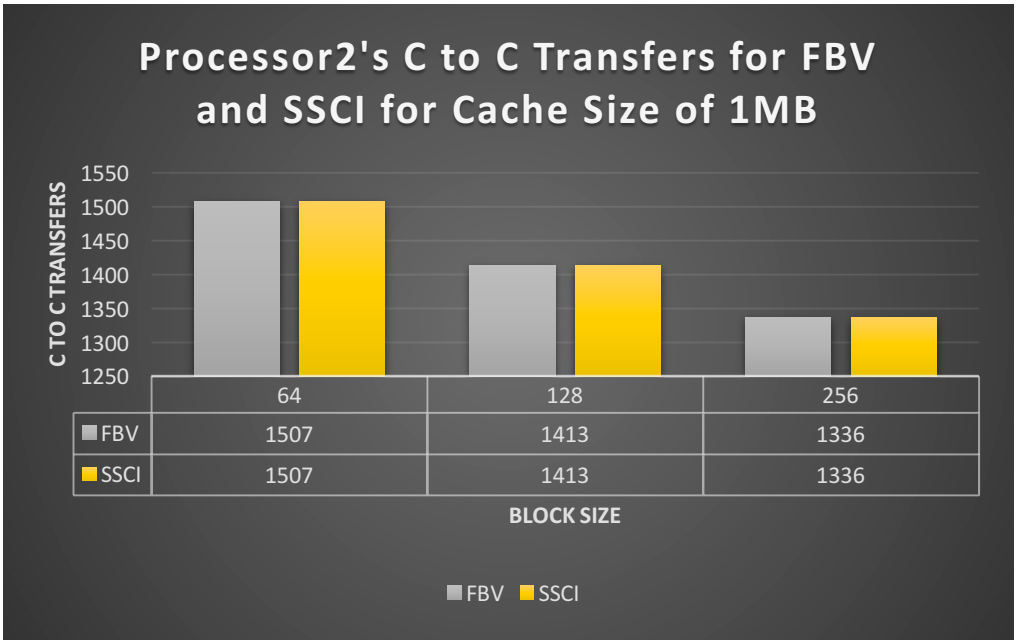

Processor3's C to C Transfers for FBV and SSCI for Block Size of 64B
C TO C TRANSFERS
58
56
54
52
50
48
46
44
42
32 64 128 256 512
FBV 48 49 53 56 57
SSCI 48 49 53 56 57
CACHE SIZE
FBV SSCI

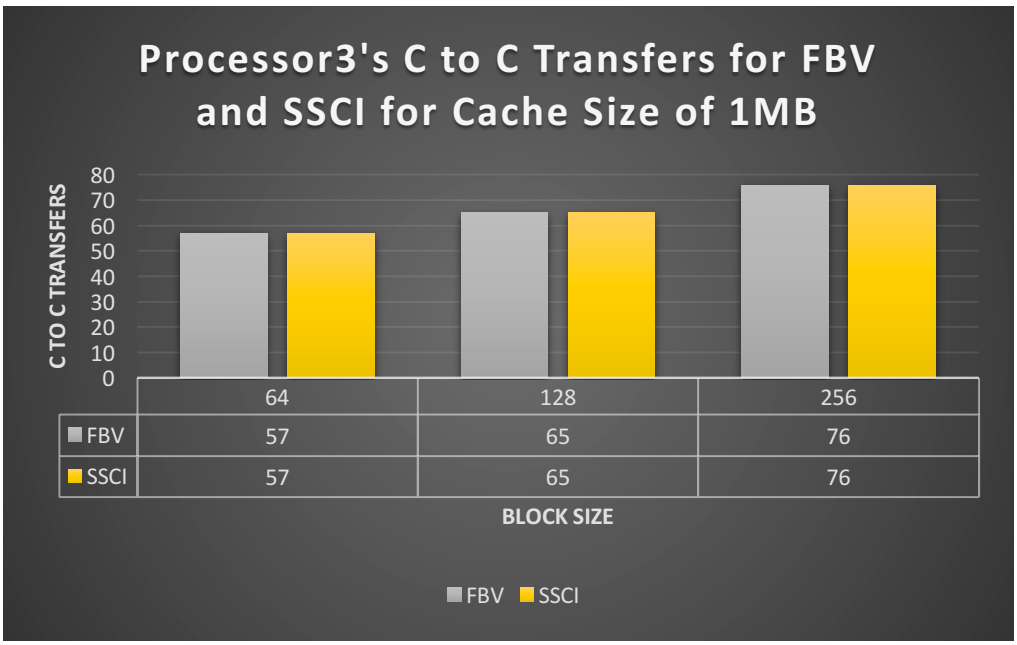

Processor4's C to C Transfers for FBV and SSCI for Block Size of 64B
C TO C TRANSFERS
66
64
62
60
58
56
54
52
50
32 64 128 256 512
FBV 55 57 58 64 64
SSCI 55 57 58 64 64
CACHE SIZE
FBV SSCI

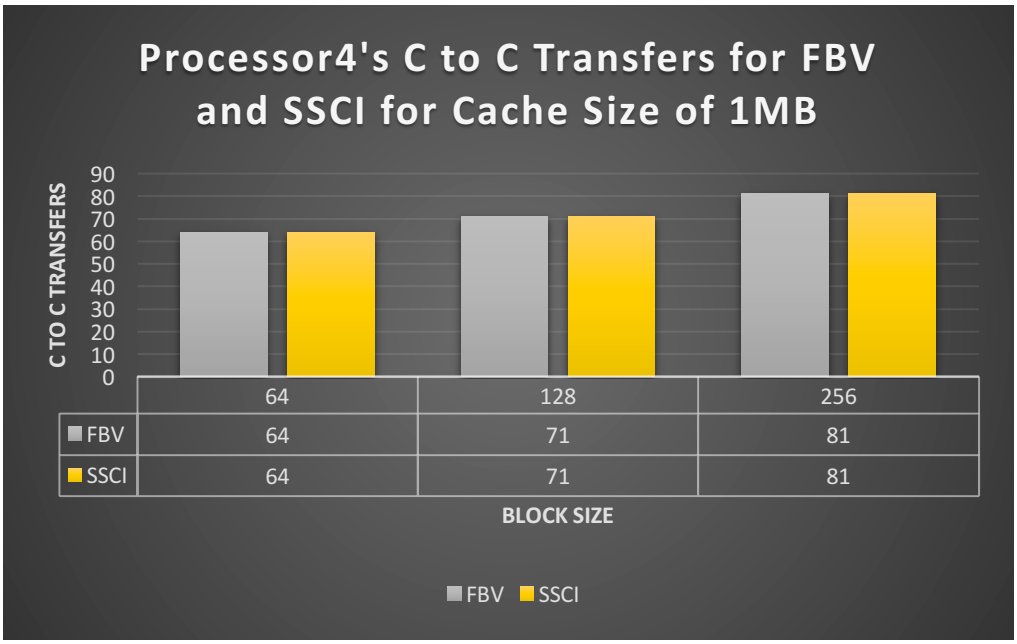
2.10 Effect of Block Size on Cache to Cache Transfers

We can see that cache-to-cache transfer is deceasing with increase in block size. The reason is same as reduced miss rates.



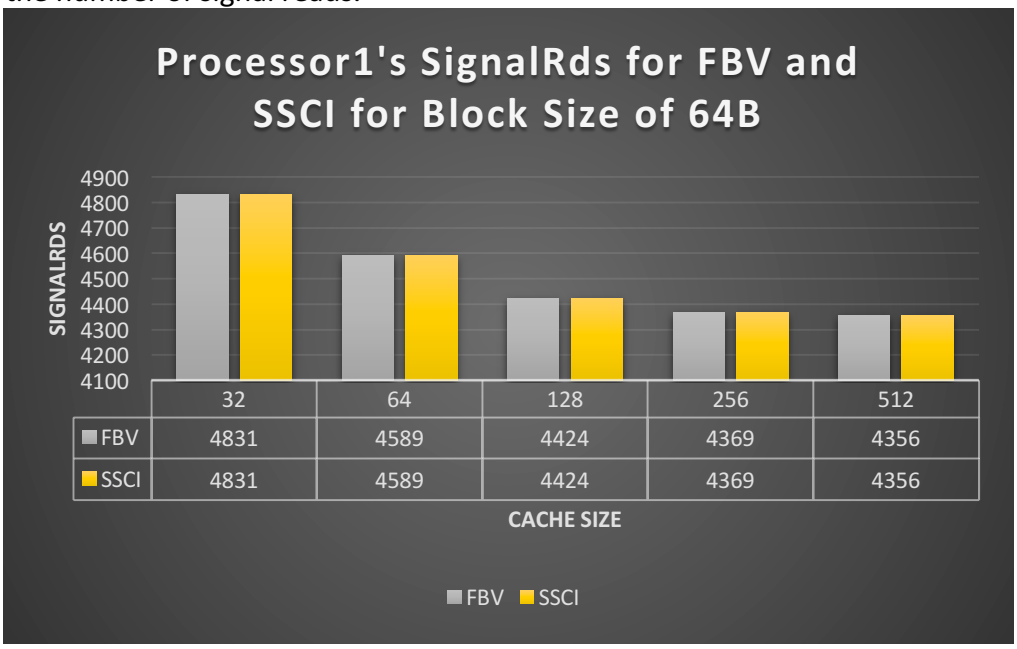


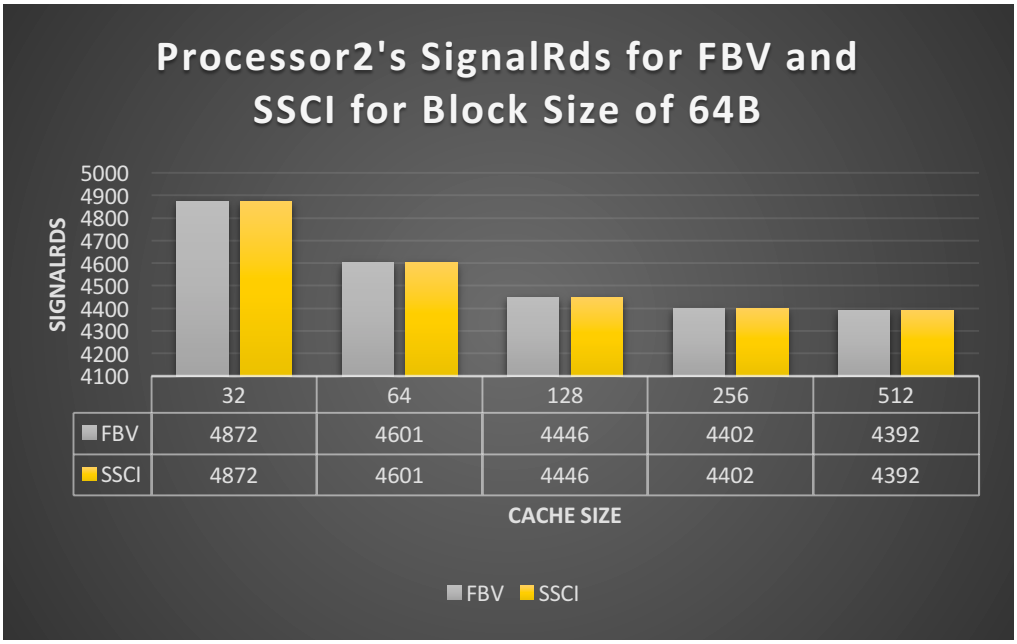

Processor3's C to C Transfers for FBV and SSCI for Cache Size of 1MB
C TO C TRANSFERS
80
70
60
50
40
30
20
10
0
64
128
256
FBV
57
65
76
SSCI
57
65
76
BLOCK SIZE
FBV
SSCI

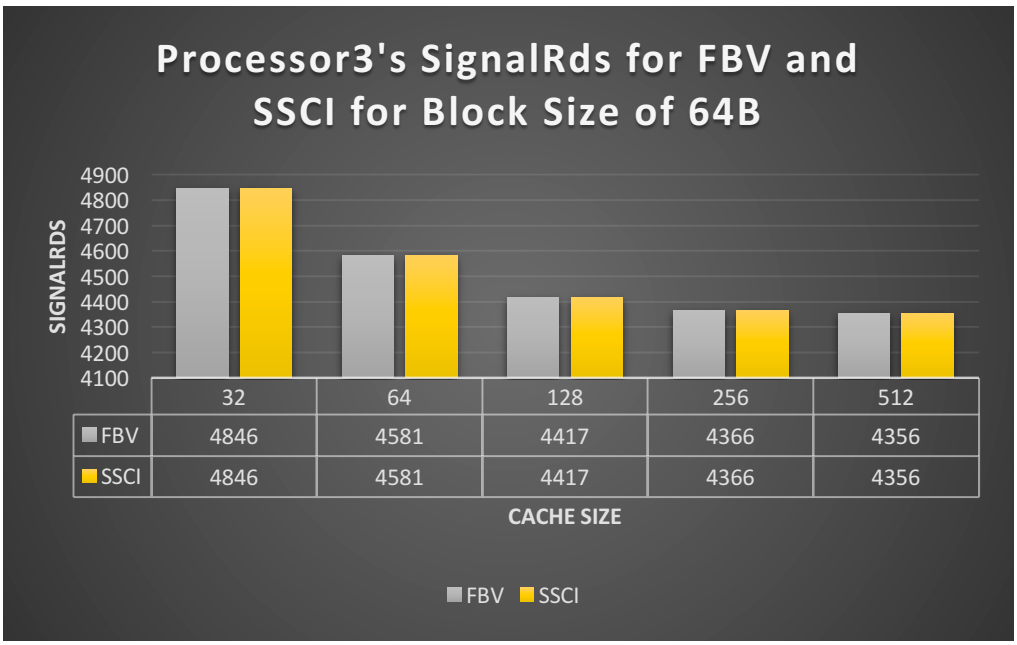

Processor4's C to C Transfers for FBV and SSCI for Cache Size of 1MB
C TO C TRANSFERS
90
80
70
60
50
40
30
20
10
0
64
128
256
FBV
64
71
81
SSCI
64
71
81
BLOCK SIZE
FBV
SSCI

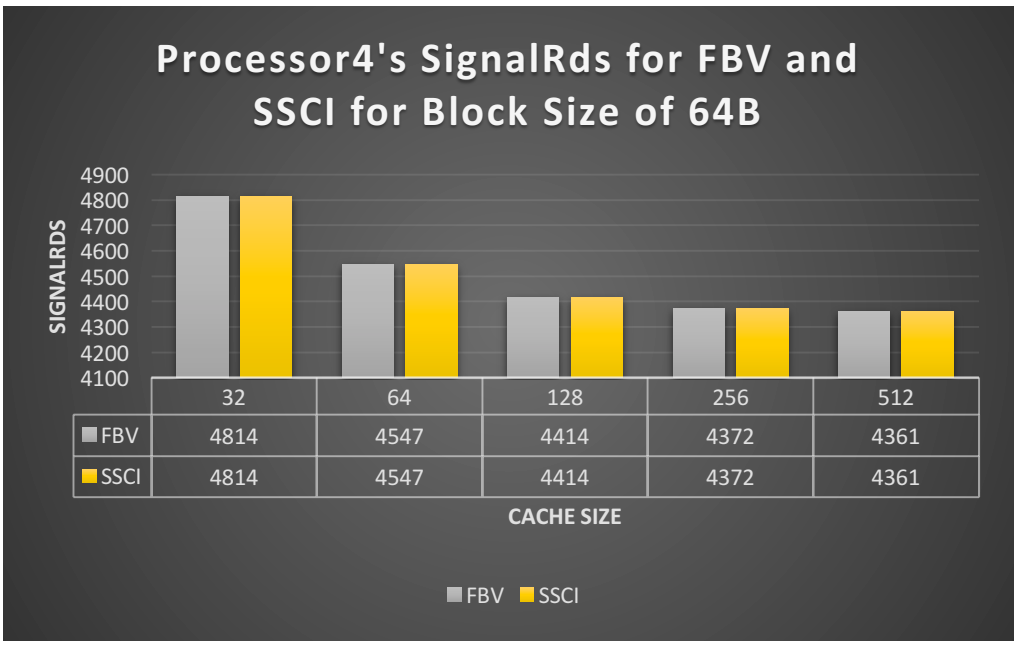
2.11 Effect of Cache Size on SignalRd

The trend is decrease in SignalRd with increase in the cache size. This is due to less capacity misses which leads to less read signals from the requestor to home directory and thus reducing the number of signal reads.



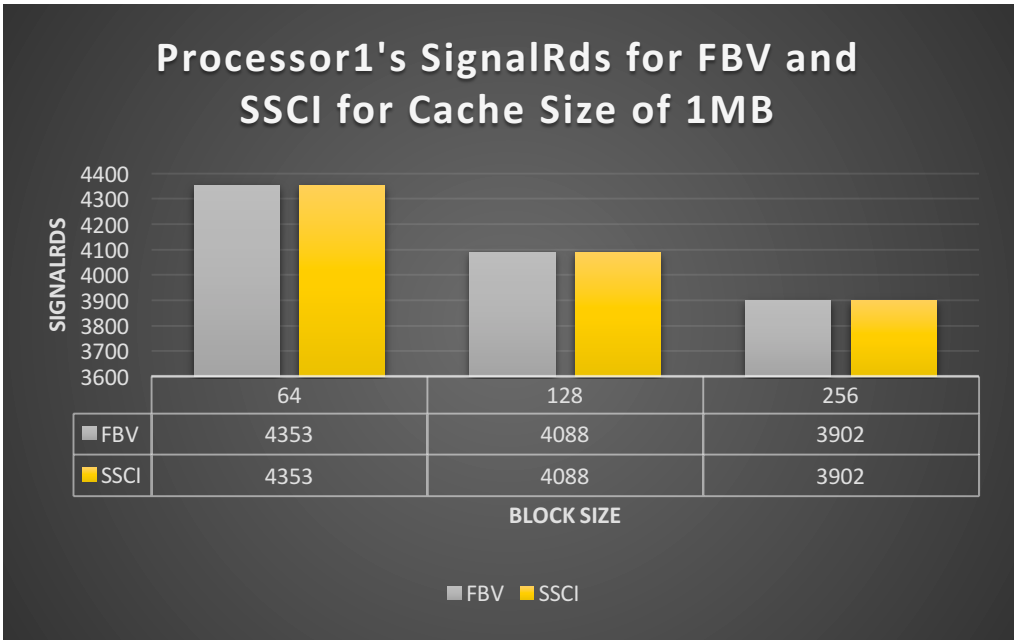


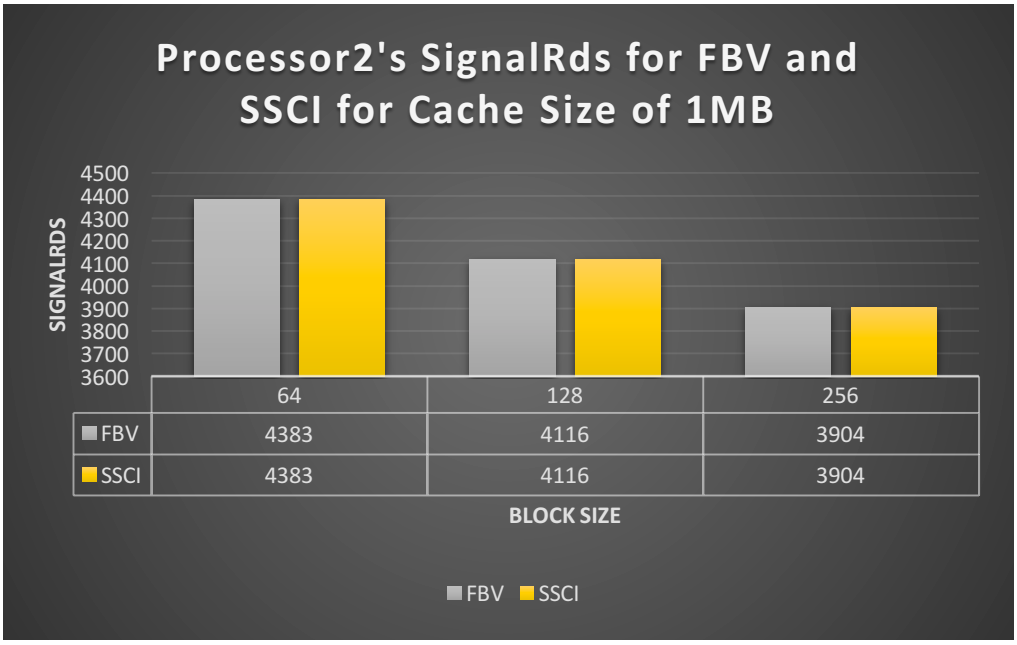

Processor3's SignalRds for FBV and SSCI for Block Size of 64B
SIGNALRDS
4900
4800
4700
4600
4500
4400
4300
4200
4100
32 64 128 256 512
FBV 4846 4581 4417 4366 4356
SSCI 4846 4581 4417 4366 4356
CACHE SIZE
FBV SSCI

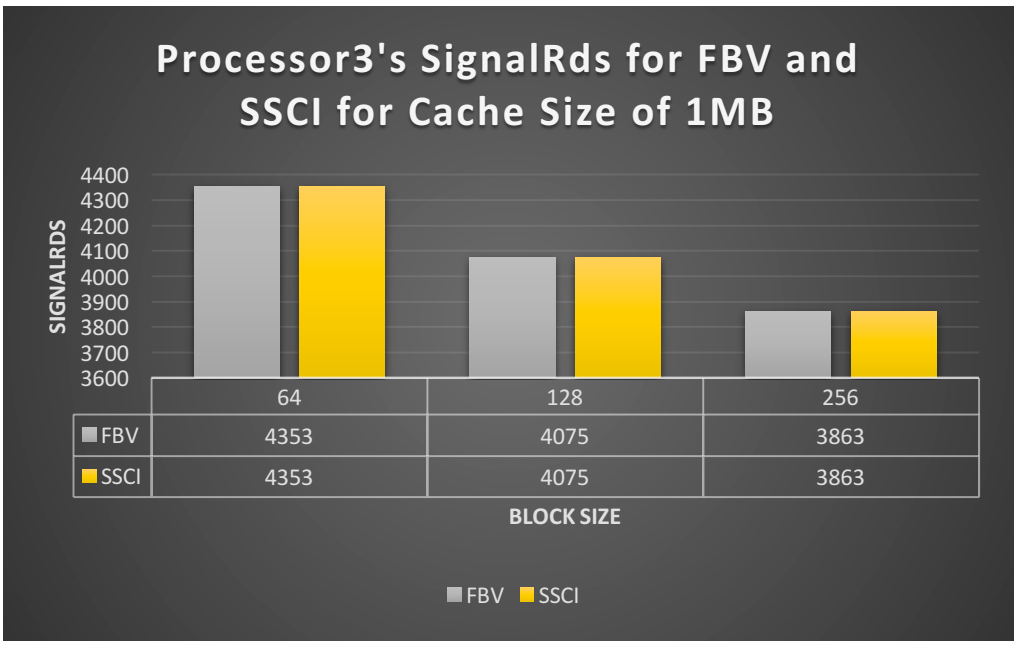

Processor4's SignalRds for FBV and SSCI for Block Size of 64B
SIGNALRDS
4900
4800
4700
4600
4500
4400
4300
4200
4100
32 64 128 256 512
FBV 4814 4547 4414 4372 4361
SSCI 4814 4547 4414 4372 4361
CACHE SIZE
FBV SSCI

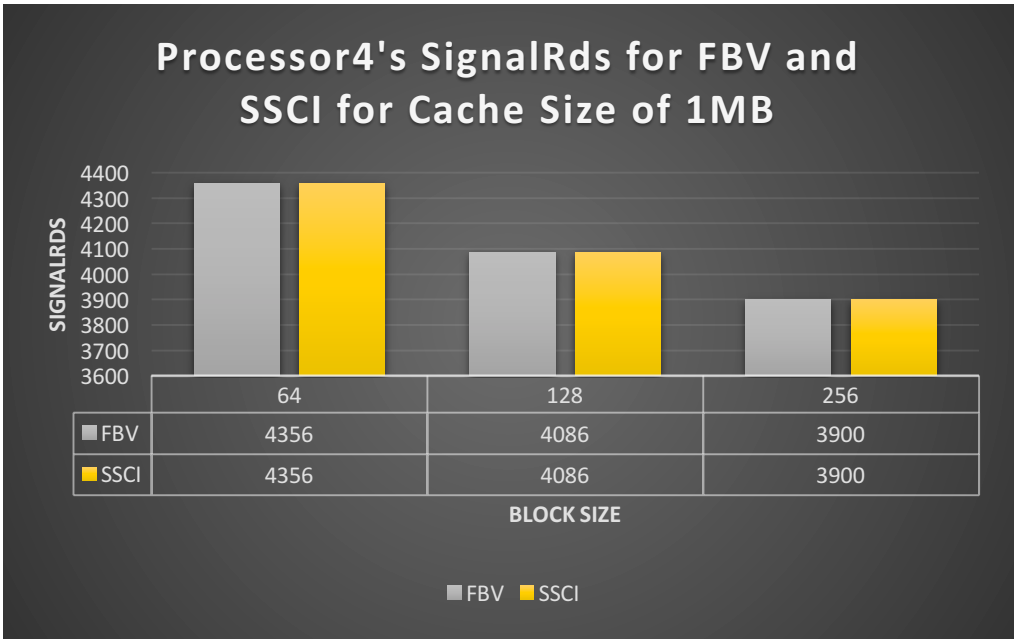
2.12 Effect of Block Size on SignalRd

We can see that signal reads are reducing with increasing of the block size. This is due to less misses due to locality property of the code provided by the trace file. This results in the reduction number of reads from the requestor processor to the home directory and thus resulting in decrease in the number of signal reads.



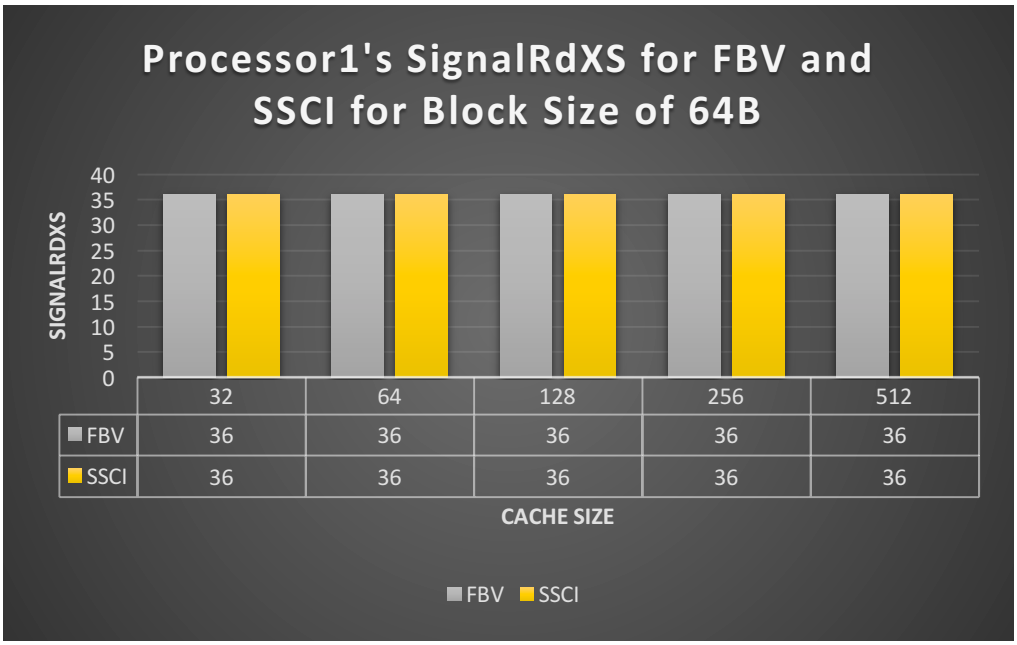


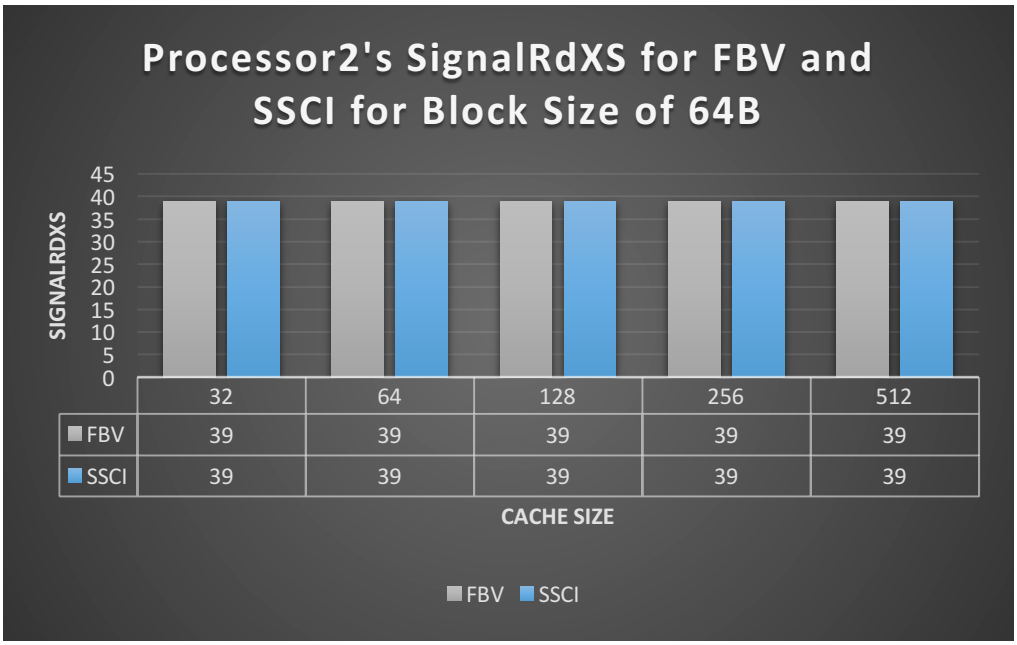

Processor3's SignalRds for FBV and SSCI for Cache Size of 1MB
SIGNALRDS
4400
4300
4200
4100
4000
3900
3800
3700
3600
64
128
256
FBV
4353
4075
3863
SSCI
4353
4075
3863
BLOCK SIZE
FBV
SSCI

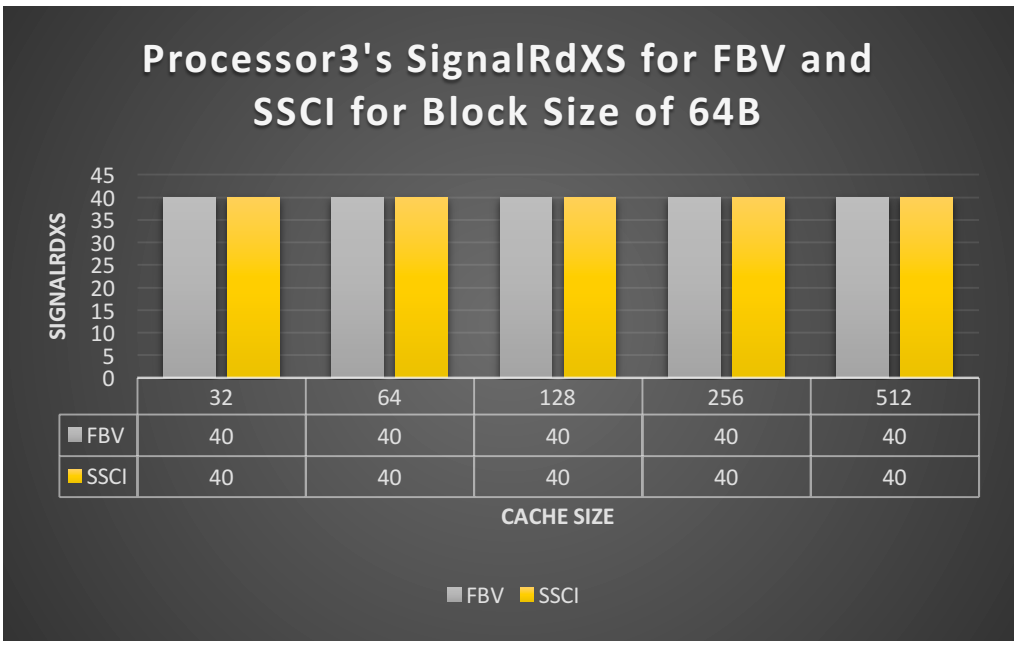

Processor4's SignalRds for FBV and SSCI for Cache Size of 1MB
SIGNALRDS
4400
4300
4200
4100
4000
3900
3800
3700
3600
64
128
256
FBV
4356
4086
3900
SSCI
4356
4086
3900
BLOCK SIZE
FBV
SSCI

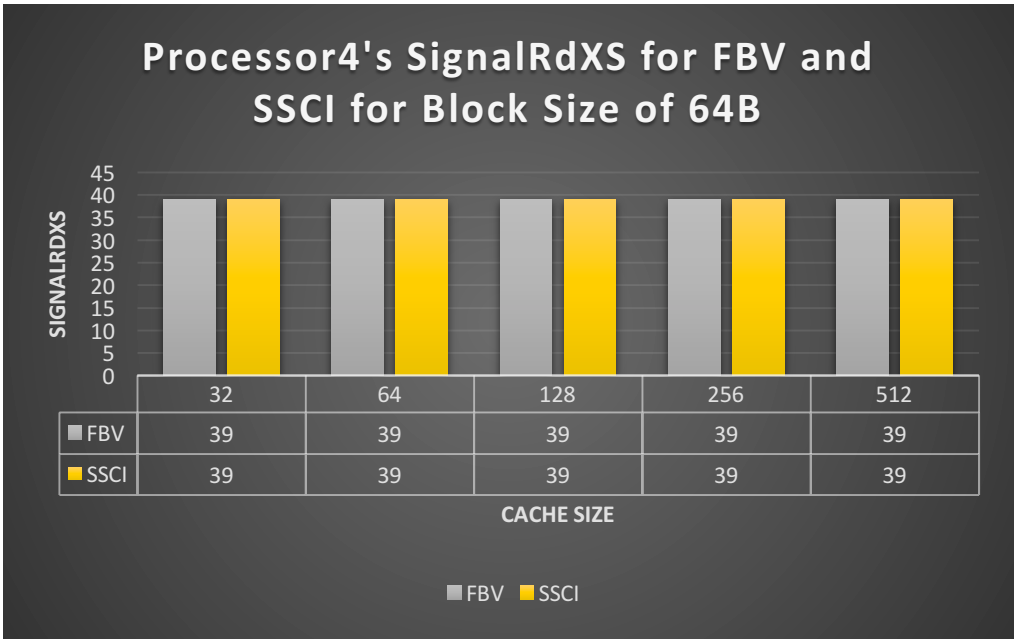
2.13 Effect of Cache Size on SignalRdX

Cache size seems to have no effect on the number of signal readX. This is because processor write will cause SignalRdX and is not affected by the other parameters but number of processor writes.



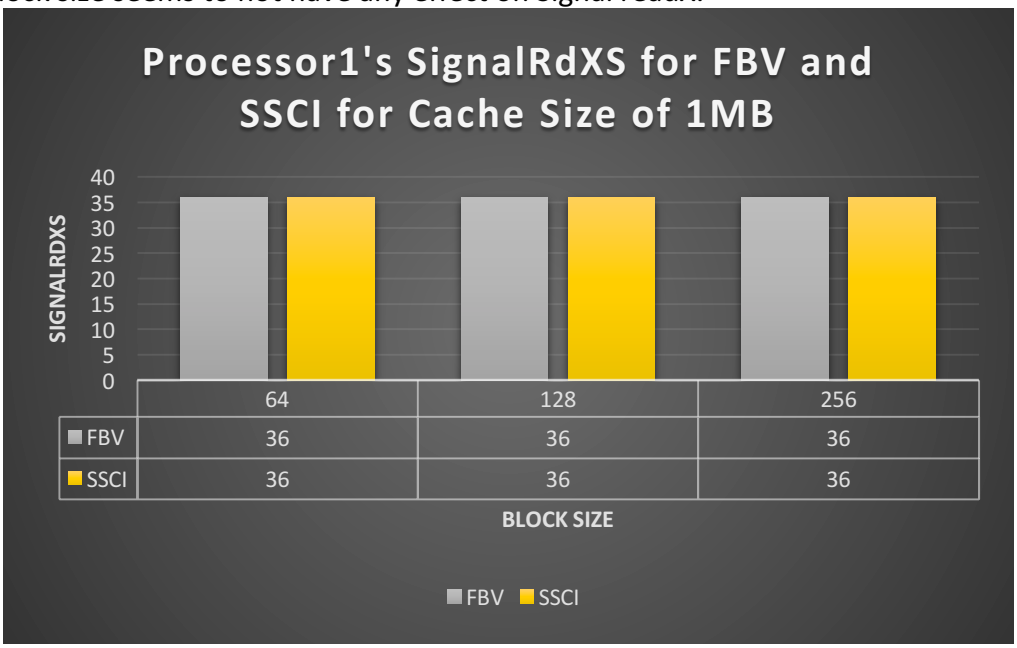


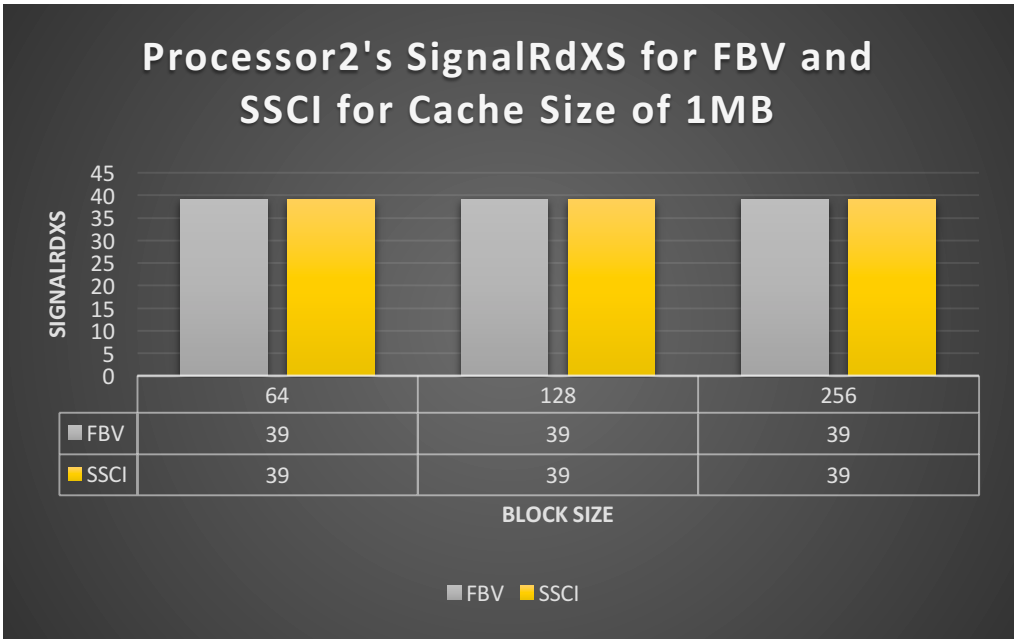

Processor3's SignalRdXS for FBV and SSCI for Block Size of 64B
SIGNALRDXS
45
40
35
30
25
20
15
10
5
0
32 64 128 256 512
FBV 40 40 40 40 40
SSCI 40 40 40 40 40
CACHE SIZE
FBV SSCI

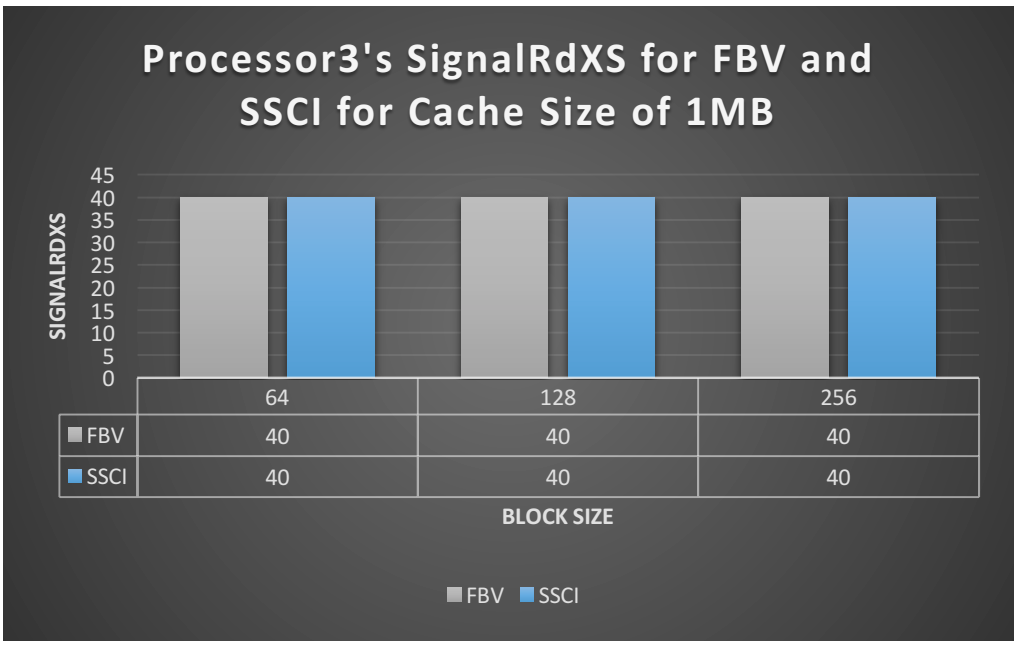

Processor4's SignalRdXS for FBV and SSCI for Block Size of 64B
SIGNALRDXS
45
40
35
30
25
20
15
10
5
0
32 64 128 256 512
FBV 39 39 39 39 39
SSCI 39 39 39 39 39
CACHE SIZE
FBV SSCI

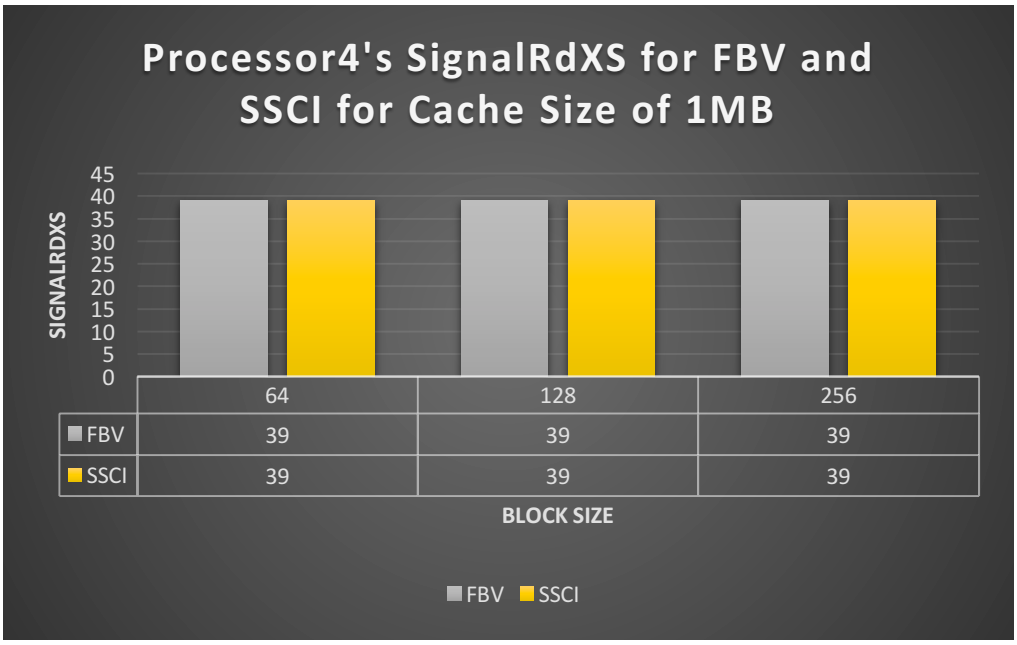
2.14 Effect of Block Size on SignalRdX

Block size seems to not have any effect on Signal readX.



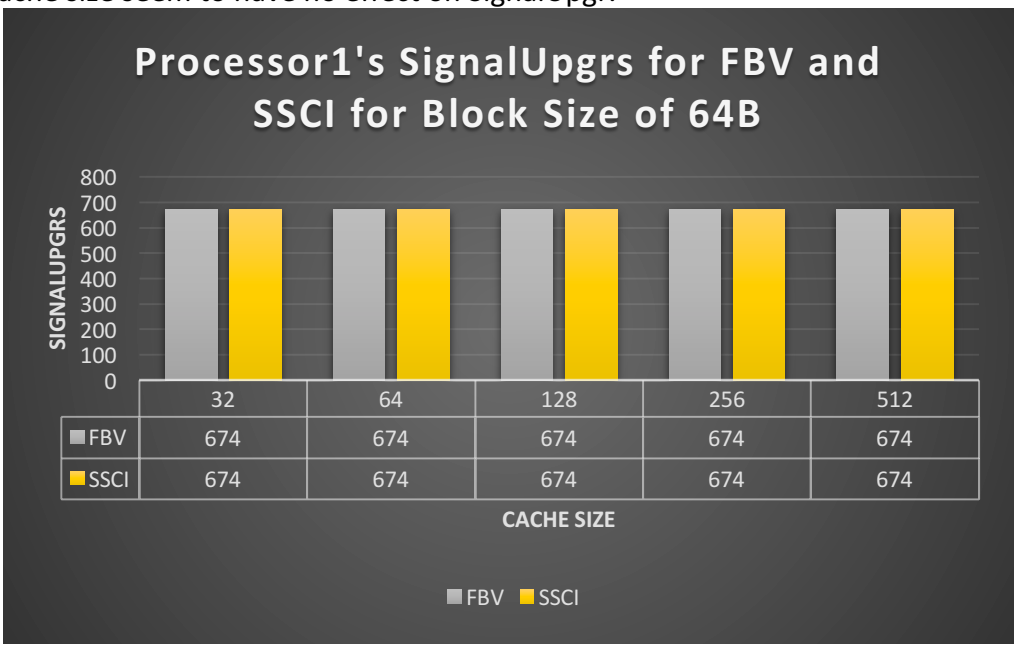


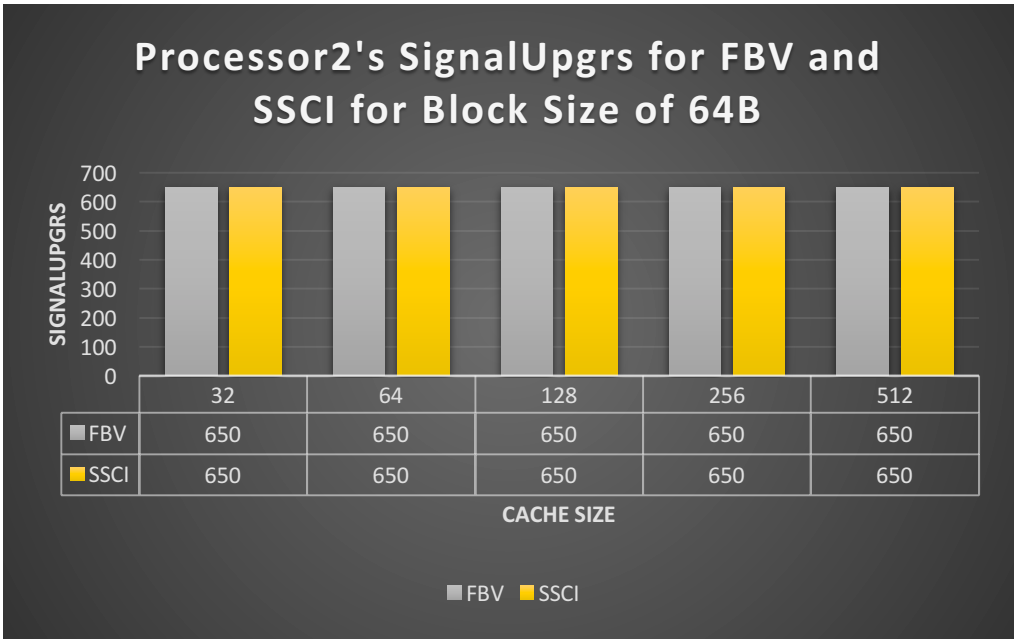

Processor3's SignalRdXS for FBV and SSCI for Cache Size of 1MB
SIGNALRDXS
45
40
35
30
25
20
15
10
5
0
64
128
256
FBV
40
40
40
SSCI
40
40
40
BLOCK SIZE
FBV
SSCI

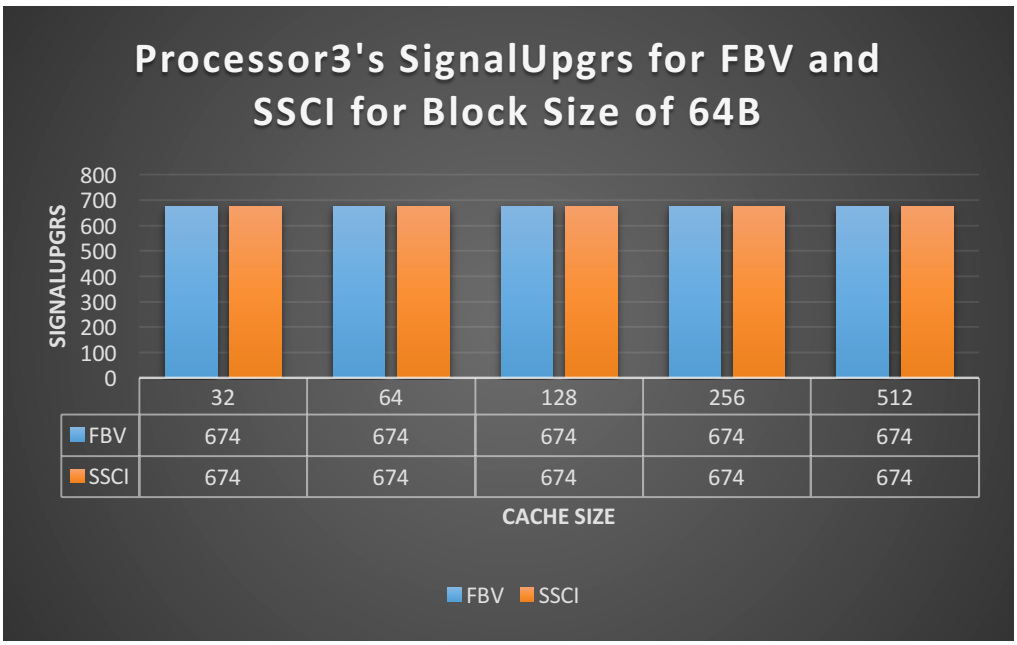

Processor4's SignalRdXS for FBV and SSCI for Cache Size of 1MB
SIGNALRDXS
45
40
35
30
25
20
15
10
5
0
64
128
256
FBV
39
39
39
SSCI
39
39
39
BLOCK SIZE
FBV
SSCI

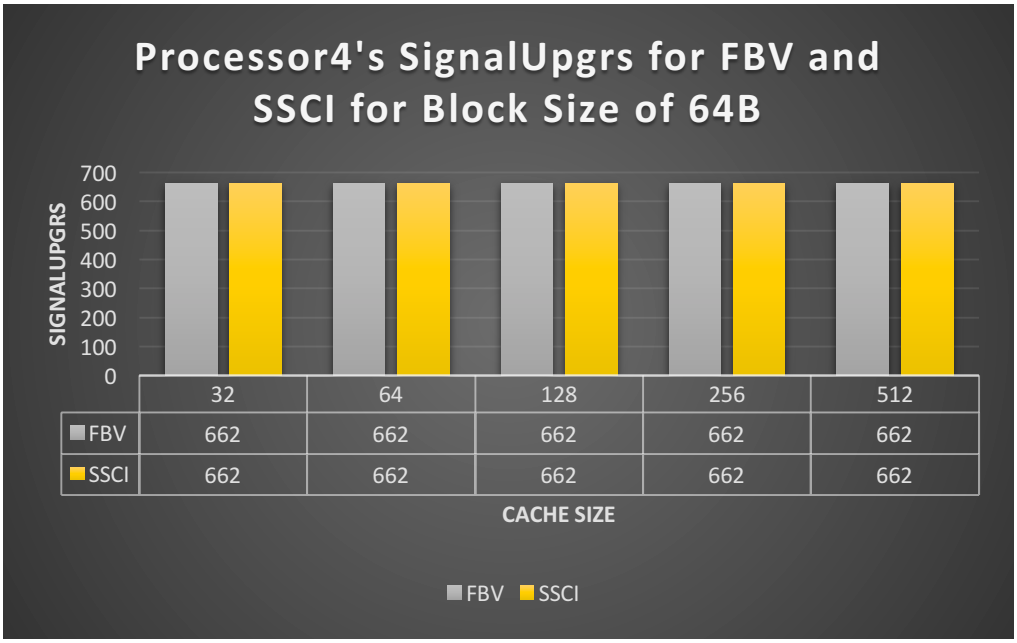
2.15 Effect of Cache size on SignalUpgr

Cache size seem to have no effect on SignalUpgr.



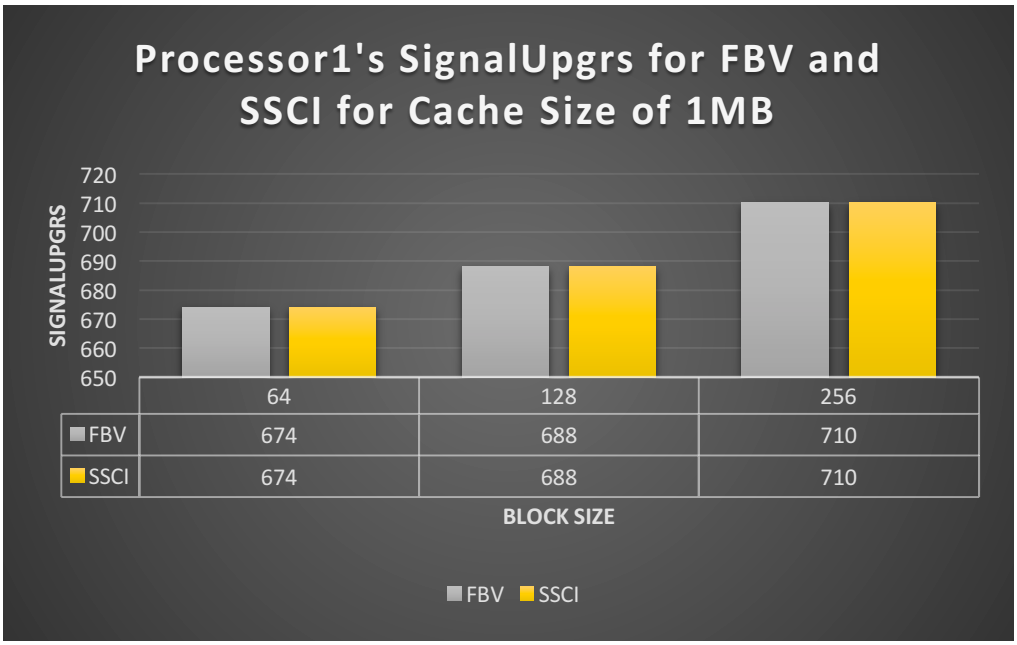


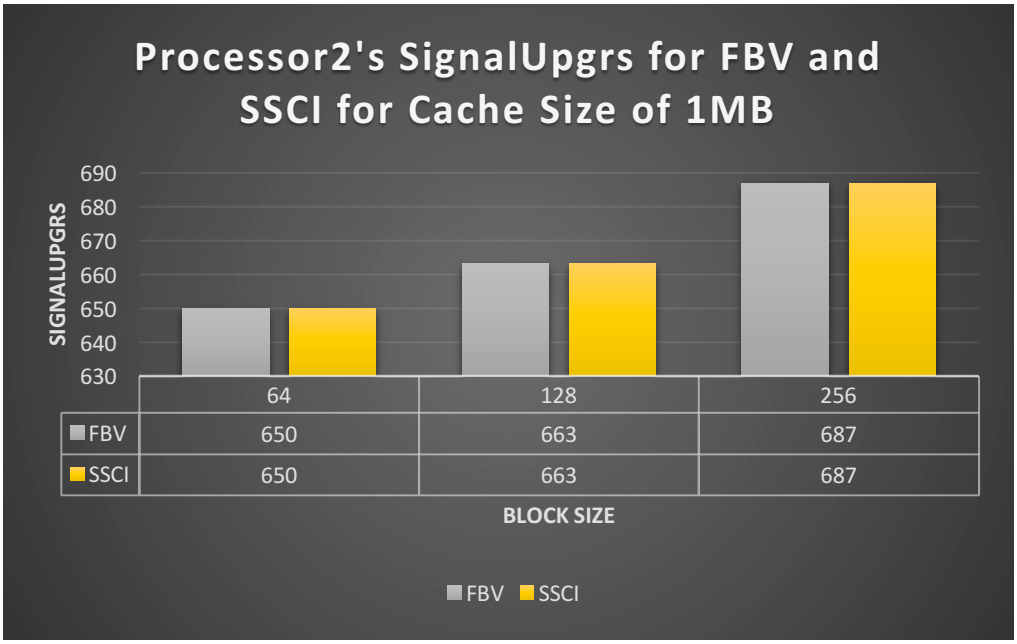

Processor3's SignalUpgrs for FBV and SSCI for Block Size of 64B
SIGNALUPGRS
800
700
600
500
400
300
200
100
0
32 64 128 256 512
FBV 674 674 674 674 674
SSCI 674 674 674 674 674
CACHE SIZE
FBV SSCI

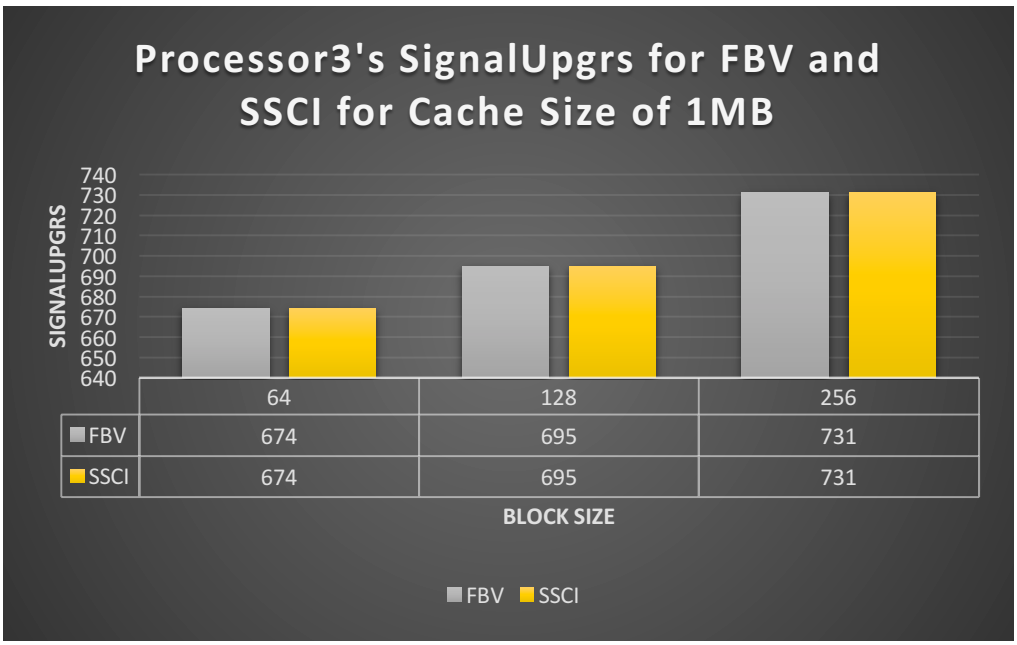

Processor4's SignalUpgrs for FBV and SSCI for Block Size of 64B
SIGNALUPGRS
700
600
500
400
300
200
100
0
32 64 128 256 512
FBV 662 662 662 662 662
SSCI 662 662 662 662 662
CACHE SIZE
FBV SSCI

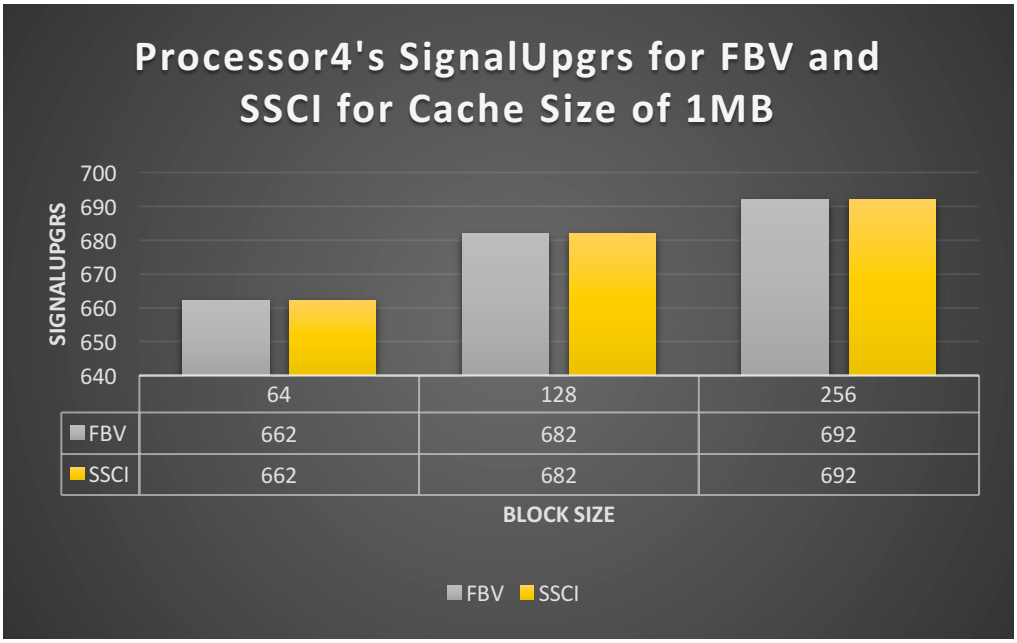
2.16 Effect of Block Size on SignalUpgr

SignalUpgr seem to increase with increase in block size. This is due to increased false sharing effect with increase in block size.



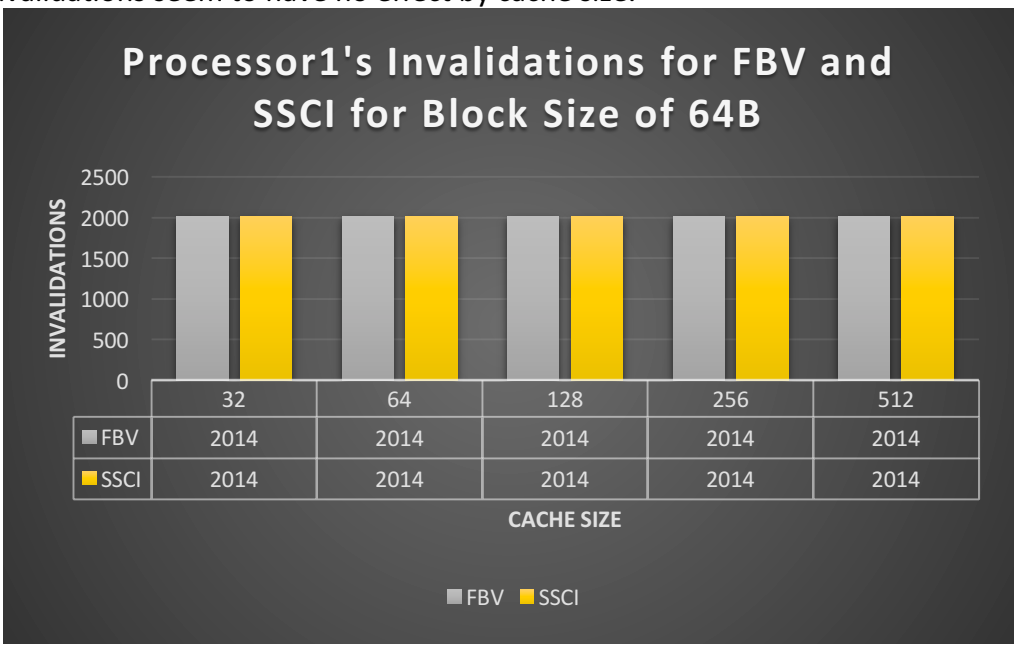


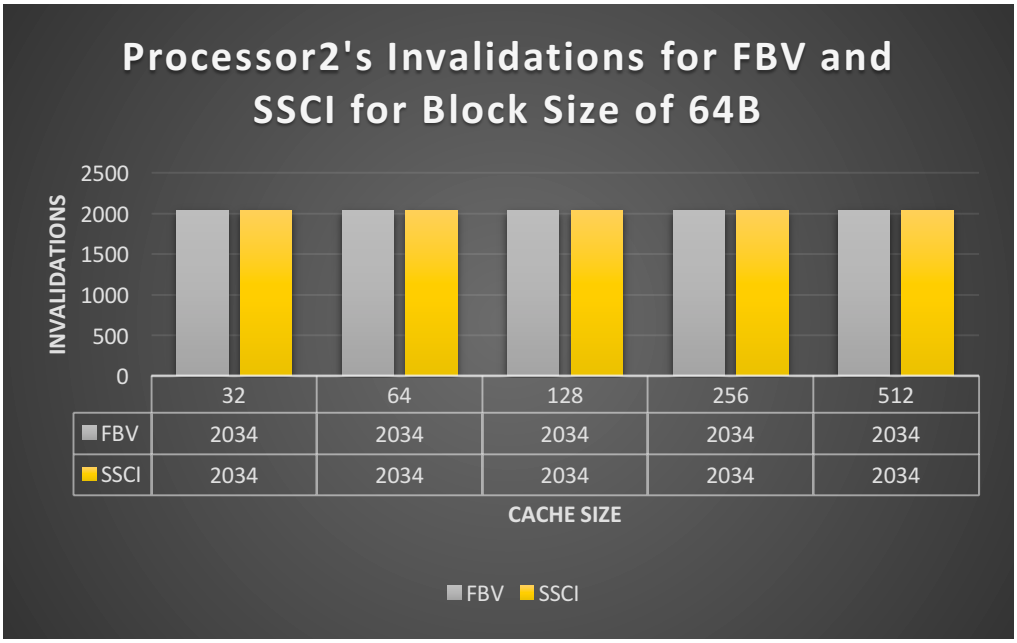

Processor3's SignalUpgrs for FBV and SSCI for Cache Size of 1MB
SIGNALUPGRS
740
730
720
710
700
690
680
670
660
650
640
64
128
256
FBV
674
695
731
SSCI
674
695
731
BLOCK SIZE
FBV
SSCI

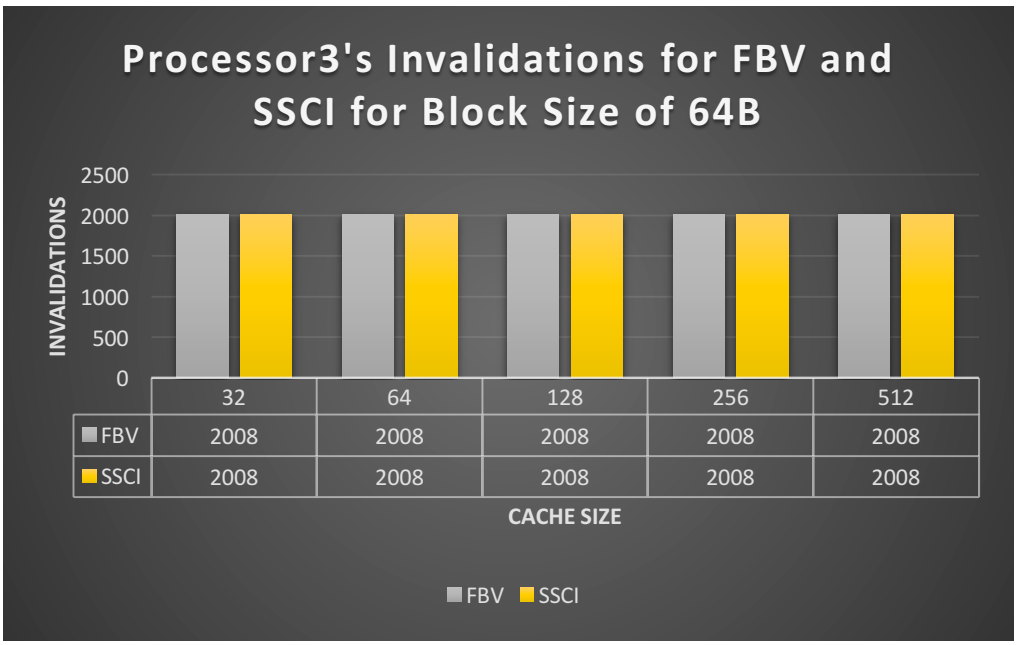

Processor4's SignalUpgrs for FBV and SSCI for Cache Size of 1MB
SIGNALUPGRS
700
690
680
670
660
650
640
64
128
256
FBV
662
682
692
SSCI
662
682
692
BLOCK SIZE
FBV
SSCI

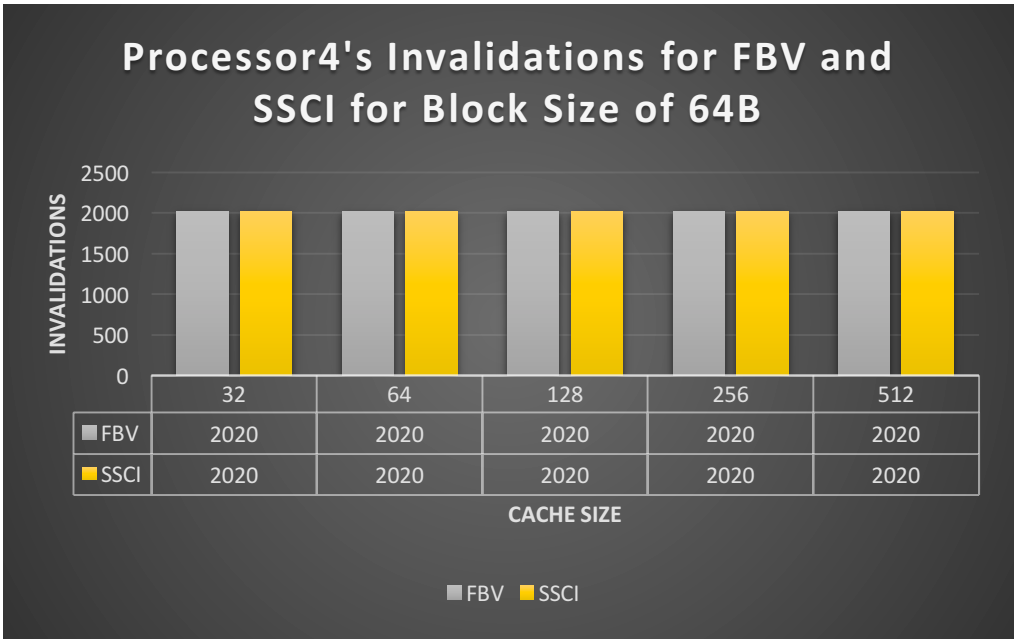
2.17 Effect of Cache size on number of Invalidations

Invalidations seem to have no effect by cache size.



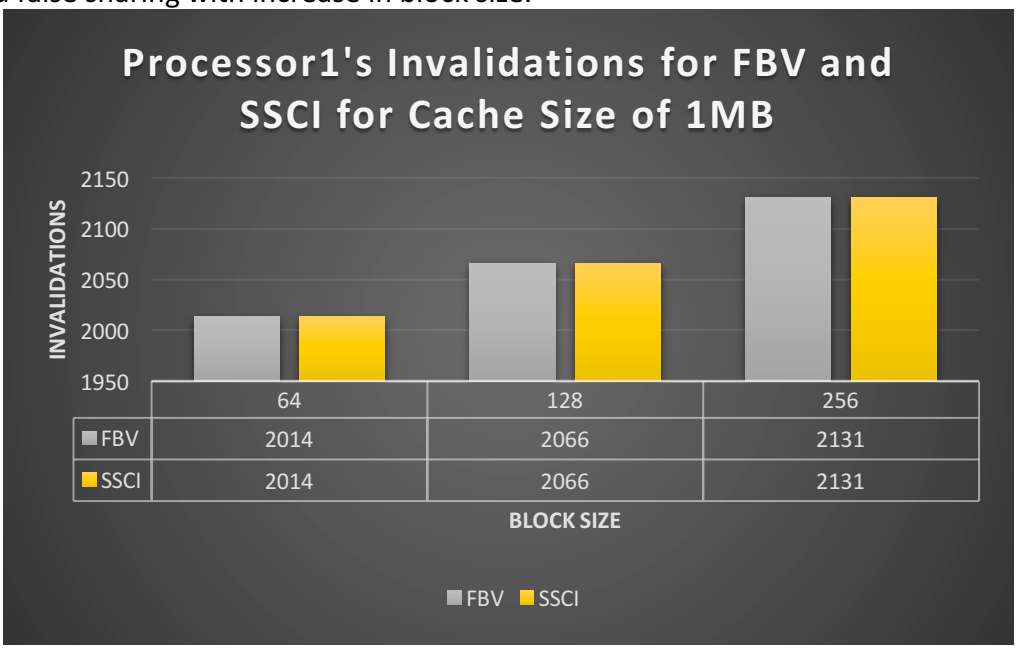


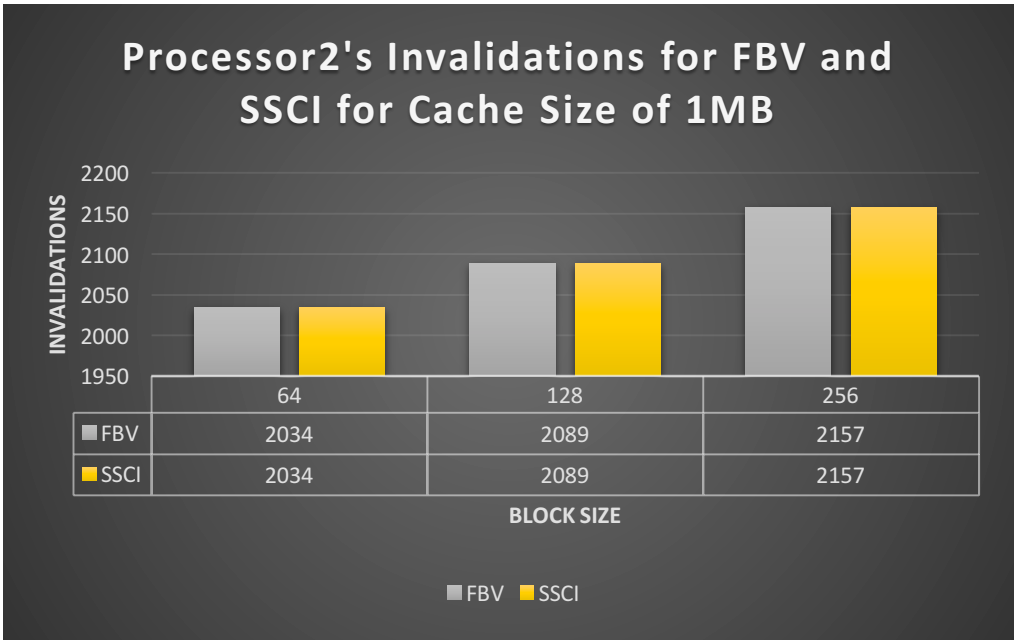

Processor3's Invalidations for FBV and SSCI for Block Size of 64B
INVALIDATIONS
2500
2000
1500
1000
500
0
32 64 128 256 512
FBV 2008 2008 2008 2008 2008
SSCI 2008 2008 2008 2008 2008
CACHE SIZE
FBV SSCI

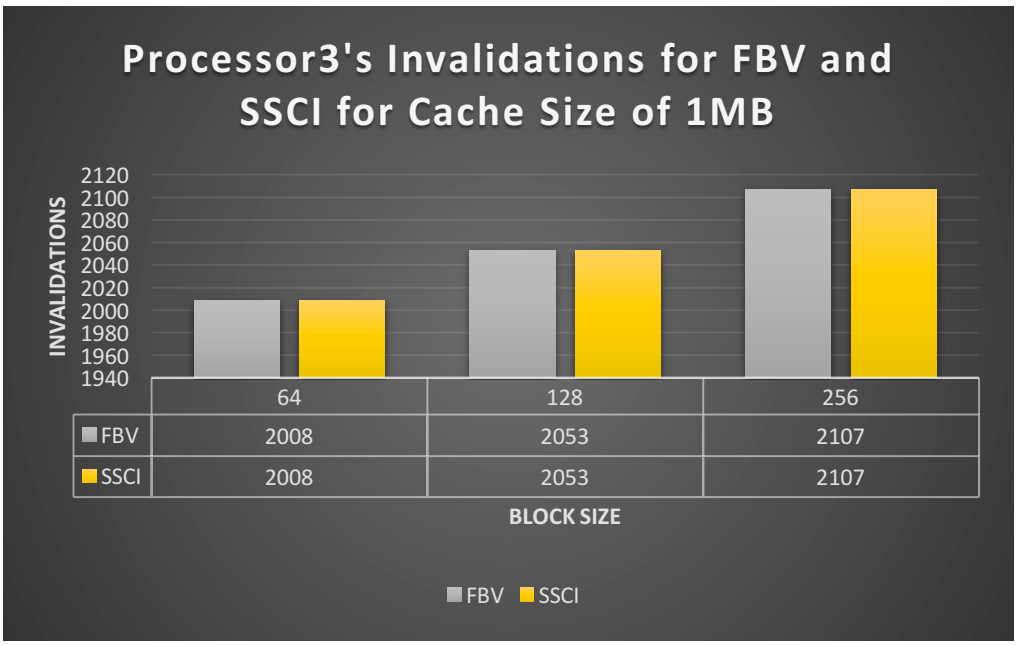

Processor4's Invalidations for FBV and SSCI for Block Size of 64B
INVALIDATIONS
2500
2000
1500
1000
500
0
32 64 128 256 512
FBV 2020 2020 2020 2020 2020
SSCI 2020 2020 2020 2020 2020
CACHE SIZE
FBV SSCI

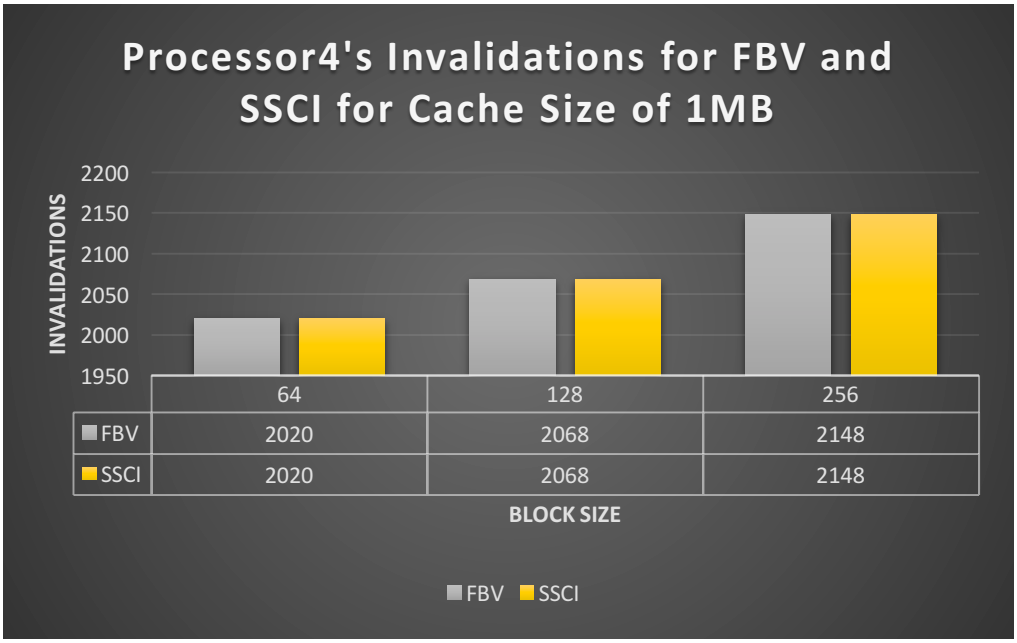
2.18 Effect of Block Size on number of Invalidations

Number of invalidation is increasing with increase in block size. This is because of increased false sharing with increase in block size.



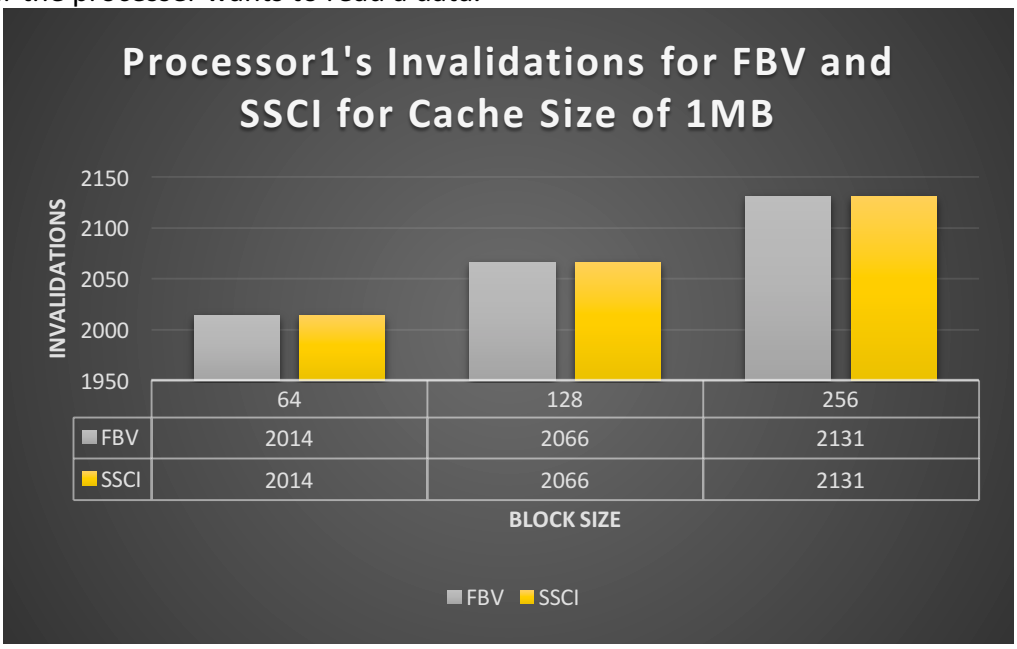


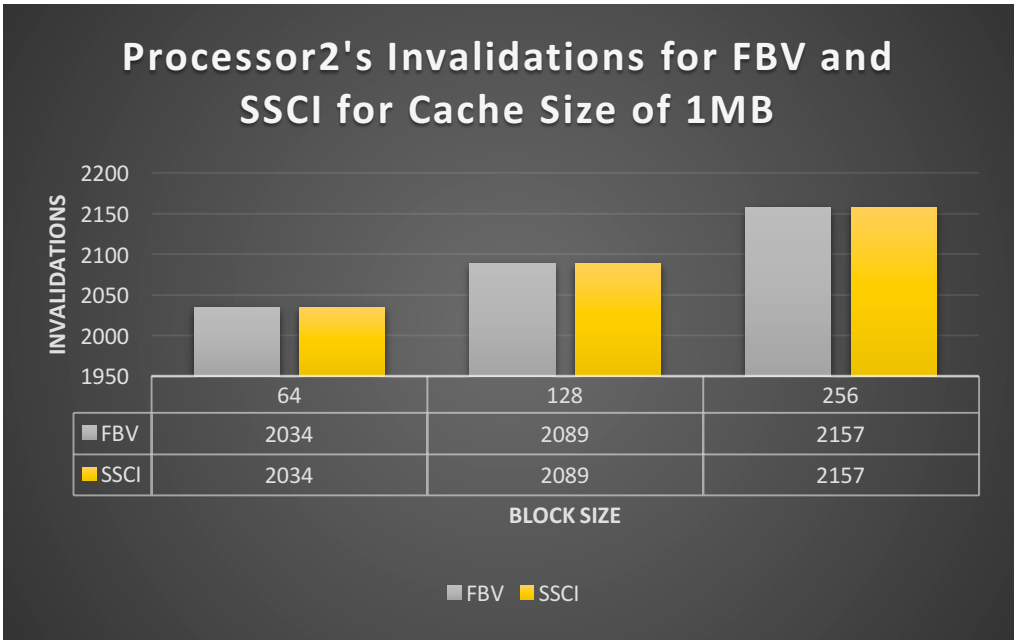

Processor3's Invalidations for FBV and SSCI for Cache Size of 1MB
INVALIDATIONS
2120
2100
2080
2060
2040
2020
2000
1980
1960
1940
64
128
256
FBV
2008
2053
2107
SSCI
2008
2053
2107
BLOCK SIZE
FBV
SSCI

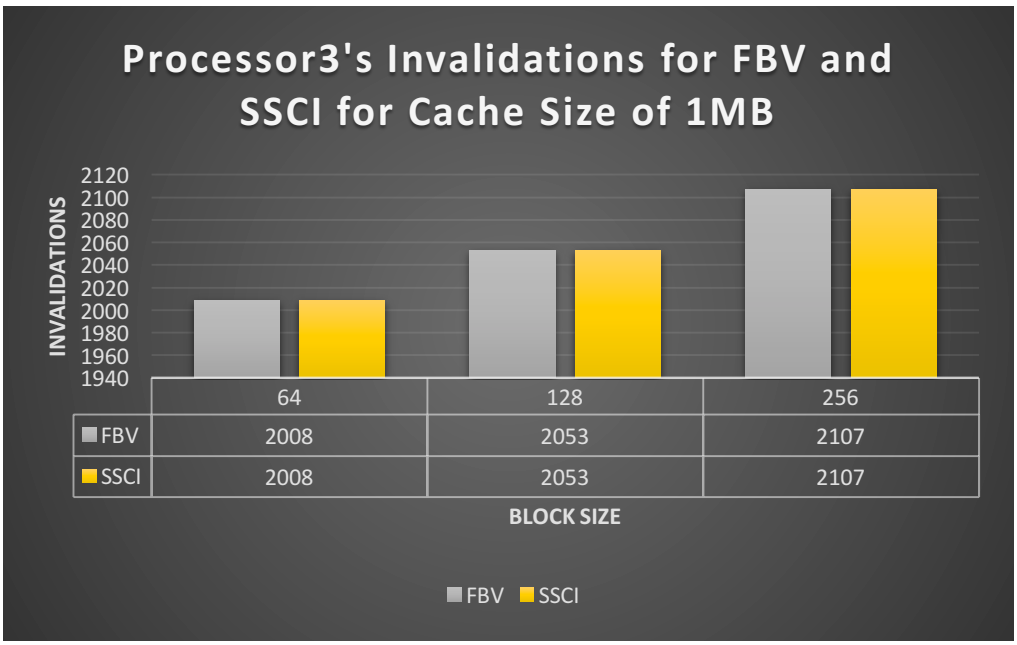

Processor4's Invalidations for FBV and SSCI for Cache Size of 1MB
INVALIDATIONS
2200
2150
2100
2050
2000
1950
64
128
256
FBV
2020
2068
2148
SSCI
2020
2068
2148
BLOCK SIZE
FBV
SSCI

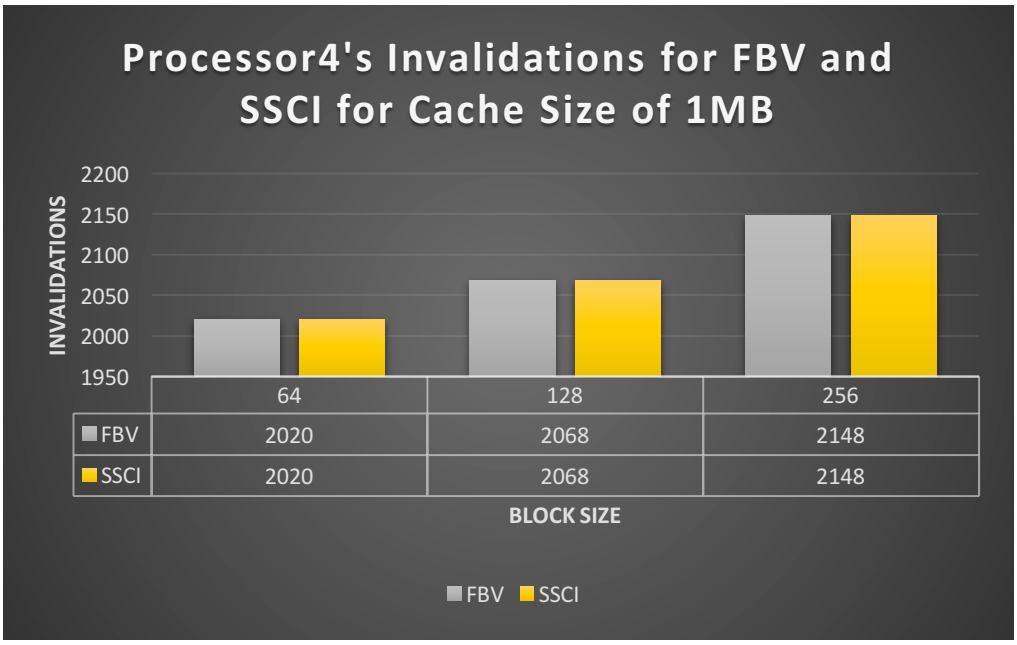
2.19 Effect of Cache size on number of Interventions

Numbers of interventions are increasing with increase in cache size. This is because with increased there will be less misses and thus more shares. This results in increased interventions whenever the processer wants to read a data.



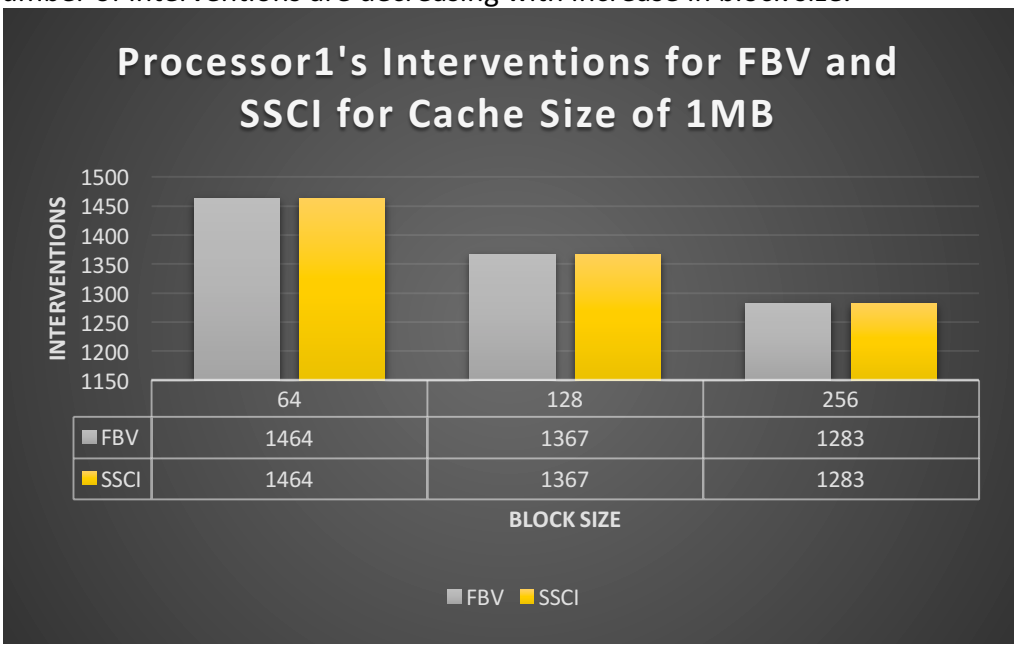


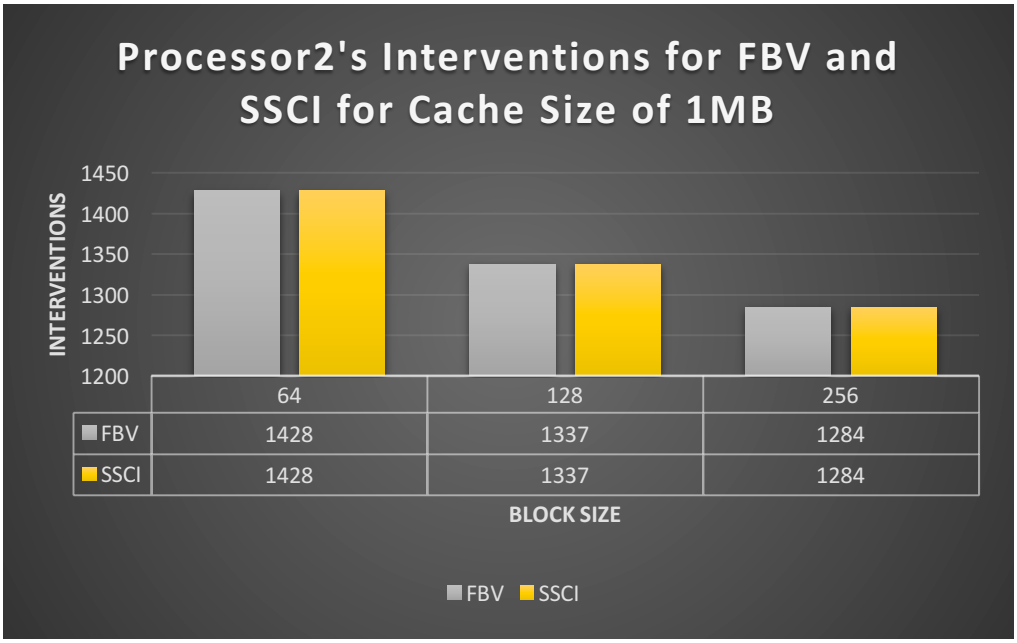

Processor3's Invalidations for FBV and SSCI for Cache Size of 1MB
INVALIDATIONS
2120
2100
2080
2060
2040
2020
2000
1980
1960
1940
64
128
256
FBV
2008
2053
2107
SSCI
2008
2053
2107
BLOCK SIZE
FBV
SSCI

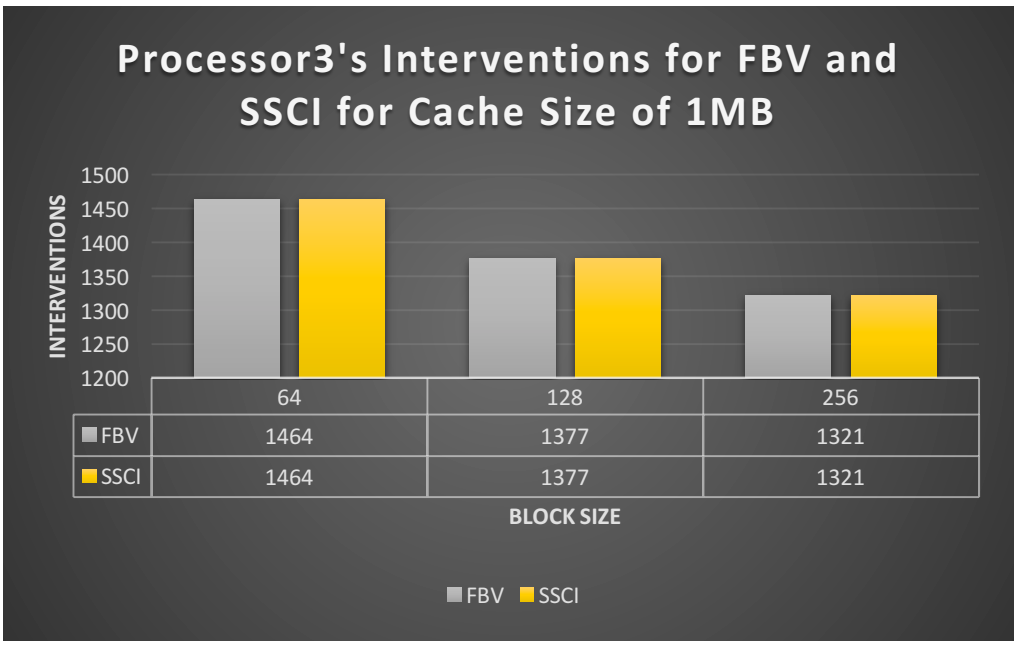

Processor4's Invalidations for FBV and SSCI for Cache Size of 1MB
INVALIDATIONS
2200
2150
2100
2050
2000
1950
64
128
256
FBV
2020
2068
2148
SSCI
2020
2068
2148
BLOCK SIZE
FBV
SSCI

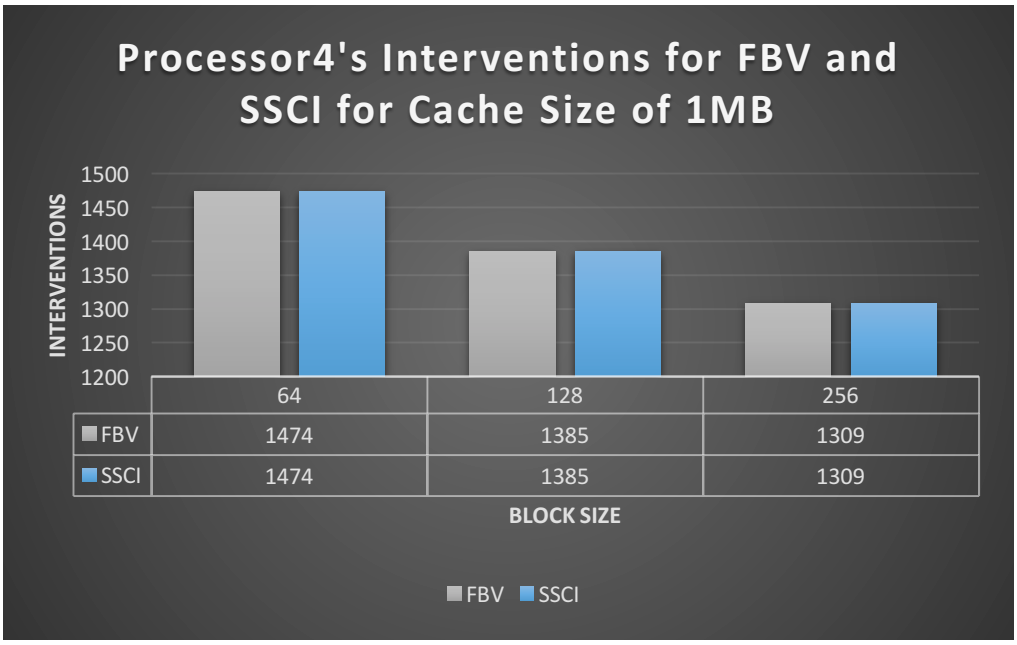
2.20 Effect of Block Size on number of Interventions

Number of interventions are decreasing with increase in block size.






Processor3's Interventions for FBV and SSCI for Cache Size of 1MB
INTERVENTIONS
1500
1450
1400
1350
1300
1250
1200
64
128
256
FBV
1464
1377
1321
SSCI
1464
1377
1321
BLOCK SIZE
FBV
SSCI


Processor4's Interventions for FBV and SSCI for Cache Size of 1MB
INTERVENTIONS
1500
1450
1400
1350
1300
1250
1200
64
128
256
FBV
1474
1385
1309
SSCI
1474
1385
1309
BLOCK SIZE
FBV
SSCI