**CSE460 Lab3 assessment**

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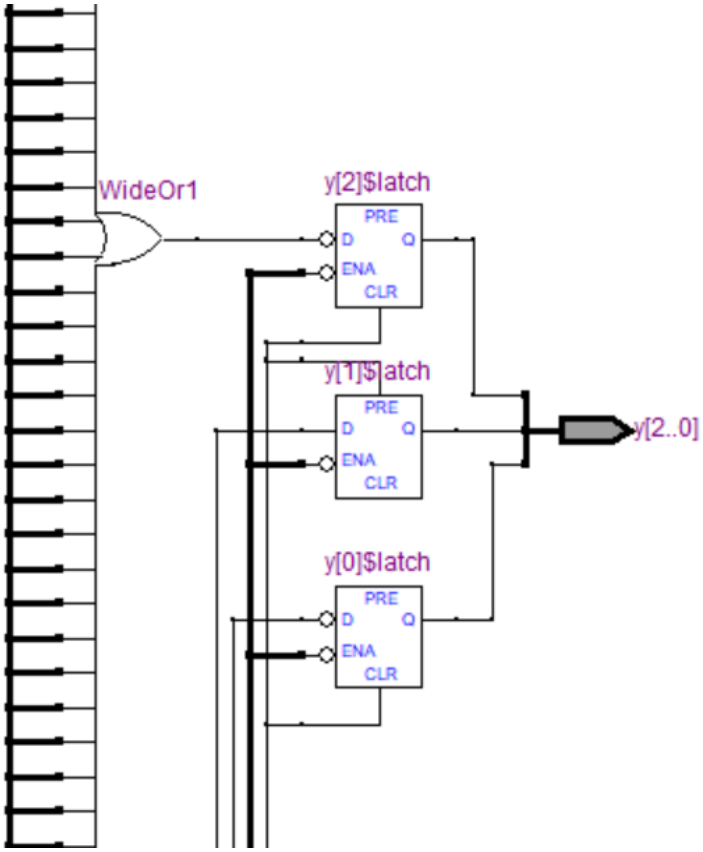
Section: 05

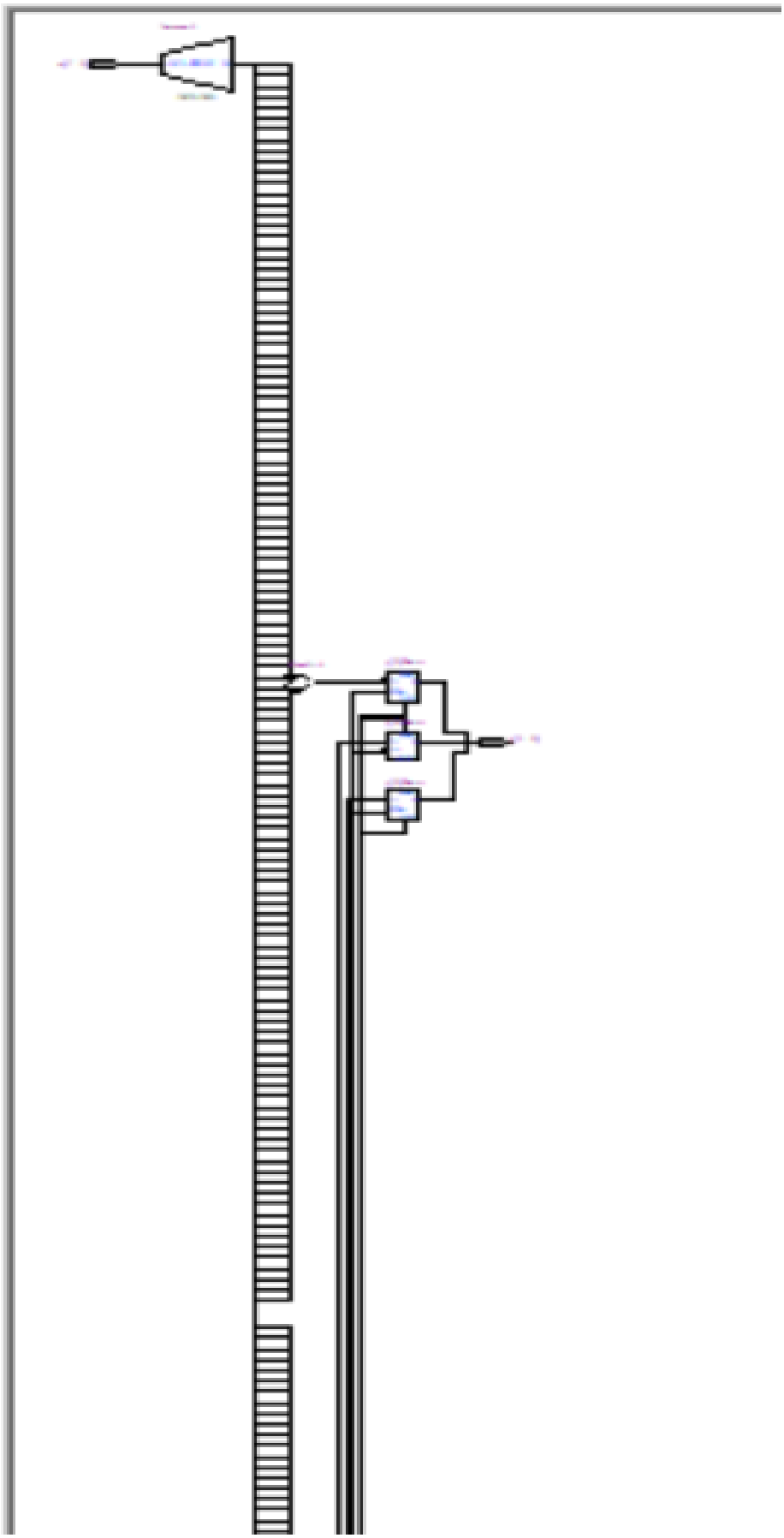
**Task1:**

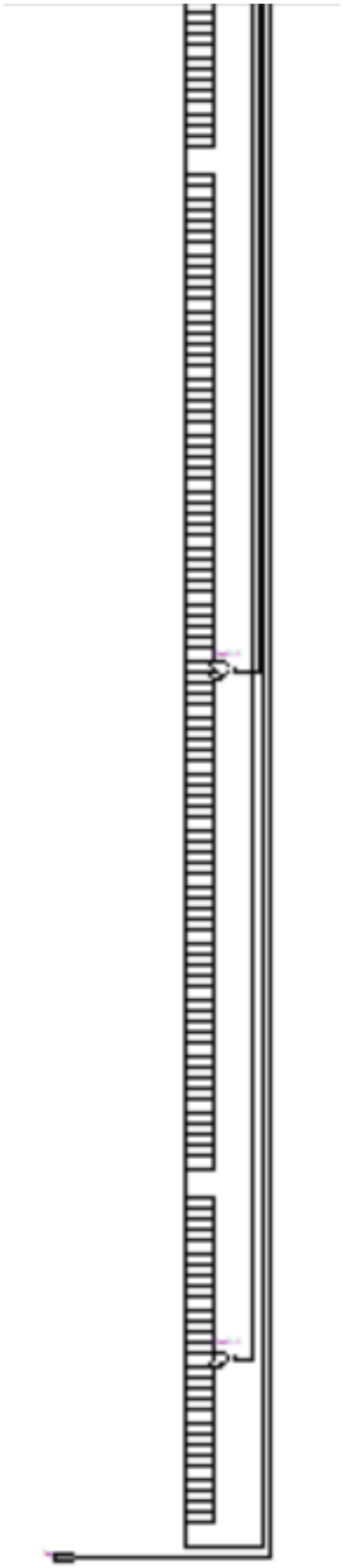
Code:

```
module lab3assessment(y,w,flag);
input [7:0]w;
input flag;
output reg [2:0]y;

always@(flag, w)
	if (flag == 1)
		y = 2;   // Last digit of ID
	else
		begin
			casex(w)
				8'bxx1xxxxx: y = 5;
				8'bxx0xxxx1: y = 0;
				8'bxx0xxx10: y = 1;
				8'bxx0xx100: y = 2;
				8'bx10xx000: y = 6;
				8'bx00x1000: y = 3;
				8'b100x0000: y = 7;
				8'b00010000: y = 4;
			endcase
		end

endmodule
```

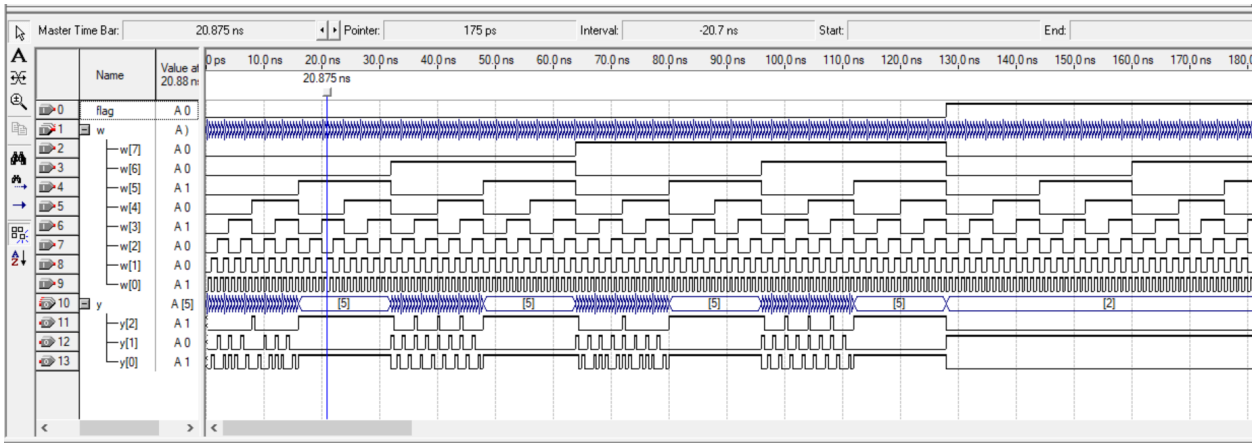
Circuit:


WideOr1
y[2]$latch
PRE
D
Q
ENA
CLR
y[1]$latch
PRE
D
Q
ENA
CLR
y[0]$latch
PRE
D
Q
ENA
CLR
y[2..0]





Timing Diagram:

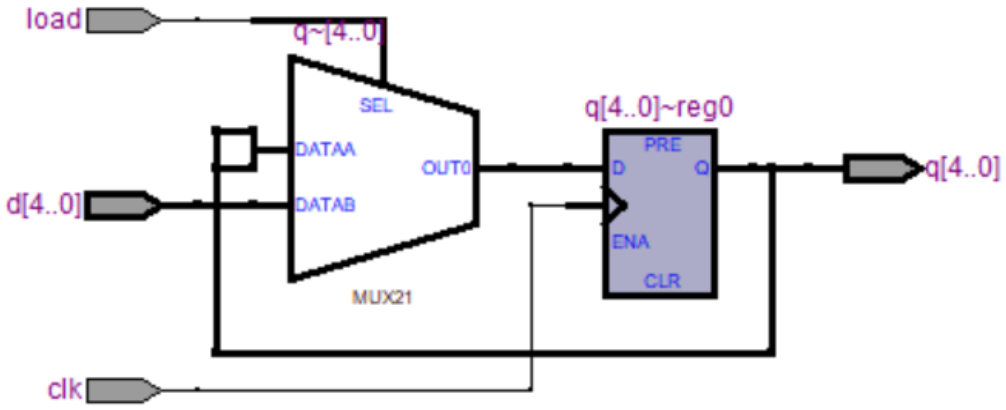



Task2:

Code:

```
module lab3assessment(q, d, load, clk);
input [4:0]d;
input load, clk;
output reg [4:0]q;

always@(posedge clk)
        if(load)
                q <= d;
        else
                begin
                        q[4]<=q[3];
                        q[3]<=q[2];
                        q[2]<=q[1];
                        q[1]<=q[0];
                        q[0]<=q[4];
                end

endmodule
```

Circuit:




Timing diagram: