Working with Altera Quartus:

Creating a new Project

1. From Desktop / search for quartus-> Open Quartus.(**8.1**) **[DO NOT OPEN Quartus 11]**
2. Click File->New Project Wizard->Next
3. Fill out the following:
    - Working directory? – Browse->Create a folder in a directory **other than C drive (Downloads, Desktop are parts of C drive, DO NOT OPEN A PROJECT THERE!).**
    - *The name of the folder should **not** start with a number or any special character!->* Select the folder
    - What is the name of the project->Type a name and remember it (Say "expt1"). Same name is going to be copied to the next box automatically.[**DO NOT start the name with any special character or number**]
    - Press next.
4. Press next **again**
5. Select Device Family: **FLEX10KE** and press next.
6. Fill out the following in **all three pair of boxes:**

Tool name: 1. Custom / **2.** Custom / **3.** Custom
Format: 1. Verilog HDL/ **2.** Verilog/ **3.** Verilog
Press Next->Finish

Creating a New Verilog file:

7. From the Quartus application->File->New->Verilog HDL File->OK
8. Write the code and save it with the same name as that given in expt1 with extension of .v (Example: expt1.v)
9. The **project name** [expt1] and the **module name** [expt1] should be the same.

Viewing RTL Circuit

10. Compile the code. RTL circuit: **Tools-> Netlist viewer->RTL viewer.**

Output: Creating a new vector Waveform File & Simulation

11. File->New->Vector Waveform File
12. Save as-> Save with the same filename as the .vwf file (Example: expt1.vwf)
13. Right click on Name->Insert->Insert Node or BUS
14. Click Node Finder
    Filter: Pins: all
    Look in: Filename (Example expt2.v)

Click list->Click ">>" -> OK -> OK

13. Right click on each **input**->Value->Clock and set up the clocks.
14. From the menu -> Assignment->Settings->Simulator Settings
    - Simulation Mode: **Functional**
    - Click OK.
15. From the menu -> Processing-> Generate Functional Simulation Netlist
16. Processing-> Start Simulation