CSE460 Handout (Fall 2023)

Exam schedule (tentative)

Exam	Time	Date	Syllabus*
Quiz 1	2nd Week	[TBA]	Lecture 1-3
Quiz 2	4th Week		Lecture 5-6
Quiz 3	6th Week		Lecture 8-10
Midterm	***7th Week***	***November 04, 2023***	***Lecture 1-10***
Quiz 4	9th or 10th Week	[TBA]	Lecture 13-16
Quiz 5	12th or 13th Week		Lecture 17- 20
Final	***14th Week***	***December 26, 2023***	***Lecture 11-20***

*Follow course timeline

Marks distribution

Theory/Lab	Assessment	Percentage	Total number of assessments	Number of assessment to be graded
Theory (75%)	Attendance	**10%**	-	85% and up for full marks
	Assignment	**5%**	2+	All
	Quiz*	**15%**	5 (n)	Best 4 (n-1)
	Midterm	**20%**	1	1
	Final	**25%**	1	1
Lab (25%)	Lab-attendance	**5%**	-	100% for full marks
	Lab-report	**5%**	6-7 (n)	Best 5-6 (n-1)
	Lab-test	**5%**	1	1
	Paper presentation	**10%**	1	1

*The last quiz (n^{th} quiz) will be considered as make-up for any missed quiz (maximum of 1), whatever the reason. **No other make-up quizzes will be taken.**

Class schedule

Course	Sec	Theory Day	Theory Time	Theory Room	Theory Teacher	Lab Day	Lab Time	Lab Room	Lab Teacher
CSE460	1	SUN, TUE	02:00 PM-03:20 PM	UB81403	MAQ	SAT	08:00 AM-10:50 AM	UB41203	HAD, FHF
CSE460	2	SUN, TUE	03:30 PM-04:50 PM	UB70403	BRH	SAT	11:00 AM-01:50 PM	UB41203	AGS, ABY
CSE460	3	MON, WED	02:00 PM-03:20 PM	UB70302	FHF	THU	08:00 AM-10:50 AM	UB41203	ABY, MAQ
CSE460	5	SAT, THU	11:00 AM-12:20 PM	UB70702	AJB	TUE	11:00 AM-01:50 PM	UB80404	MOM, PMD
CSE460	6	SAT, THU	12:30 PM-01:50 PM	UB70301	TAF	MON	08:00 AM-10:50 AM	UB41203	HRY, FHF
CSE460	7	SAT, THU	02:00 PM-03:20 PM	UB70402	FHF	TUE	11:00 AM-01:50 PM	UB41203	BRH, MAQ
CSE460	8	SAT, THU	03:30 PM-04:50 PM	UB70702	ABY	WED	02:00 PM-04:50 PM	UB41203	MOM, HRY

Lab Status

Section	Faculty	Day	Schedule	Room	Lab Executed
01	HAD, FHF	SAT	08:00 AM-10:50 AM	UB41203	NONE
02	AGS, ABY	SAT	11:00 AM-01:50 PM	UB41203	NONE
03	ABY, MAQ	THU	08:00 AM-10:50 AM	UB41203	NONE
05	MOM, PMD	TUE	11:00 AM-01:50 PM	UB80404	NONE
06	HRY, FHF	MON	08:00 AM-10:50 AM	UB41203	NONE
07	BRH, MAQ	TUE	11:00 AM-01:50 PM	UB41203	NONE
08	MOM, HRY	WED	02:00 PM-04:50 PM	UB41203	NONE

Lab software

- **dsch2**
  Download link:
  https://drive.google.com/drive/folders/1xwzh8gbnfAvQBYRBd9xDs20lFbyK6SlJ?usp=sharing (For experiments: 1)
- **Quartus**
  Download link:
  https://drive.google.com/drive/folders/1VVXijpn4d9LY4PS-Q_dAKXCU8q9xoESm?usp=sharing (For experiments: 2, 3,4,5)
- **Microwind**
  Download link:
  https://drive.google.com/drive/folders/11xGLeyzWkfMV4nPgUqLjLi4eXAZVs7WM?usp=sharing (For experiments: 6)
- Jupyter Notebook / Google Colab (For experiments: 7)

Course team

Theory

Initial	Name	BRACU Email
AJB	Abdullah Jubair Bin Iqbal	jubair.iqbal@bracu.ac.bd
ABY	Md Asif Hossain Bhuiyan	asif.hossain@bracu.ac.bd
BRH	Beig Rajibul Hasan	rajib.hasan@bracu.ac.bd
TAF	Tasnim Ferdous	tasnim.ferdous@bracu.ac.bd
FHF	Fahim Faisal	
MAQ	Mohammed Aminul Haque	

Lab

Initial	Name	BRACU Email
AJB	Abdullah Jubair Bin Iqbal	jubair.iqbal@bracu.ac.bd
AGS	Aroni Ghosh	aroni.ghosh@bracu.ac.bd
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HRY	Himaddri Roy	himaddri.roy@bracu.ac.bd
HAD	Shadman Shahid	
MAQ	Mohammed Aminul Haque	
PMD	Prithu Mahmud	
FHF	Fahim Faisal	

Communication platform

CSE460 Fall ’23 Official Discord Server: https://discord.gg/kVkgeqy2

Textbooks

- **[Weste&Harris]** CMOS VLSI Design A Circuit and Systems Perspective 4e - Weste, Harris: http://library.lol/main/51BD9C7E9E62DF12B1122C9B874DBFAC
  [*Solution manual is also available online*]
- **[Brown&Vranesic]** Fundamentals of Digital Logic with Verilog Design 3e - Stephen Brown, Zvonko Vranesic:
  http://library.lol/main/7084609A715D3C56A468C66D66DD1019
  [*Solution manual is also available online*]
- **[Andrew,Jens,Igor&Jin]** VLSI Physical Design: From Graph Partitioning to Timing Closure 1e - Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu:
  https://theswissbay.ch/pdf/Gentoomen%20Library/Misc/Springer%20-%20VLSI%20Physical%20Design.pdf
- [Naveed A. Sherwani] Algorithms for VLSI Physical Design automation (third edition)
  https://drive.google.com/file/d/1zN8dcQeKMQdQj-ejm17JCRlWwx58VpfZ/view?usp=share_link
- ***Chapter wise topic lists from the Books-***
  https://drive.google.com/file/d/1nVr_EWHiICuEubedRChEcz0Y9VqXNJEx/view?usp=share_link

Practice problems sheet

After watching/attending the lectures and reading the corresponding texts, try to solve the following problems:

Week-wise Practice Problems:CSE460: VLSI Design Practice Problems for Exam (Fall 2023)
Solution Manual for Practice Problems: [Answer_Sheet]

**[*The problems are compiled from the corresponding reading sections’ solved example problems or exercises.*]
****The final questions in the exam will be conceptual & analytical (theoretical and problem-solving).**

Course timeline

Week	Event	Details/Syllabus	Reference	Slide
1 [Sep 23 - Sep 28] Sep 28 (Thu)	Theory: Week 1 Lecture 1	Introduction to VLSI	[Weste&Harris] Chapter 1 1.1 A Brief History	CSE460 Lec…
	Theory: Week 1 Lecture 2	- Review of digital electronics - Logic gates in CMOS	[Brown&Vranesic] Chapters 2, 4, 5 2.4 Logic Gates and Networks [Full, up to Functionally Equivalent Networks] 2.3 Boolean Algebra: Axioms of Boolean Algebra, Examples: 2.3, 2.4 4.1 Multiplexers [up to example 4.1(included)] 5.3 Gated D Latch [Full, 5.3.1 will be covered in future] 5.4.1 Master-Slave D Flip-flop [Full]	CSE460 Lec…
2 [Sep 30 - Oct 5]	**Lab:** Experiment 1	CMOS Schematic Circuit Design in DSCH2	CSE 460 Ex…	
	Theory: Week 2 Lecture 1	Implementation of logic blocks and sequential elements in CMOS technology	[Weste&Harris] Chapter 1 1.3 MOS Transistors (full) 1.4 CMOS Logic (1.4.1-1.4.5)	CSE460 Lec…
	Theory: Week 2 Lecture 2	CMOS Implementation	[Weste&Harris] Chapter 1 1.4 CMOS Logic (1.4.6-1.4.9)	CSE460 Lec…
3 [Oct 7 - Oct 12]	**Lab**: Experiment 2	Introduction to Verilog; Verilog Design Part 1 (combinational logic)	Altera Quart… CSE 460 Ex…	CSE460 Lab…
	Theory: Week 3 Lecture 1	CMOS transistor theory	[Weste&Harris] Chapter 2 2.1 Introduction 2.2 Long-channel I-V Characteristics	CSE460 Lec…

	Theory: Week 3 Lecture 2	CMOS transistor theory	[Weste&Harris] Chapter 2 2.2 Long-channel I-V characteristics Example 2.1 2.3.1 Simple MOS capacitance models + mathematical problem solving	CSE460 Lec… CSE460 Lec…
4 [Oct 14 - Oct 19]	**Lab**: Experiment 3	Verilog Design Part 2 (sequential logic)	CSE 460 Ex…	CSE460 Lab…
	Theory: Week 4 Lecture 1	DC response of CMOS inverter	[Weste&Harris] Chapter 2 2.5 DC Transfer Characteristics 2.5.1 Static CMOS Inverter DC Characteristics 2.5.2 Beta Ratio Effects 2.5.4 Pass Transistor DC Characteristic	CSE460 Lec…
	Theory: Week 4 Lecture 2	Introduction to system design using finite state machines	[Brown&Vranesic] Chapter 6 6.1 Basic Design Steps [Brown&Vranesic] Chapter 6 Example 6.1 [full]	CSE460 Lec… CSE460 Lec…
5 [Oct 21 - Oct 26] Oct 23 (Mon) Oct 24 (Tue)	**Lab Test**	Experiment 1 - Experiment 3		
	Theory: Week 5 Lecture 1	System design using moore and mealy type finite state machines (FSM1)	[Brown&Vranesic] Chapter 6 Section 6.2, 6.2.1 [Full], 6.3 Mealy State Model [full] Example 6.2, 6.4	CSE460 Lec…
	Theory: Week 5 Lecture 2	System design using moore and mealy type finite state machines (FSM2)		CSE460 Lec…
6 [Oct 28 - Nov 2]	**Lab**: Experiment 4	Verilog Design Part 3 (FSMs)		CSE460 Lab…
	Theory	Reserved		
7	**Midterm exam**	**Lecture 1 - Lecture 10**		
8	**Lab**: Experiment 5	Verilog Design Part 4 (FSMs)		CSE460 Lab…

[Nov 13 - Nov 16]	Theory: Week 8 Lecture 1	Fabrication of CMOS devices	[Weste&Harris] Chapter 1 1.5 CMOS Fabrication and Layout (1.5.1-1.5.3)	CSE460 Lec…
	Theory: Week 8 Lecture 2	Layouts and stick diagrams	[Weste&Harris] Chapter 1 1.5.5 Stick Diagrams (Full + Example 3)	CSE460 Lec… CSE460 Lec…
9 [Nov 18 - Nov 23]	**Lab**: Experiment 6	CMOS Layout Design in Microwind	CSE 460 Ex…	
	Theory: Week 9 Lecture 1	1. Physical Design	https://nmsu.zoom.us/rec/share/wO2p7vq3qyfhb1mMELK3d3pliaasuQRWnf649-ric_qXzLSd2Ci1GjXtZio8Kze7.DihKlAL49_UpAWnr	CSE460 Lec…
	Theory: Week 9 Lecture 2	Physical Design (algorithm 1)	Video URL: https://nmsu.zoom.us/rec/share/wO2p7vq3qyfhb1mMELK3d3pliaasuQRWnf649-ric_qXzLSd2Ci1GjXtZio8Kze7.DihKlAL49_UpAWnr	CSE460 Lec…
10 [Nov 25 - Nov 30]	**Lab**: Experiment 7	Algorithm implementation using Python	TBA	
	Theory: Week 10 Lecture 1	Physical Design (algorithm 2)	Lecture note	CSE460 Lec…
	Theory: Week 10 Lecture 2	Physical Design (algorithm 2)	Lecture note	CSE460 Lec…
11 [Dec 2 - Dec 7]	**Lab: No lab**			
	Theory: Week 11 Lecture 1	Delay in CMOS circuits(Part1)	[Weste&Harris] Chapter 4 4.2 Transient Response 4.3 RC Delay Model 4.3.1 Effective Resistance 4.3.2 Gate and	CSE460 Lec…

			Diffusion Capacitance 4.3.3 Equivalent RC Circuits	
	Theory: Week 11 Lecture 2	Delay in CMOS circuits(Part2)	[Weste&Harris] Chapter 4 4.3.5 Elmore Delay Example 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9	CSE460 Lec…
12 [Dec 9 - Dec 14]	**Lab**: Presentation	Paper presentation		
	Theory: Week 12 Lecture 1	Power in CMOS circuits	[Weste&Harris] Chapter 5 5.1.1 Definitions 5.1.2 Examples 5.1.3 Sources of Power Dissipation Example 5.1	CSE460 Lec… CSE460 Lec…
	Theory: Week 12 Lecture 2	Power in CMOS circuits (Continued)		CSE460 Lec…
13 [Dec 16 - Dec 24] Dec 16 (Sat)	Lab	Reserved		
	Theory	Reserved		
14	**Final exam**	**Lecture 11 - Lecture 20**		

Course contents

Detailed List of Topics

1. **Week 1**
   - Introduction to VLSI, history, timeline. Moore's law.
   - Review of digital logic design. Complete VLSI flow (top down / bottom up)

2. **Week 2**
   - Logic circuit families: n-MOS, p-MOS, pseudo n-MOS and CMOS technologies. Introduction to CMOS logic. Pull-up and pull-down networks, implementation using series and parallel MOSFETs.
   - Combinational logic circuit design using CMOS. Complex gate design using CMOS such as And-Or-Invert or Or-And-Invert. Implementation of different circuit elements like basic gates.
   - Multiplexers, encoder, latch, flip-flops using CMOS

3. **Week 3**
   - CMOS transistor theory

4. **Week 4**
   - DC Response of CMOS gates. Pass transistors. Logic levels and noise margins. DC transfer characteristics.
   - FSM Introduction
   - FSM moore and mealy type machines
   -

5. **Week 5**
   - System design using moore and mealy type finite state machines
   - Different hardware implementation techniques
6. **Week 6**
   - CMOS Transistor theory: modes of operation. Derivation of I-V characteristics. MOS Capacitance.

7. **Week 7**
   - Midterm week

8. **Week 8**
   - CMOS Fabrication: Inverter cross-section and layout analysis.
   - Layout
   - Masks. Stick diagrams and area estimation. (Eulerian path. Complex examples)

9. **Week 9, 10**
   - Physical design: floorplanning, partitioning, routing, clock tree synthesis.
   - KL algorithm for partitioning.
   - Lee's maze algorithm for global routing

10. **Week 11**
    - Transient response of CMOS gates. Delay definitions: rise time, fall time, propagation delay and contamination delay, RC delay model. Effective resistance. MOS Capacitance.
    - Elmore delay. Parasitic and effort delay. Fan-in and fan-out. Layout comparisons
11. **Week 12**
    - CMOS Power: Instantaneous and Average power, Energy. Power in circuit elements analysis (R, C, DC Supply). Switching waveforms of an inverter. Static power and Dynamic power. Activity factor. Power reduction techniques: Clock gating, Power gating, Dynamic voltage scaling.

FALL 2023-CSE460 Calendar(Tentative)

Day-Month	September		October			November		December	Jan-24
Sunday		1	W2: PQ1(opt); Lab1				31	Final Examinations	
Monday		2							1
Tuesday		3							2
Wednesday		4		1					3 Final Examinations
Thursday		5		2		W6:Quiz2; Lab4/5			4 Last Day of Submitting Grades (PHR)
Friday		6		3			1		5
Saturday	2	7		4		MIDTERM EXAM-CSE460	2		6
Sunday	3	8		5		WEEK 7: MID WEEK [NO CLASS/LAB]	3		7 Publication of Results (PHR)
Monday	4	9	Week3: Lab2	6			4	W11: Quiz-3; L7	8 Last Day of Submitting Grades
Tuesday	5	10					5		9
Wednesday	6 Janmastami*	11		8			6		10 Publication of Results, Fall 2023
Thursday	7	12		9			7		11
Friday	8	13	13	10			8		12
Saturday	9 Classes of Fall 2023 Start (LLB)	14		11		W7: MID WEEK [NO CLASS/LAB]	9	W12: QUIZ-4	13 Payment of Tuition Fees 14 Spring 2024 (14 Jan - 18 Jan)
Sunday	10	15		12			10		
Monday	11 Last Day of Submitting Grades	16	Week4: Quiz1;Lab3	13			11		15
Tuesday	12	17		14		WEEK 8: L5	12	Lab Presentation	16 Registration, Spring 2024
Wednesday	13 Publication of Results, Summer 2023	18		15			13		17
Thursday	14	19		16					18 FYAT DAY
Friday	15	20		17		Undergraduate Admission Test 17 for Spring 2024 (1st Intake) [Tentative]	15		19
Saturday	16	21	Week5: PQ2;Lab4	18		W9: PQ-3; LAB TEST	16		20 Classes of Spring 2024

								Begin & RS Orientation
Sunday	Payment of Tuituion Fees 17 Fall 2023 (17 Sep - 21 Sep)	**22**		**19**		**17**	**W13: PQ4(optional)**	**21**
Monday	**18**	**23**	**Durga Puja (Bijoya Dashami)***	**20**		**18**		**22**
Tuesday	**19 Mid-Term Examinations (PHR)**	**24**		**21**		**19**	**NO LAB**	**23**
Wednesday	**20 Registration, Fall 2023**	**25**	**Week5:PQ2;Lab4**	**22**		**20**		**24**
Thursday	**21 FYAT DAY**	**26**		**23**		**21**		**25**
Friday	**22**	**27**		**24**		**22**		**26**
Saturday	**23 Week1:Class Start**	**28**		**25**		**23**		**27**
Sunday	**24 NO LAB**	**29**		**26**		**24**	**Classes of Fall 2023 End**	**28**
Monday	**25**	**30**	**W6: Quiz2; Lab4/5**	**27**	**Week 10: Lab6**	**25**	**Christmas Day**	**29**
Tuesday	**26**	**31**		**28**		**26**	**FINAL EXAM-CSE460**	**30**
Wednesday	**27**			**29**		**27**		**31**
Thursday	**28 Eid-e-Miladun Nabi***			**30**		**28**		
Friday	**29**					**29**		
Saturday	**30 Week2**					**30**	**Final Examinations**	