1. Suppose you wish to design using Verilog a 8 to 3 priority encoder where the priority follows the sequence 5>0>1>2>6>3>7>4. You also want an extra feature of the encoder, that is, the encoder will have an extra input pin named **flag.** As long as the **flag** is **high** the encoder **will not follow** any priority, it only passes the last **digit of your student id (but if your last digit of id is 8 or 9 then pass 0 to its output)** to its **output**. But when the **flag** is **low** the encoder will follow the **priority** as a regular priority encoder.

2. Suppose you want to develop a circuit using Verilog that can **multiply** a number (minimum **5 bit** in binary) with **2** sequentially in each positive edge of the clock. The multiplier circuit has an input pin named **load,** when the **load** is **high** it will load the **input** to the **output** for performing **multiplication**. For example: if input d = 3 and when load = 1 then input will be loaded in the output q that is q = 3 now.. Then on next positive edge of the clock, q will be 3*2 that is q = 6, then on next positive edge q will be 6*2 that is q= 12 and this will be continued until you get q = 0.

Submission Guidelines:

 # Make a pdf with:

1. Copy the Verilog code and paste it

2. Screenshot of the timing diagram [vector waveform]

3. Screenshot of RTL circuit view

 # Rename the pdf like id_lab3.pdf [If your id is 123 then the pdf name should be 123_lab3.pdf]