

# CSE460: VLSI Design

Lecture 5 + 6



# CMOS Transistor Theory

# Contents

- Introduction
- MOS Capacitor
- nMOS I-V Characteristics
- pMOS I-V Characteristics
- Gate and Diffusion Capacitance

# Introduction

So far, we have treated transistors as ideal switches

An ON transistor passes a finite amount of current

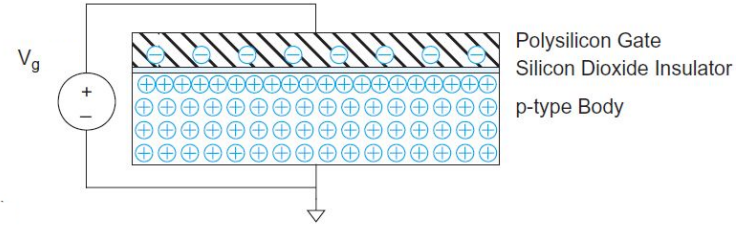
- Depends on terminal voltages
- Derive current-voltage (I-V) relationships

Transistor gate, source, drain all have capacitance

- $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C / I) \Delta V$
- Capacitance and current determine speed

# MOS Capacitor

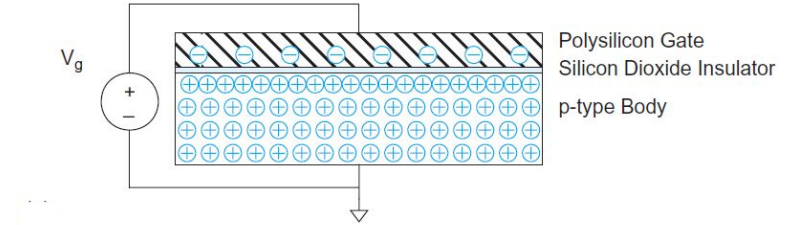
- The MOS transistor is a majority-carrier device
- Current in a conducting channel between the source and drain is controlled by a voltage applied to the gate
  - nMOS majority carriers are electrons
  - pMOS majority carriers are holes
- First, let's examine an isolated MOS structure (of an nMOS) with a gate and body, but no source or drain



# MOS Capacitor: Operating Modes

## MOS Structure

- Top layer: Gate
  - A Good conductor, metal or polysilicon
- Middle layer: Oxide
  - Silicon dioxide, good insulator
- Bottom layer: Silicon (doped)
  - nMOS: p-type, pMOS: n-type



Lets ground the body, connect a voltage source  $V_g$  between the gate and body

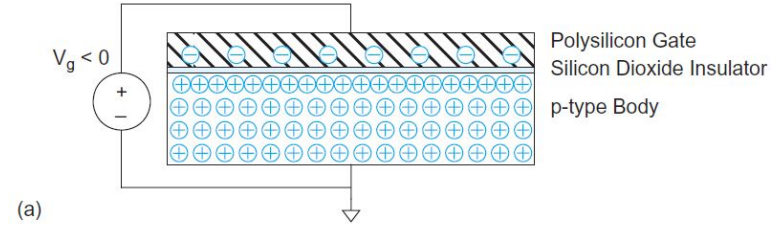
Value of  $V_g$  decides one of three MOS operating modes: (a) Accumulation, (b) Depletion & (c) Inversion

# MOS Capacitor: Accumulation Mode

Case (a):  $V_g < 0$

- a negative voltage is applied to the gate
- there is negative charge on the gate
- The mobile positively charged holes are attracted to the region beneath the gate

This is called the ***accumulation*** mode

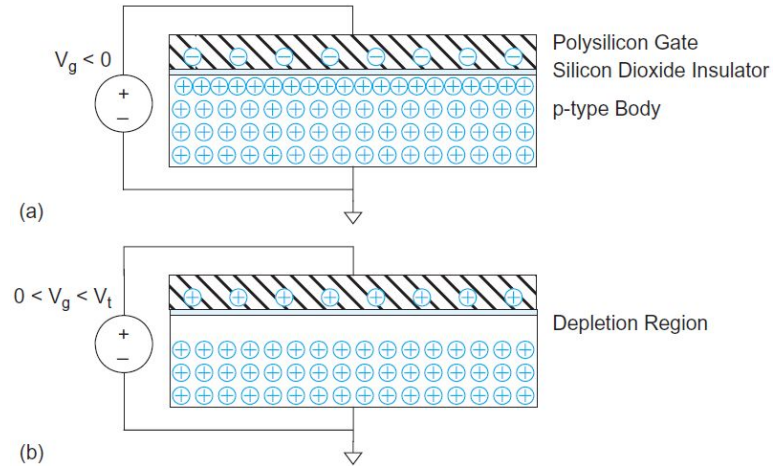


# MOS Capacitor: Depletion Mode

Case (b):  $0 < V_g < V_t$

- a small positive voltage is applied to the gate
- resulting in some positive charge on the gate
- The holes in the body are repelled from the region directly beneath the gate, resulting in a *depletion* region forming below the gate

This is called the **depletion** mode



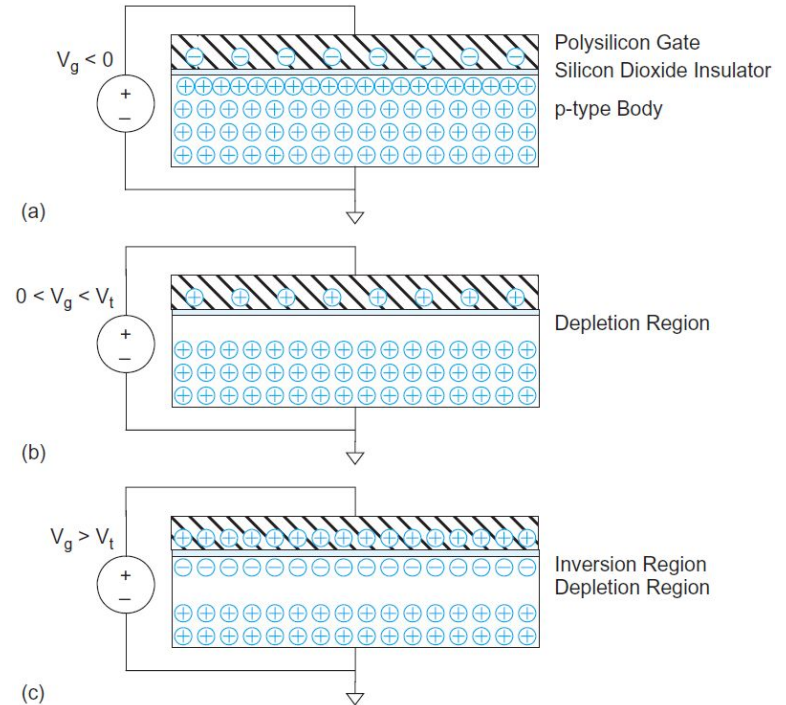


# MOS Capacitor: Inversion Mode

## Case (c): $V_g > V_t$

- a higher positive potential exceeding a critical threshold voltage  $V_t$  is applied
- more positive charge at the gate
- the holes are repelled further
- some free electrons in the body are attracted to the region beneath the gate
- this conductive layer of electrons in the p-type body is called the *inversion layer*

This is called the ***inversion*** mode



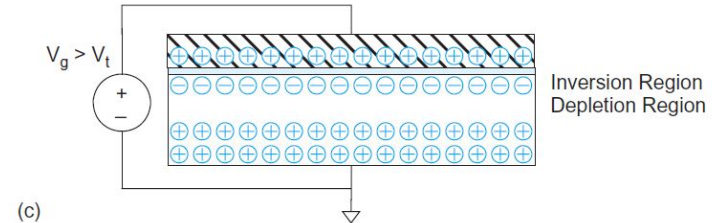
# MOS Capacitor: Inversion Mode

## Observation

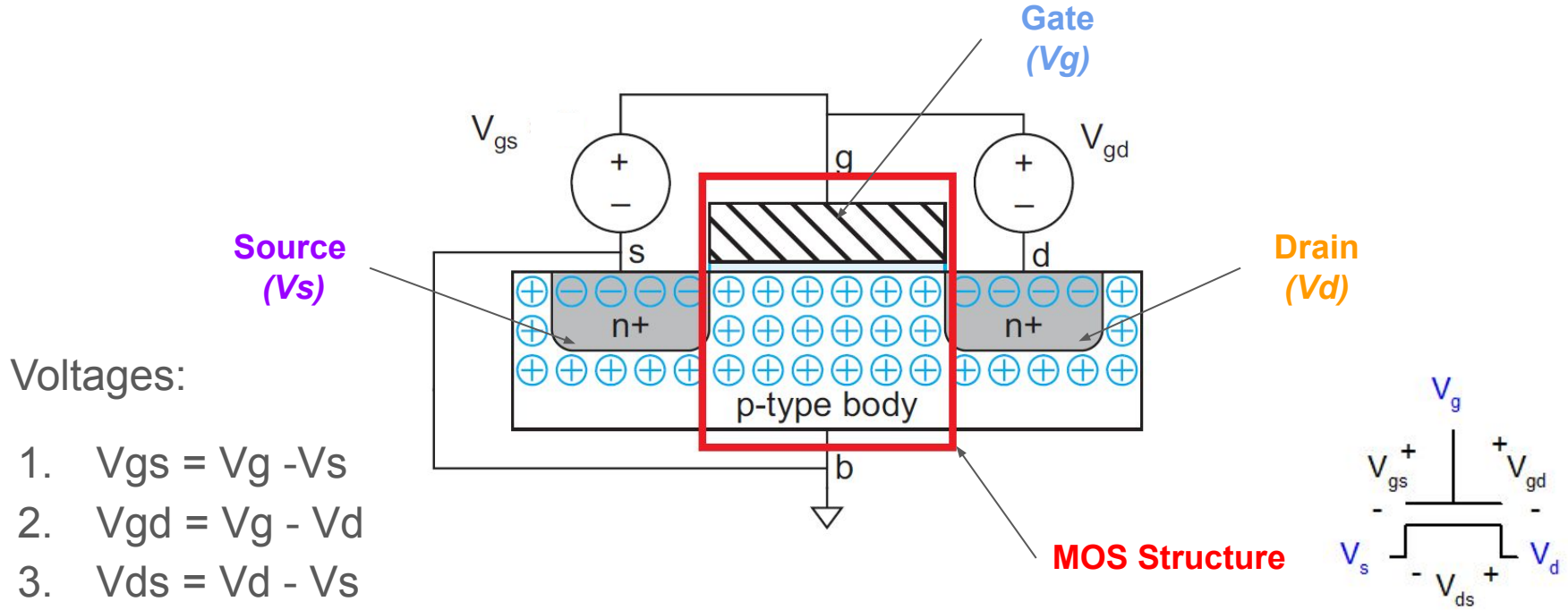
- To conduct current we need a channel between source and drain
- An inversion channel is formed only in the inversion mode when  $V_g > V_t$
- $V_t$  is called threshold voltage ( $V_t > 0$ )

Channel exists in **Inversion mode** ( $V_g > V_t$ )

No channel exists in **Accumulation or Depletion mode** ( $V_g < V_t$ )



# nMOS Transistor



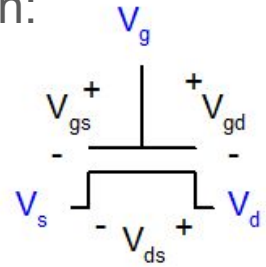
# nMOS Transistor

The gate voltage  $V_g$  merely sets up the conduction path (inversion layer) in the body of the transistor underneath the gate, i.e. it is now ready to conduct current if a voltage is set up across the conducting path, between the source and drain.

The nMOS mode of operation hence depends on all three terminal voltages & the threshold voltage of the transistor:  $V_g$ ,  $V_d$ ,  $V_s$  &  $V_t$

The source and drain are symmetric diffusion terminals. By convention:

- **nMOS** source is at lower voltage than drain while conducting
- Or,  $V_d \geq V_s \Rightarrow V_d - V_s \geq 0 \Rightarrow V_{ds} \geq 0$
- nMOS body is grounded



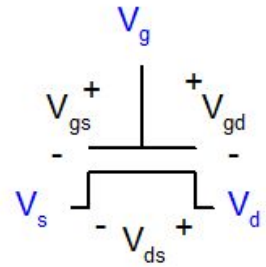
# nMOS Transistor: Operating Regions

Depending on the terminal voltage and their differences, nMOS transistor could be operating in one of the following 3 regions:

1. **Cutoff** (No current flows)
2. **Linear** (Current flows & is *proportional* to the applied voltage)
3. **Saturation** (Current flows & is *independent* of the applied voltage)

We will develop the I-V characteristics for an nMOS transistor

Similar result can be obtained from analysis of a pMOS transistor.



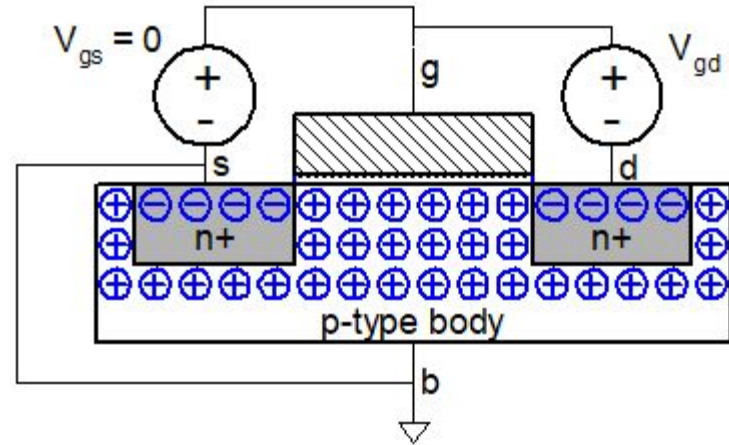
# nMOS Transistor: Cutoff

Conditions:

- $V_{gs} < V_t$
- $V_{ds}$  (doesn't matter)

Results:

- No channel, hence no current
- $I_{ds} \approx 0$  independent of  $V_{ds}$



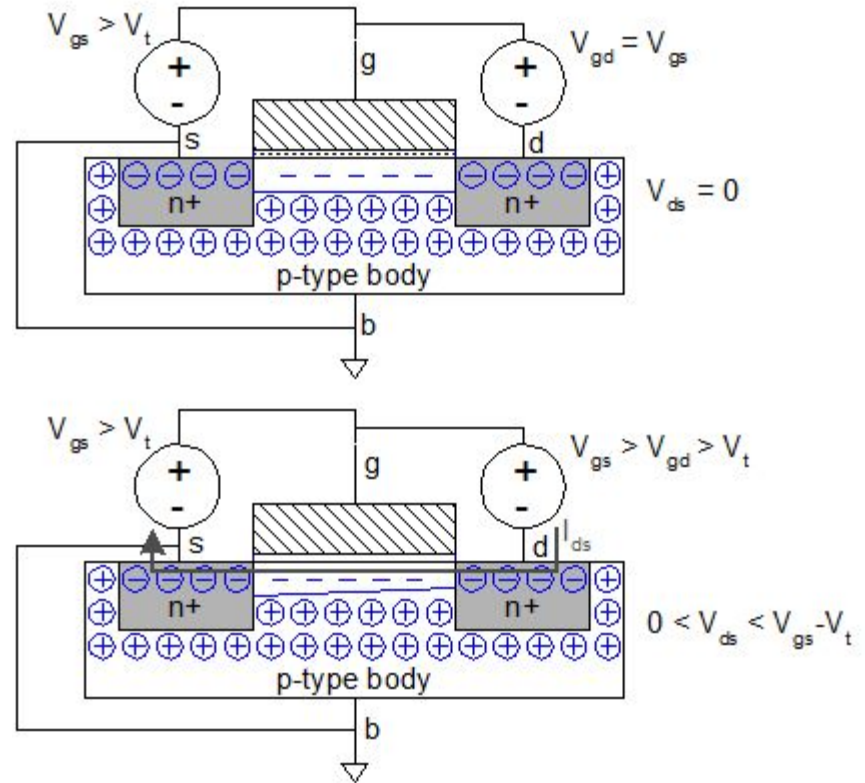
# nMOS Transistor: Linear

Conditions:

- $V_{gs} > V_t$
- $0 \leq V_{ds} < V_{gs} - V_t$

Results:

- Channel forms hence current flows
- $I_{ds} > 0$
- $I_{ds}$  increases with  $V_{ds}$
- Similar to a linear resistor



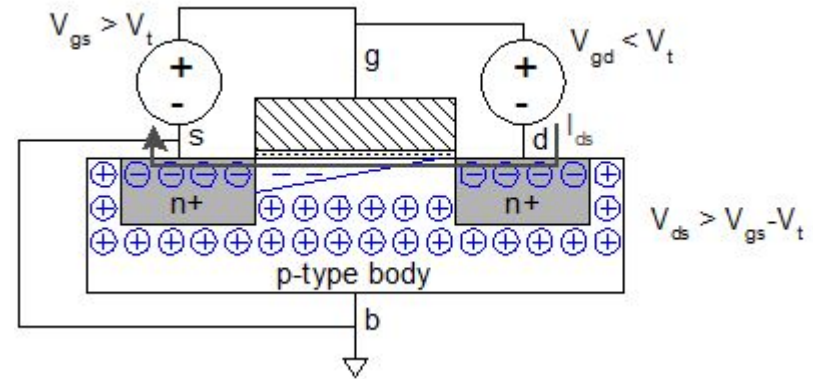
# nMOS Transistor: Saturation

Conditions:

- $V_{gs} \geq V_t$
- $V_{ds} \geq V_{gs} - V_t$

Results:

- Channel forms, hence current flows
- $I_{ds} > 0$
- But channel is pinched off near the drain terminal,  $I_{ds}$  saturates
- $I_{ds}$  is independent of  $V_{ds}$
- Similar to a current source





# nMOS Transistor Operating Regions: Summary

**$V_t$** : nMOS threshold voltage,  **$V_t > 0$**  (nMOS device property)

**$V_{gs}$** : gate to source voltage,  **$V_{gs} = V_g - V_s$**

**$V_{ds}$** : drain to source voltage,  **$V_{ds} = V_d - V_s$**

	$V_{gs} < V_t$	$V_{gs} \geq V_t$
$0 < V_{ds} < V_{ds}(\text{sat})$	Cutoff	Linear
$V_{ds} \geq V_{ds}(\text{sat})$	Cutoff	Saturation

## nMOS Transistor: I-V Summary

$$I_{ds} = \begin{cases} 0 & \text{if } V_{gs} < V_t \text{ (Cutoff)} \\ \beta(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} & \text{if } V_{ds} < V_{ds(sat)} \text{ (Linear)} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & \text{if } V_{ds} \geq V_{ds(sat)} \text{ (Saturation)} \end{cases}$$

Where  $\beta = \mu_n C_{ox} W/L$  &  $V_{ds(sat)} = V_{gs} - V_t$

# pMOS Transistor Operating Regions: Summary

**$V_{tp}$** : pMOS threshold voltage,  **$V_{tp} < 0$**  (pMOS device property)

**$V_{sg}$** : source to gate voltage,  **$V_{sg} = V_s - V_g$**

**$V_{sd}$** : source to drain voltage,  **$V_{sd} = V_s - V_d$**

	$V_{sg} <  V_{tp} $	$V_{sg} \geq  V_{tp} $
$0 < V_{sd} < V_{sd}(\text{sat})$	Cutoff	Linear
$V_{sd} \geq V_{sd}(\text{sat})$	Cutoff	Saturation

## pMOS Transistor: I-V Summary

$$I_{sd} = \begin{cases} 0 & \text{if } V_{sg} < |V_{tp}| \text{ (Cutoff)} \\ \beta_p(V_{sg} - |V_{tp}| - \frac{V_{sd}}{2})V_{sd} & \text{if } V_{sd} < V_{sd(sat)} \text{ (Linear)} \\ \frac{\beta_p}{2}(V_{sg} - |V_{tp}|)^2 & \text{if } V_{sd} \geq V_{sd(sat)} \text{ (Saturation)} \end{cases}$$

Where  $\beta_p = \mu_p C_{ox} W/L$  &  $V_{sd(sat)} = V_{sg} - |V_{tp}|$

# MOSFET Capacitance

Any two conductors separated by an insulator have capacitance

Gate to channel capacitor is very important (**gate capacitance:  $C_g$** )

- Creates channel charge necessary for operation

Source and drain have capacitance to body (**diffusion capacitance:  $C_{sb}$ ,  $C_{db}$** )

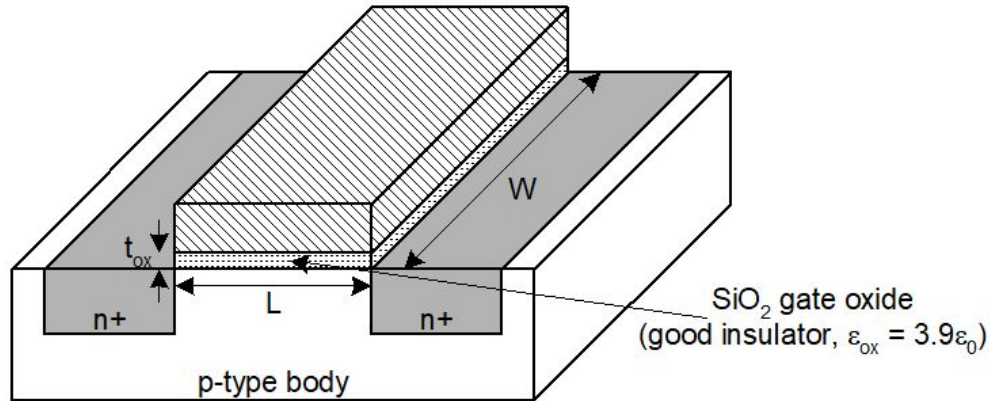
- Across reverse-biased diodes
- Called diffusion capacitance because it is associated with source/drain diffusion
- Remember that nMOS body is connected to ground and pMOS body is connected to supply ( $V_{dd}$ )

# Gate Capacitance

$C_g$  = Gate capacitance

$$C_g = \epsilon_{ox} WL / t_{ox} = C_{ox} WL = C_{permicron} W$$

$C_{permicron}$  is typically about 2 fF/mm



# Diffusion Capacitance

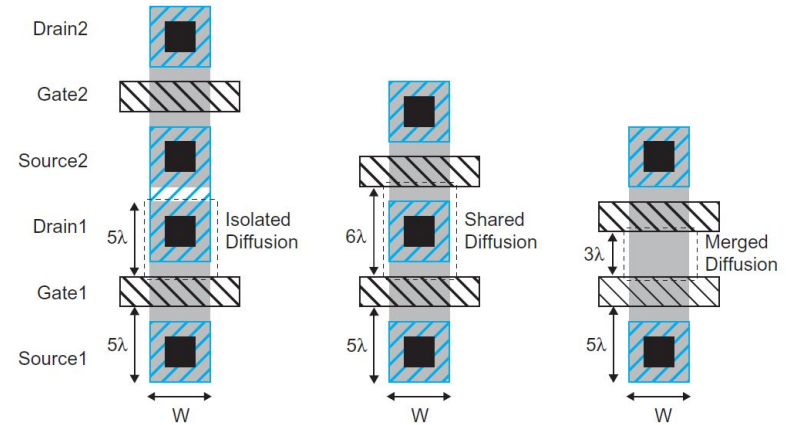
$C_{sb}$  = Source to body capacitance

$C_{db}$  = Drain to body capacitance

Undesirable, called parasitic capacitance

Capacitance depends on area and perimeter

- Use small diffusion nodes
- Comparable to  $C_g$  for contacted diff
- $\frac{1}{2} C_g$  for uncontacted
- Varies with process



Thank You!