CSE460 Book Chapters

Week 01

Readings for lecture 2:

1. [Brown&Vranesic]
    - 2.4 Logic Gates and Networks [Full, up to Functionally Equivalent Networks]
    - 2.3 Boolean Algebra: Axioms of Boolean Algebra, Examples: 2.3, 2.4
    - 4.1 Multiplexers [up to example 4.1(included)]
    - 4.2 Decoders [up to example 4.7(excluded)]
    - 4.3.1 Binary Encoders [Full]
    - 4.3.2 Priority Encoders [Full]
    - 5.3 Gated D Latch [Full, 5.3.1 will be covered in future]
    - 5.4.1 Master-Slave D Flip-flop [Full]

Week 02

Readings for lecture 3:

1. [Weste&Harris] Chapter 1
    - 1.3 MOS Transistors (full)
    - 1.4 CMOS Logic (1.4.1-1.4.5)

Readings for lecture 4:

1. [Weste&Harris] Chapter 1
    - 1.4 CMOS Logic (1.4.6-1.4.9)

Week 03

Readings for lecture 5 &6:

1. [Brown&Vranesic]
    - 6.1 Basic Design Steps

Week 04

Readings for lecture 7:

1. [Brown&Vranesic] Chapter 6
    - Example 6.1 [full]

Readings for lecture 8:

1. [Brown&Vranesic] Chapter 6
    - Section 6.2, 6.2.1 [Full], 6.3 Mealy State Model [full]
    - Example 6.2, 6.4

Week 05

Readings for lecture 9:

1. [Weste&Harris] Chapter 1
    - 1.5 CMOS Fabrication and Layout (1.5.1-1.5.3)

Readings for lecture 10 & 11:

1. [Weste&Harris] Chapter 1
    - 1.5.4 Gate Layouts (full)
    - 1.5.5 Stick Diagrams (Full + Example 3)

Week 06- MIDTERM[Based on week 1-5]

Week 07

Readings for lecture 13:

1. [Weste&Harris] Chapter 2
    - 2.1 Introduction
    - 2.2 Long-channel I-V Characteristics

Readings for lecture 14:

1. [Weste&Harris] Chapter 2
    - 2.2 Long-channel I-V characteristics
    - Example 2.1
    - 2.3.1 Simple MOS capacitance models (only the part covered in video)

Week 08

Readings for lecture 15:

1. [Weste&Harris] Chapter 2
    - 2.5 DC Transfer Characteristics
        - 2.5.1 Static CMOS Inverter DC Characteristics

- 2.5.2 Beta Ratio Effects

Readings for lecture 16:

1. [Weste&Harris] Chapter 2

- 2.5.4 Pass Transistor DC Characteristic

2. [Weste&Harris] Chapter 2

- 5.1.1 Definitions
- 5.1.2 Examples
- 5.1.3 Sources of Power Dissipation
- Example 5.1

Week 09

Readings for lecture 17:

1. [Weste&Harris] Chapter 4

- 4.2 Transient Response
- 4.3 RC Delay Model
- 4.3.1 Effective Resistance
- 4.3.2 Gate and Diffusion Capacitance
- 4.3.3 Equivalent RC Circuits

Readings for lecture 18:

1. [Weste&Harris] Chapter 4

- 4.3.5 Elmore Delay
- Example 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9
- Exercises 4.1 4.2, 4.3, 4.4, 4.5, 4.6, 4.9, 4.18, 4.19

Week 10

Introduction to VLSI Physical Design

Class recording:

https://nmsu.zoom.us/rec/share/wO2p7vq3qyfhb1mMELK3d3pliaasuQRWnf649-ric_qXzLSd2Ci1GjXtZio8Kze7.DihKIAL49_UpAWnr

Week 11- Final [Based on week 7-10]