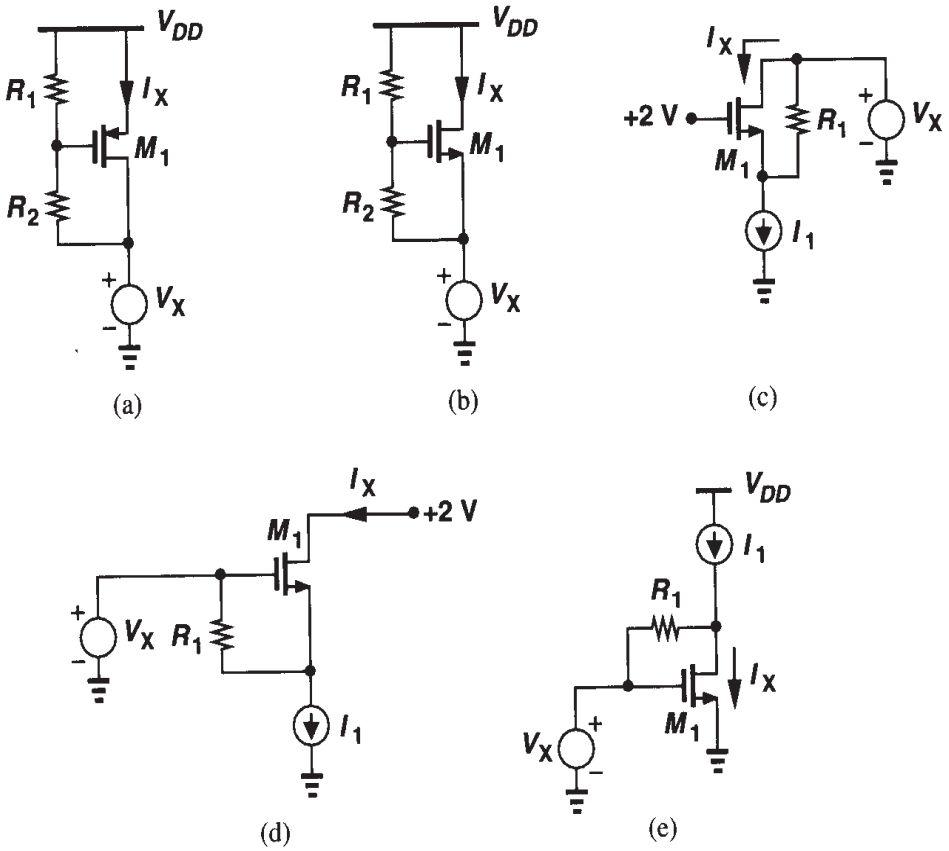


Figure 2.43

2.6. Sketch I_X and the transconductance of the transistor as a function of V_X for each circuit in Fig. 2.43 as V_X varies from 0 to V_{DD}.

2.7. Sketch V_{out} as a function of V_{in} for each circuit in Fig. 2.44 as V_{in} varies from 0 to V_{DD}.

2.8. Sketch V_{out} as a function of V_{in} for each circuit in Fig. 2.45 as V_{in} varies from 0 to V_{DD}.

2.9. Sketch V_X and I_X as a function of time for each circuit in Fig. 2.46. The initial voltage of C_1 is equal to 3 V.

2.10. Sketch V_X and I_X as a function of time for each circuit in Fig. 2.47. The initial voltages of C_1 and C_2 are equal to 1 V and 3 V, respectively.

2.11. Sketch V_X as a function of time for each circuit in Fig. 2.48. The initial voltage of each capacitor is shown.

2.12. Sketch V_X as a function of time for each circuit in Fig. 2.49. The initial voltage of each capacitor is shown.

2.13. The transit frequency, f_T, of a MOSFET is defined as the frequency at which the small-signal current gain of the device drops to unity while the source and drain terminals are held at ac ground.

(a) Prove that

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})}. \tag{2.45}$$

Note that f_T does not include the effect of the S/D junction capacitance.

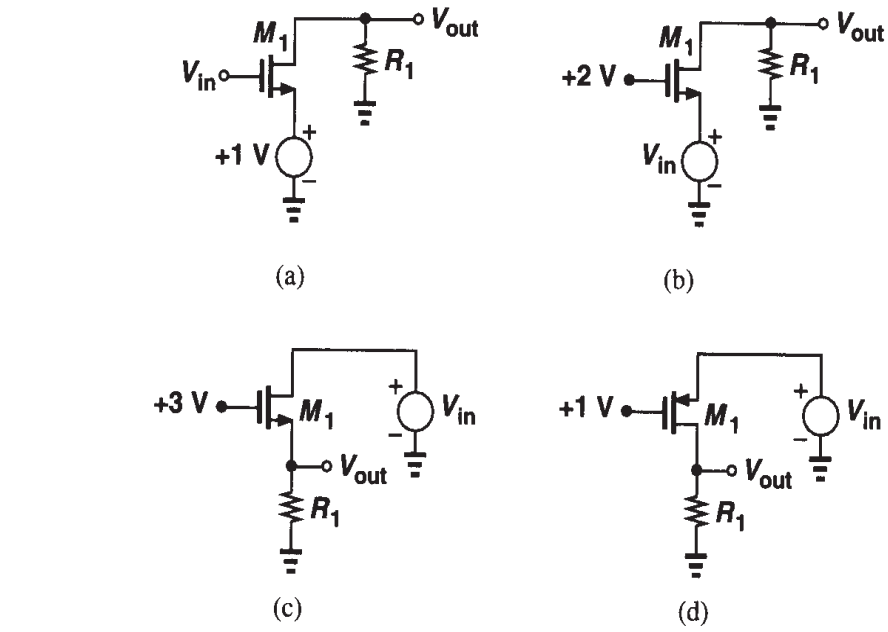


Figure 2.44

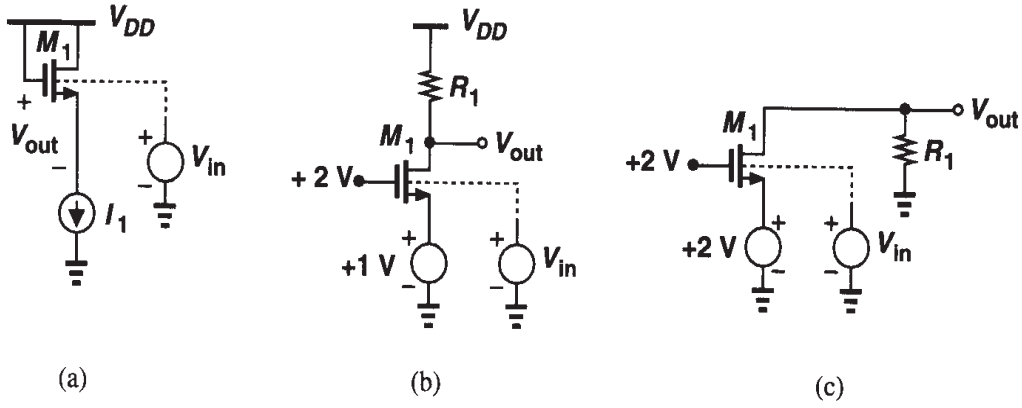


Figure 2.45

(b) Suppose the gate resistance, R_G, is significant and the device is modeled as a distributed set of n transistors each with a gate resistance equal to R_G/n. Prove that the f_T of the device is independent of R_G and still equal to the value given above.

(c) For a given bias current, the minimum allowable drain-source voltage for operation in saturation can be reduced only by increasing the width and hence the capacitances of the transistor. Using square-law characteristics, prove that

$$f_T = \frac{\mu_n}{2\pi} \frac{V_{GS} - V_{TH}}{L^2}. \tag{2.46}$$

This relation indicates how the speed is limited as a device is designed to operate with lower supply voltages.

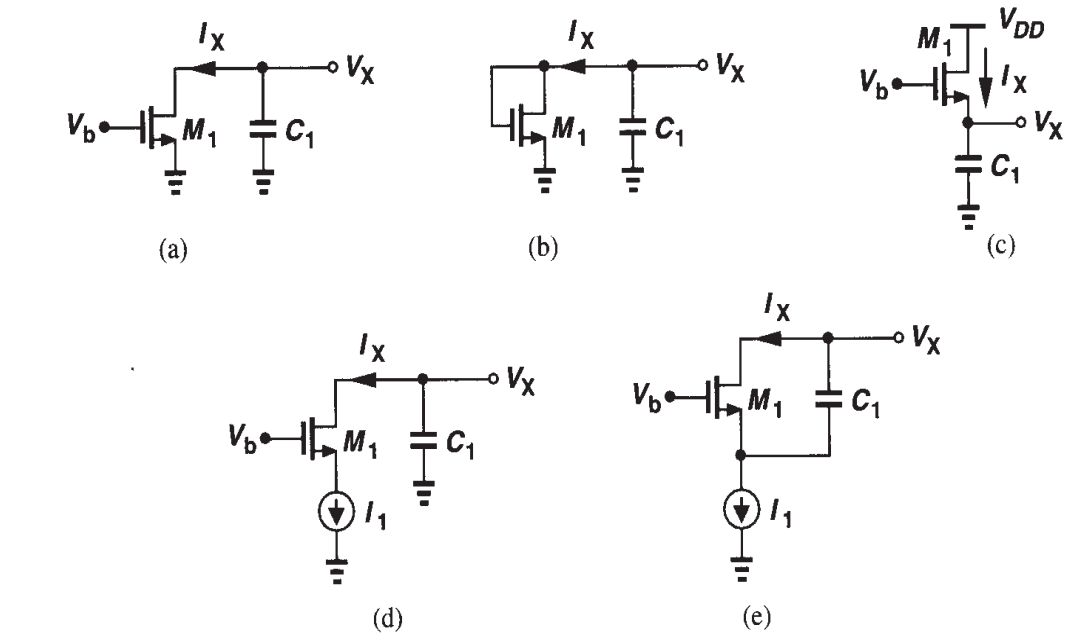


Figure 2.46

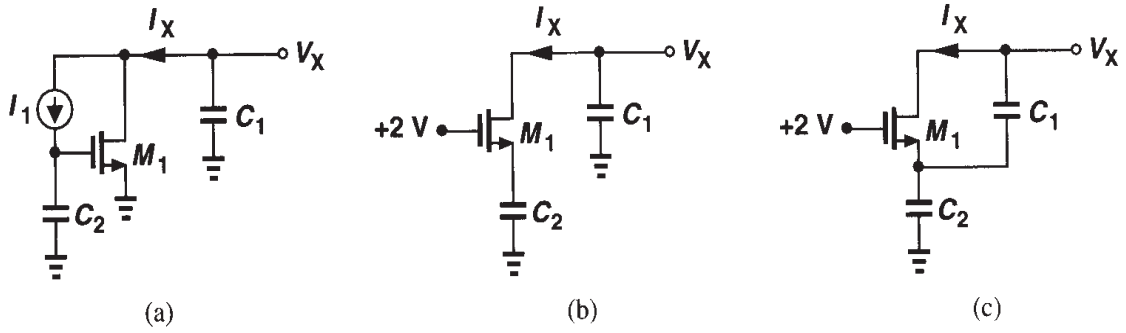


Figure 2.47

2.14. Calculate the f_T of a MOS device in the subthreshold region and compare the result with those obtained in Problem 2.13.

2.15. For a saturated NMOS device having $W = 50\ \mu$m and $L = 0.5\ \mu$m, calculate all of the capacitances. Assume the minimum (lateral) dimension of the S/D areas is $1.5\ \mu$m and the device is folded as shown in Fig. 2.32(b). What is the f_T if the drain current is 1 mA?

2.16. Consider the structure shown in Fig. 2.50. Determine I_D as a function of V_{GS} and V_{DS} and prove that the structure can be viewed as a single transistor having an aspect ratio $W/(2L)$. Assume $\lambda = \gamma = 0$.

2.17. For an NMOS device operating in saturation, plot W/L versus $V_{GS} - V_{TH}$ if (a) I_D is constant, (b) g_m is constant.

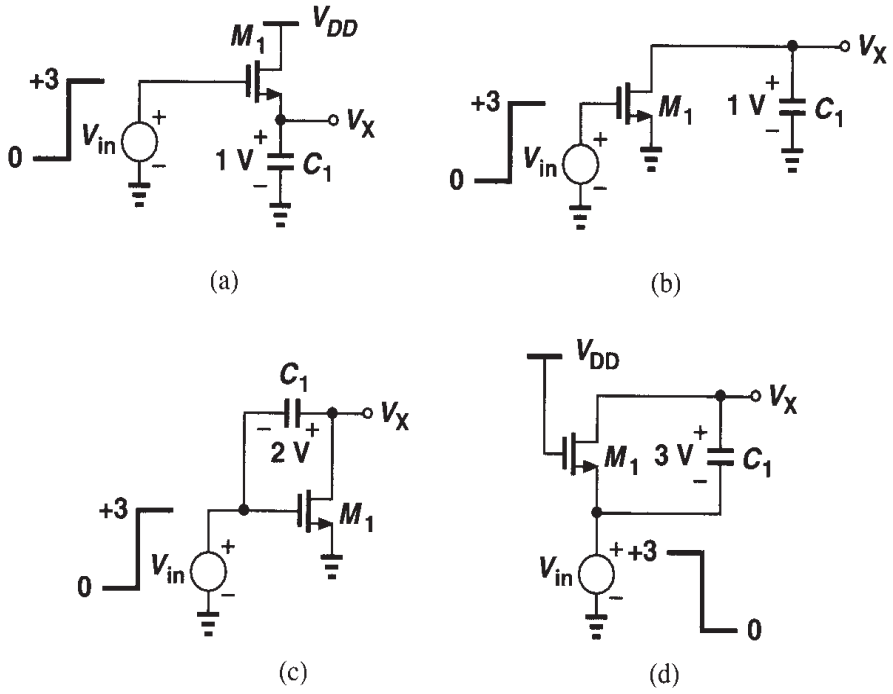


Figure 2.48

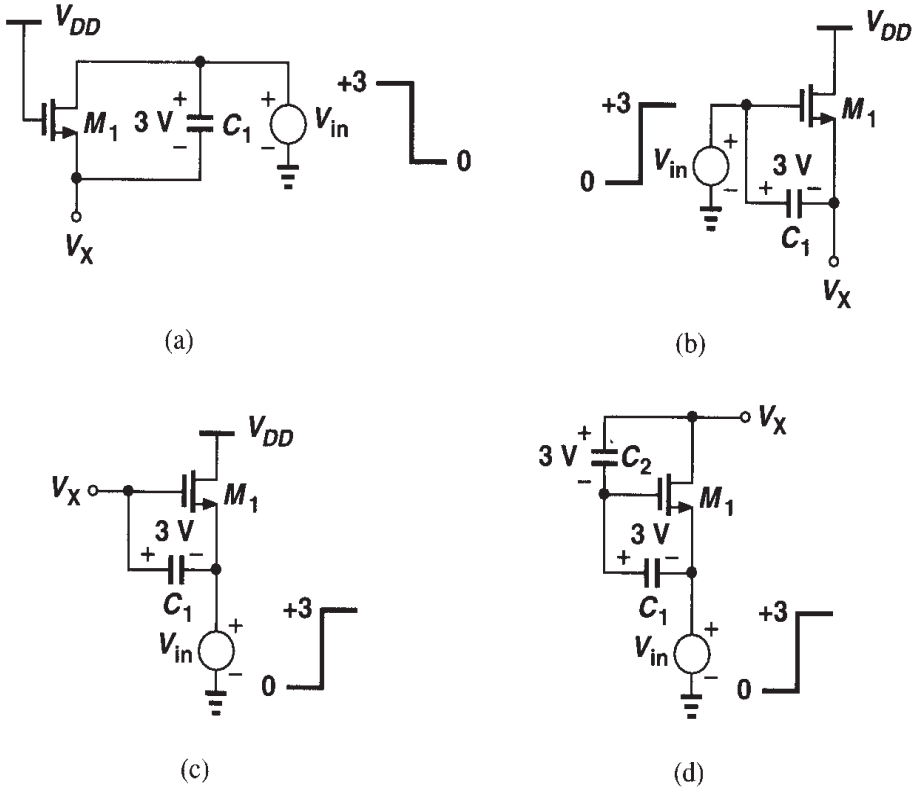


Figure 2.49

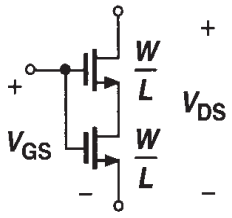
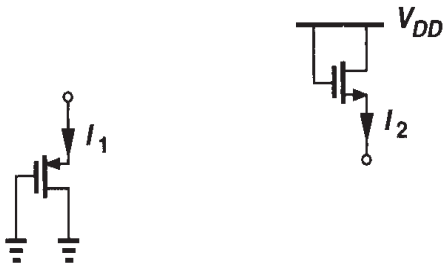


Figure 2.50

2.18. Explain why the structures shown in Fig. 2.51 cannot operate as current sources even though the transistors are in saturation.



(a) (b)

Figure 2.51

2.19. Considering the body effect as "backgate effect," explain intuitively why γ is directly proportional to $\sqrt{N_{sub}}$ and inversely proportional to C_{ox}.

2.20. A "ring" MOS structure is shown in Fig. 2.52. Explain how the device operates and estimate its equivalent aspect ratio. Compare the drain junction capacitance of this structure with that of the devices shown in Fig. 2.32.

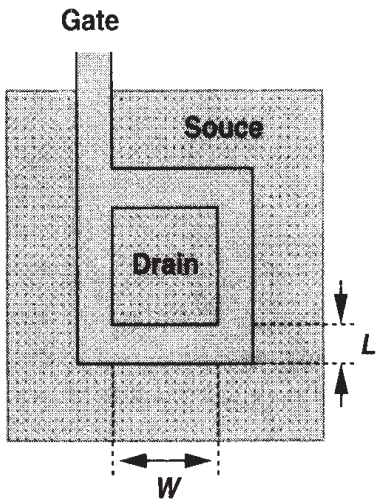


Figure 2.52

2.21. Suppose we have received an NMOS transistor in a package with four unmarked pins. Describe the minimum number of dc measurement steps using an ohmmeter necessary to determine the gate, source/drain, and bulk terminals of the device.

2.22. Repeat Problem 2.21 if the type of the device (NFET or PFET) is not known.

2.23. For an NMOS transistor, the threshold voltage is known but $\mu_n C_{ox}$ and W/L are not. Assume $\lambda = \gamma = 0$. If we cannot measure C_{ox} independently, is it possible to devise a sequence of dc measurement tests to determine $\mu_n C_{ox}$ and W/L? What if we have two transistors and we know one has twice the aspect ratio of the other?

2.24. Sketch I_X versus V_X for each of the composite structures shown in Fig. 2.53 with V_G as a parameter. Also, sketch the equivalent transconductance. Assume $\lambda = \gamma = 0$.

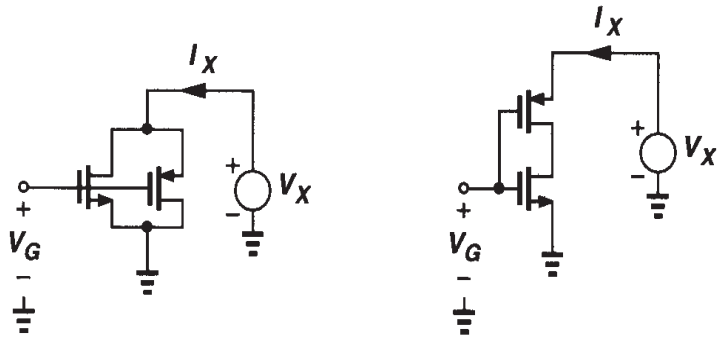


Figure 2.53

2.25. An NMOS current source with $I_D = 0.5$ mA must operate with drain-source voltages as low as 0.4 V. If the minimum required output impedance is 20 kΩ, determine the width and length of the device. Calculate the gate-source, gate-drain, and drain-substrate capacitance if the device is folded as in Fig. 2.32 and $E = 3$ μm.

2.26. Consider the circuit shown in Fig. 2.54, where the initial voltage at node X is equal to V_{DD}. Assuming $\lambda = \gamma = 0$ and neglecting other capacitances, plot V_X and V_Y versus time if (a) V_{in} is a positive step with amplitude $V_0 > V_{TH}$, (b) V_{in} is a negative step with amplitude $V_0 = V_{TH}$.

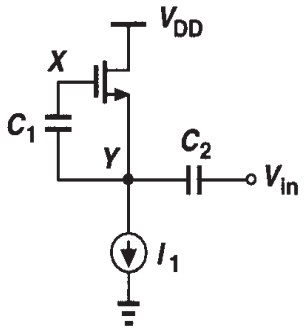


Figure 2.54

2.27. An NMOS device operating in the subthreshold region has a ζ of 1.5. What variation in V_{GS} results in a ten-fold change in I_D? If $I_D = 10$ μA, what is g_m?

2.28. Consider an NMOS device with $V_G = 1.5$ V and $V_S = 0$. Explain what happens if we continually decrease V_D below zero or increase V_{sub} above zero.