# SmartFusion2 MSS

## SPI Configuration

Microsemi

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# Introduction

The SmartFusion2 Microcontroller Subsystem (MSS) provides two SPI hard peripherals (APB_0 and APB_1 sub busses) with optional slave select ports extension.

On the MSS canvas, you must enable (default) or disable each SPI instance based on whether it is being used in your current application. Disabled SPI instances are held in reset (lowest power state). By default, ports of enabled SPI instances are configured to connect to the device Multi Standard I/Os (MSIOs). Note that MSIOs allocated to a SPI instance are shared with other MSS peripherals. These shared I/Os are available to connect to MSS GPIOs and other peripherals when the SPI instance is disabled or if the SPI instance ports are connected to the FPGA fabric.

The functional behavior of each SPI instance must be defined at the application level using the SmartFusion2 MSS SPI Driver provided by Microsemi.

In this document, we describe how you to configure the MSS SPI instances and define how the peripheral signals are connected.

For more details about the MSS SPI hard peripherals, please refer to the SmartFusion2 User Guide.

# 1 – Configuration Options

**Slave Select Extension -** You may drive up to eight slave select signals for each of the SPI instances as master.


***Figure 1-1*** **• SPI Configuration Options**

# 2 – Peripheral Signals Assignment Table

The SmartFusion2 architecture provides a very flexible schema for connecting peripherals signals to either MSIOs or the FPGA fabric. Use the signal assignment configuration table to define what your peripheral is connected to in your application. This assignment table has the following columns (Figure 2-1):

**MSIO -** Identifies the peripheral signal name configured in a given row.

**Main Connection -** Use the drop-down list to select whether the signal is connected to an MSIO or the FPGA fabric.

**Direction -** Indicates if the signal direction is IN, OUT or INOUT.

**Package Pin -** Shows the package pin associated with the MSIO when the signal is connected to an MSIO.

**Extra Connections -** Use the Advanced Options check-box to view the extra connection options:

- Check the Fabric option to observe into the FPGA fabric a signal that is connected to an MSIO.
- Check the GPIO option to observe an input direction signal - from either the FPGA fabric or an MSIO - using an MSS GPIO.

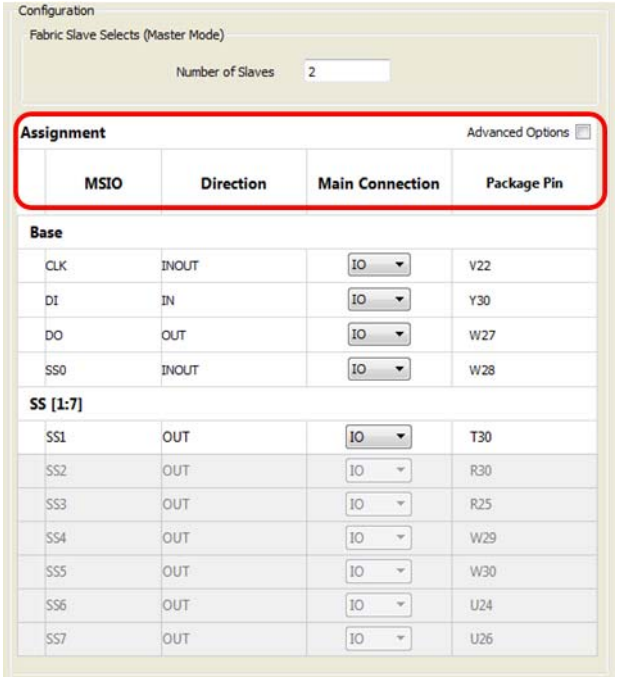


***Figure 2-1* • SPI Peripheral Signals Assignment Table**

# 3 – Connectivity Preview

The Connectivity Preview panel in the MSS SPI Configurator dialog shows a graphical view of the current connections for the highlighted signal row (Figure 3-1).

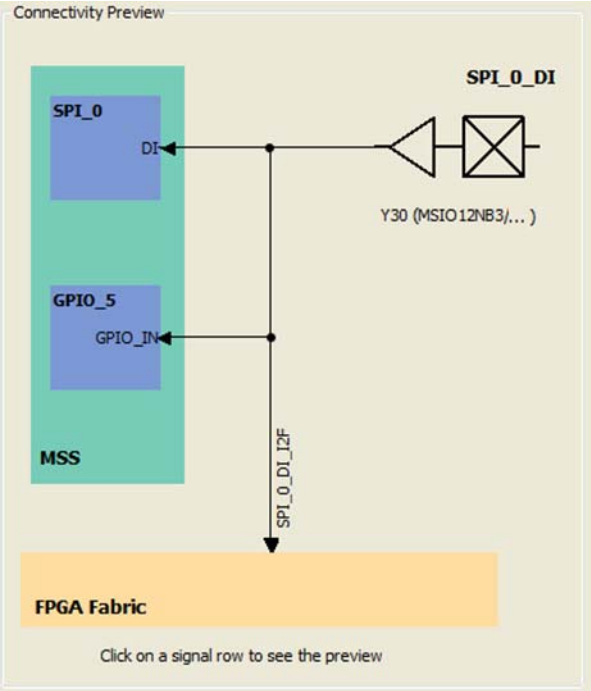


***Figure 3-1*** **• SPI Connectivity Preview**

# 4 – Resource Conflicts

Because MSS peripherals (MMUART, I2C, SPI, CAN, GPIO, USB, Ethernet MAC) share MSIO and FPGA fabric access resources, the configuration of any of these peripherals may result in a resource conflict when you configure an instance of the current peripheral. Peripheral configurators provide clear indicators when such a conflict arises.

Resources used by a previously configured peripheral result in three types of feedback in the current peripheral configurator:

- **Information -** If a resource used by another peripheral does not conflict with the current configuration, an information icon appears in the connectivity preview panel, on that resource. A tooltip on the icon provides details about which peripheral uses that resource.
- **Warning/Error -** If a resource used by another peripheral conflicts with the current configuration, a warning or error icon appears in the connectivity preview panel, on that resource. A tooltip on the icon provides details about which peripheral uses that resource.

When errors are displayed you will not be able to commit the current configuration. You can either resolve the conflict by using a different configuration or cancel the current configuration using the Cancel button.

When warnings are displayed (and there are no errors), you can commit the current configuration. However, you cannot generate the overall MSS; you will see generation errors in the Libero SoC log window. You must resolve the conflict that you created when you committed the configuration by re-configuring either of the peripherals causing the conflict.

The peripheral configurators implement the following rules to determine if a conflict should be reported as an error or a warning.

1. If the peripheral being configured is the GPIO peripheral then all conflicts are errors.
2. If the peripheral being configured is not the GPIO peripheral then all conflicts are errors unless the conflict is with a GPIO resource in which case conflicts will be treated as warnings.

# Error Example

The USB peripheral is used and uses the device PAD bounded to package pin Y30. Configuring the SPI_0 peripheral such that the DI port is connected to an MSIO results in an error.

Figure 4-1 shows the error icon displayed in the Connectivity Assignment table for the DI port.


***Figure 4-1* • Error Displayed in the Connectivity Assignment Table**

Figure 4-2 shows the error icon displayed in the Preview panel on the PAD resource for the DI port.

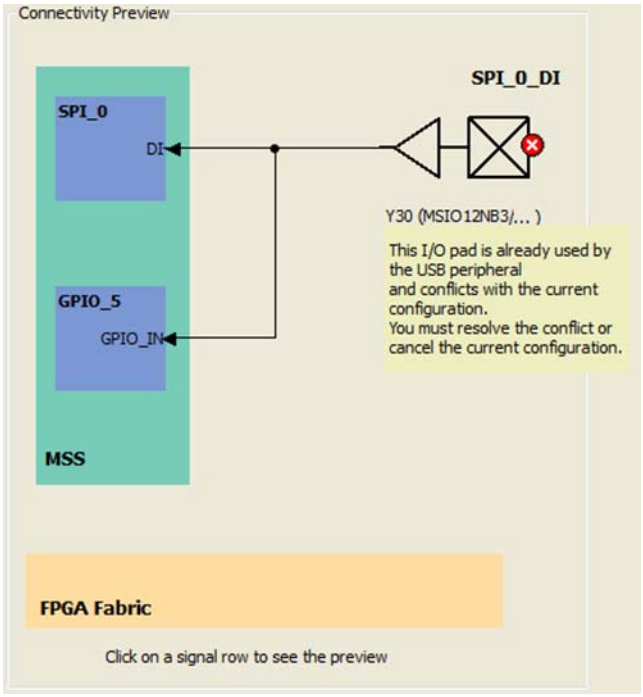


***Figure 4-2* • Error in the Preview Panel**

# Warning Example

The GPIO peripheral is used and uses the device PAD bounded to package pin Y30(GPIO_5). Configuring the SPI_0 peripheral such that the DI port is connected to an MSIO results in a warning.

Figure 4-3 shows the warning icon displayed in the Connectivity Assignment table for the DI port.


***Figure 4-3* • Warning Displayed in the Connectivity Assignment Table**

Figure 4-4 shows the warning icon displayed in the preview panel on the PAD resource for the DI port.

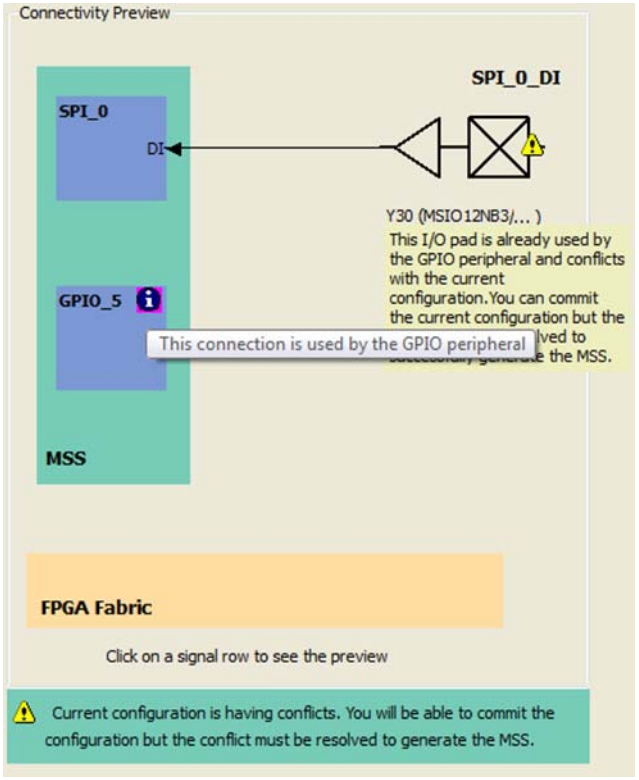


***Figure 4-4* • Warning in the Preview Panel**

# Information Example

The USB peripheral is used and uses the device PAD bounded to package pin Y30. Configuring the SPI_0 peripheral such that the DI port is connected to the FPGA fabric does not result in a conflict. However, to indicate that he PAD associated with the DI port (but not used in this case), the Information icon is displayed in the Preview panel (Figure 4-5). A tooltip associated with the icon provides a description of how the resource is used (USB in this case).

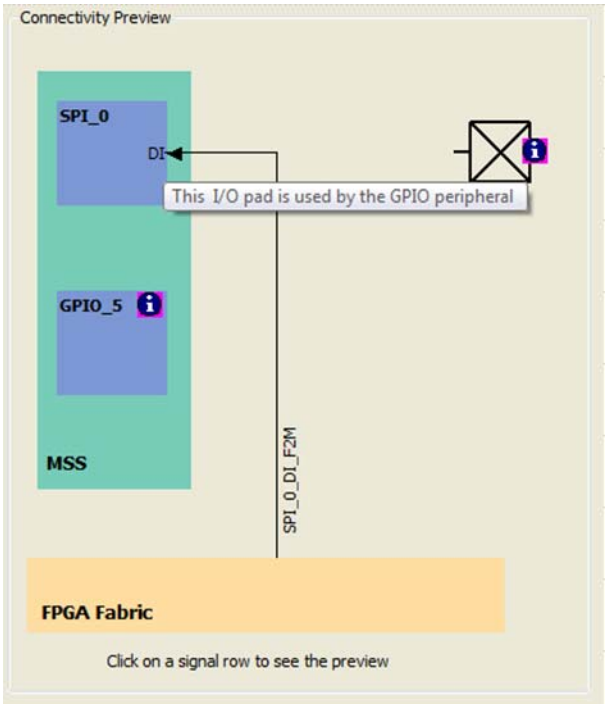


***Figure 4-5* • Information Displayed in the Preview Panel**

# 5 – Port Description

***Table 5-1 •***

| Port Name | Port Group | Direction | Description |
|---|---|---|---|
| DI | SPI_<n>_PADS<br>SPI_<n>_FABRIC | In | Shift data in (master or slave) |
| DO | SPI_<n>_PADS<br>SPI_<n>_FABRIC | Out | Serial data out (generated by SPI as master) |
| CLK | SPI_<n>_PADS<br>SPI_<n>_FABRIC | Inout | Shift clock out (generated by SPI as master) |
| SS0 | SPI_<n>_PADS<br>SPI_<n>_FABRIC | Inout | Dedicated slave select port (generated by SPI as master) |
| SS<1:7> | SPI_<n>_SS_PADS<br>SPI_<n> _SS_FABRIC | Out | Optional slave select ports (generated by SPI as master) |

Note:

- Port names have the name of the SPI instance as a prefix, e.g. SPI_<n>_DI.
- Fabric main connection input ports names have "F2M" as a suffix, e.g. SPI _<n>_DI_F2M.
- Fabric extra connection input ports names have "I2F" as a suffix, e.g. SPI_<n>_DI_I2F.
- Fabric output and output-enable ports names have "M2F" and "M2F_OE" as a suffix, e.g. SPI_<n>_DI_M2F and SPI_<n>_ DI_M2F_OE.
- PAD ports are automatically promoted to top throughout the design hierarchy.

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## Customer Technical Support Center

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Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

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## Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

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