Total No. of Questions : 4] **SEAT No. :**

P8498 **[Total No. of Pages : 1**

Oct.-22/BE/Insem-91

B.E. (E & TC) (Semester - VII)

VLSI DESIGN AND TECHNOLOGY

(2019 Pattern) (404182)

Time : 1 Hour] ***[Max. Marks : 30***

Instructions to the candidates:

1) ***Attempt Q. No. 1 or Q. No. 2 and Q. No. 3 or Q. No. 4.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) What is meant by concurrent and sequential statements in VHDL? Describe with two examples of each. **[5]**

b) What is meant by synthesizable and non-synthesizable statement? Give two example of each. **[5]**

c) Write VHDL code for 4:1 Mux using behavioral modeling style. **[5]**

OR

Q2) a) Write VHDL Code for full adder and its test bench. **[10]**

b) Explain in brief different modeling styles supported by VHDL. **[5]**

Q3) a) What is Clock Skew? What are techniques to minimize it? **[5]**

b) Draw state diagram and write VHDL code and its test bench for sequence detector 101. **[10]**

OR

Q4) a) What is meant by Meta-stability? Explain any one solution in detail. **[5]**

b) Explain clock Distribution Techniques in detail. **[5]**

c) Write Short note on Power Optimization. **[5]**

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