Total No.	of Questions : 4]	SEAT No.:
P5235		[Total No. of Pages : 1
	[6188] 190	
	B.E. (E & TC) (Insen	<b>n</b> )
	VLSI DESIGNAND TECHN	OLOGY
1) A 2) I 3) I	(2019 Pattern) (Semester - VII) (The state of the condidates:  Attempt Q.1 or Q.2 and Q.3 or Q.4.  Draw near diagram's wherever necessary.  Figures to the right indicate full marks.  Assume suitable data, if necessary.	[Max. Marks: 30
	6.	
<b>Q1</b> ) a)	Draw and explain design flow of VLSI.	[8]
b)	Write VHDL code for 8:1 mux using struc	tural style of modeling. [7]
<b>Q2</b> ) a)	OR  Explain different modeling styles in VHD	L. [8]
b)	Write VHDL code for 4 - bit ALU to perfo	orm different eight operations
9)		[7]
<b>Q3</b> ) a)	Explain and compare moore and mealy m	
b)	Write short note on clock skew and clock	jitter. [7]
	OR	9' 1
<b>Q4</b> ) a)	Write short note on noise margin.	[5]
b)	Explain signal integrity issues.	[5]

Write short note on power distribution techniques

**[5]** 

c)