

KLE DR. M. S. SHESHGIRI COLLEGE OF ENGINEERING AND TECHNOLOGY, BELAGAVI

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

INTERNAL ASSESSMENT TEST-1 (CBCS FORMAT)

CS FORMAT)



Code: 15CS72 Date: 19-9-19 Subject:Advanced Computer Architecture Duration:75 minutes

<u>Semester: VII Max. Marks:</u> 30 <u>Staff: Dr. V.S. Mallemath / Geeta N</u>

NOTE: Answer 3 full Questions (Question no 1 is compulsory).

Q 1 a.List and briefly explain the system attributes that affect the performance factors of a Computing System.

Determine the effective CPL MIPS rate, and execution time for this program.

b. A 600 MHz processor is used to execute a benchmark program with the following instruction mix and clock cycle counts:

Instruction type	Instruction count	Clock cycle count
Integer Arithmetic .	550000	1
Data transfer	300000 /	2
Floating Point	100000 .	2
Control Transfer	80000	2

better time the effective C11, 1131 5 rate, and execution time to this program		
Q 2 a. With neat block diagrams, explain the Flynn's classification of Computer Architecture. b. What are the conditions of parallelism?	6 mks. 4mks.	
Q 3. Explain the different types of Data dependence with an example for each.	10 mks.	
Q 4. a. What are the metrics affecting scalability of a computer system? b. What are the important characteristics of par Alel algorithms?	6 mks. 4 mks.	



KLE DR. M. S. SHESHGIRI COLLEGE OF ENGINEERING AND TECHNOLOGY, BELAGAVI



DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

INTERNAL ASSESSMENT TEST - 2 (CBCS FORMAT)

Code: 15CS72

Subject: Advanced Computer Architecture

Semester: VII

Max. Marks: 30

Staff: Dr. V.S. Mallemath /Geeta N

Date: 24-10-19

Duration: 75 minutes

NOTE: Answer 3 full Questions (Question no 1 is compulsory).

Q.	QUESTIONS	MARKS
No.	List out the characteristics of a typical RISC and CISC architecture and bring out the architectural	5+5
	a. With a neat sketch, explain the hierarchical memory technology.	5
2.	b. What a neat sketch explain the inclusion property and data transfer between adjacent levels of memory hierarchy.	5
3.	What is arbitration? Explain Central and Distributed arbitration schemes	2+8
4.	Explain the Direct mapping cache organization with an example of modulo 4 mapping.	10

....

Internal Assessment 3

ubject: Advanced Computer Architecture (15CS72)

Sem: VII Sem.

NOTE: Answer 3 full Questions with Question no 1 compulsory

- 1. a. Compare sequential and weak consistency models. ----- 5 marks
 - b. State the conditions required to maintain Sequential Consistency. ----- 5 marks
- 2. a. Differentiate Linear Pipeline processors from Nonlinear Pipeline processors.---- 5 marks
- b. With respect to Instruction pipelining, explain internal data forwarding, pre-fetch buffer and possible hazards between read and write operations. ----- 5 marks
- 3. Ja. Explain cache coherence problem.----5 marks
- b. Explain Snoopy bus protocols.-----5 marks
- 4. a. With a neat diagram explain Tomasulo's algorithm & give advantages of the approach-5 marks
 - b. Explain directory-based protocols in brief.----5 marks