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Low Cost Universal Programmable Digital Function Generator

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ABSTRACT

The design of a Low cost EPROM based digital function generator producing several waveforms with adjustable frequency is discussed in the paper. This can be developed into an economic, user friendly, commercial product suitable for academic purposes as well as R&D labs.

Keywords: Function generator, Master oscillator, Microcontroller, debounce circuit, Frequency ranging.

INTRODUCTION

A function generator is a versatile instrument that gives users a choice of selecting different waveforms such as Sinusoidal, Triangular, Square and sawtooth etc. whose amplitude and frequency are adjustable over a wide range. Generally for lab purpose there are two types of function generators are available; analog and digital.
In analog function generator, the signal is a continuous function of time and a smooth curve is obtained for the signals. The sine wave being the most commonly used test signal, various techniques are employed in generating the sine wave like Wein-bridge and LC oscillators for low and high frequency respectively. In practice, the technique employed for general function generation involves the use of square waveform generator as the basic unit with precision limiters used for obtaining a sine function.

METHODOLOGY

A digital function generator on the other hand, is build around a programmable device generally an EPROM. The digital codes of the various functions are stored as look up tables. The waveforms so stored in digital form are converted into analog form using a DAC. The universal programmable function generator (UPDFG) facilitates several functions in addition to sine, triangular, sawtooth, square and staircase

etc. with ease and compactness. The block schematic of the implementation is shown in figure 1.

The master oscillator supplies clock to an 8 bit counter. In the range selection, the clock frequency is divided into six decades and a fine variation within each decade can be obtained. The 8 bit counter generates counts from 00H to FFH providing the address for the EPROM. The EPROM is a memory unit which stores digitised information of the waveforms required. The required wave form is selected using the function selection circuit. The digitised information from EPROM is converted into analog form using a Digital to Analog Converter (DAC). The amplitude variation of the waveforms at the output is provided by the means of a gain control circuit of the amplifier.

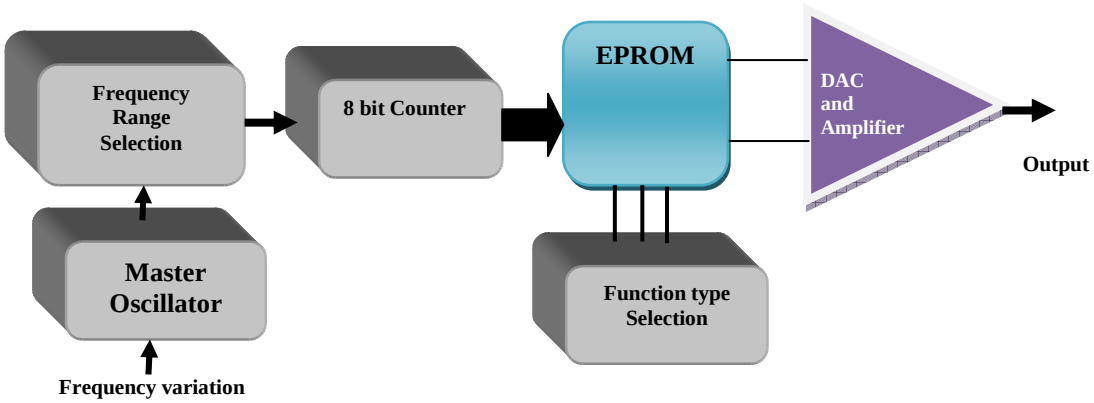

Figure 1. Block diagram of Digital function Generator (UPDFG).

Function Lookup table

The function lookup table implementation comprises of an EPROM and an 8 bit synchronous counter. The EPROM is configured as an 8 page memory. The page addresses are generated using the first three most significant bits A_{10} - A_8 and the locations on any page are addressed using bits A_7-A_0. The lookup table for each function is stored on a unique page on the memory. The table1 details the functions stored on different pages. The addresses of locations on each page are generated using 8 bit synchronous counter. The outputs of the counter are connected to the address lines A_7-A_0 of EPROM through a TTL buffer.

Table1. Lookup table allocation

FUNCTION	PAGE No.	PAGE Address
RAMP	0	000
TRIANGULAR	1	100
SQUARE	2	200
STAIRCASE	3	300
SINE	4	400

The lookup tables for sample waveforms are given in appendix section.

Function selection

The digital selection of function is achieved using a 3 bit counter. Since one function occupies only one page in the

memory, the page addresses need to be generated as per the table1 to select any function. This is done using a single key by the user with a switch debounce circuit.

Frequency Ranging

The master oscillator is implemented using a VCO chip to operate over a frequency range of100kHz to 1MHz, linearly by means of a potentiometer. The output of the oscillator drives a six stage decade counter. The output of each of these corresponds to one decade and linear variation within any decade is obtained by means of the potentiometer. The output of decade counters are connected to the clock input of the 8 bit counter through a 8:1 multiplexer. The desired decade is selected by addressing the multiplexer inputs. These addresses are again generated by employing the method used for function selection.

Output Section

The output section consists of an 8 bit bipolar DAC and an amplifier. The digital codes pertaining to any function are connected to the DAC input by sweeping the locations on the corresponding page of the EPROM by means of function select and frequency ranging circuits. The DAC provides the corresponding output, thus generating the selected analog function. The amplitude of the waveform generated is controlled by adjusting the gain of the inverting amplifier by means of a potentiometer.

Power Supply

The necessary power supply for all the circuits mentioned in the foregoing sections namely ±15V, + 5V and 10 V are designed using standard IC regulators.

Calibration and Testing

The two sub units of the digital function generator namely the VCO master oscillator and the DAC need calibration. The VCO is calibrated for the desired range frequencies by trimming the potentiometer for minimum and maximum frequencies. The DAC is calibrated for the symmetrical bipolar outputs of ±10V by adjusting its reference voltage.

The circuit is tested for the following;

Function selection, frequency ranging and output amplitude control.

Future Scope

By looking at today's developments in microcontrollers, this system can be modified to work in conjunction with a microcontroller. That could make the present implementation more flexible, user friendly incorporating features like user programmable functions, digital control of gain, alpha numeric display for the function produced, its amplitude and frequency. Also by employing clock circuitry with a suitable high frequency crystal, the range of frequencies for the waveforms can be extended.

CONCLUSION

The digital function generator (UPDFG) implemented satisfies the specifications listed in table 2.

Table 2: Specifications

Input supply	Single phase 230V, 50 Hz AC
Base oscillator frequency	100kHz -1 MHz
Range selection	6 decades, digitally selected (single key)
Functions (waveforms)	Sine, Square, Triangular, Ramp, Staircase
Function select	Digital (Single Key)
Output amplitude	20Vpp max ; potentiometer adjustment
Output impedance	50Ω (Opamp output)

The greatest advantage of the implemented digital function generator lies in its design as it consists of only EPROM as a memory unit which doesn't require any programming language to load data into it. But as a semiconductor memory unit it requires an external programming unit through which the data can be written into the EPROM.

REFERENCES

1. Digital fundamentals: T. L. Floyd, Universal Book Stall,8th edition,(2005).
2. Digital principles and applications – Malvino and Leach, 5th edition TMH, (2000).
3. Operational amplifier and linear circuits, Ramakanth Gayakwad, PHI, 3rd Edition, (2005).
4. Digital logic and computer design: M. Morris Mano – PHI 4th edition, (2002).
5. Device (Opamp, DAC) data sheet- National semiconductor.
6. Device data sheet (EPROM)- Intel.
7. Electronic Devices and circuits, T.F. Bogart and Beasley, Pearson Education, 6th Edition, (2004).
8. Electronic Instrumentation and measuring Techniques, W. D. Cooper, A.D. Helfrick 3rd Edition, PHI, (2000).