EE60032: Analog Signal Processing

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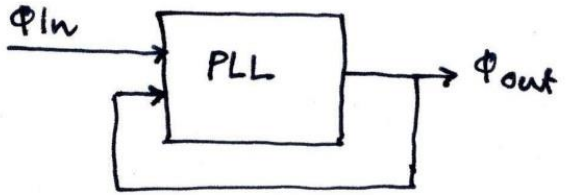
Module-4: Phase Locked Loop and Oscillators

Phase locked Loop (PLL)

- **What is PLL?**

  PLL is a negative feedback system that compares the output phase with input reference phase. i.e., $\Phi_{out} = \Phi_{in}$.



- **What is the purpose?**

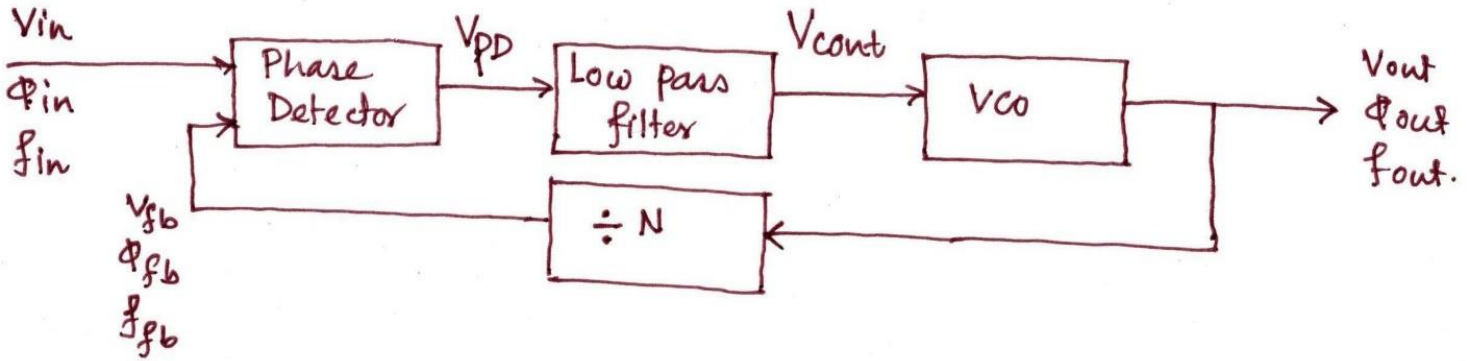
  If phases are same, frequencies are same.

  $f = \frac{\Delta\Phi}{\Delta t}$; $\frac{d\Phi_{out}}{dt} = \frac{d\Phi_{in}}{dt} \Rightarrow f_{out} = f_{in}$.

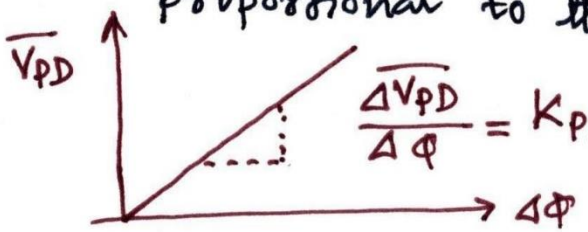
- **Why do we need PLL?**
  - An oscillator with a stable frequency is difficult to get.
  - Crystal oscillators are costly, but offers a stable frequency at low range.
  - If $f_{out} \neq f_{in}$ and/or $f_{out1}, f_{out2}, f_{out3} \ldots \neq f_{in}$, then you need a PLL.

- **Applications:-**
  - Frequency synthesis
  - clock recovery

- **Block Diagram:-**

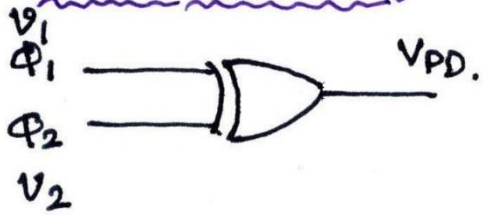


Phase detector :- A phase detector is a ckt whose average output voltage $\overline{V_{PD}}$ is linearly proportional to the input phase difference ($\Delta\phi$).



$$\frac{\Delta \overline{V_{PD}}}{\Delta \phi} = K_{PD} = \text{gain of PD.}$$

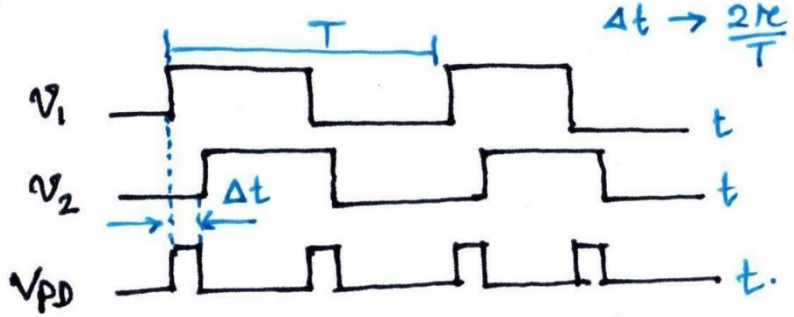
Implementation :-



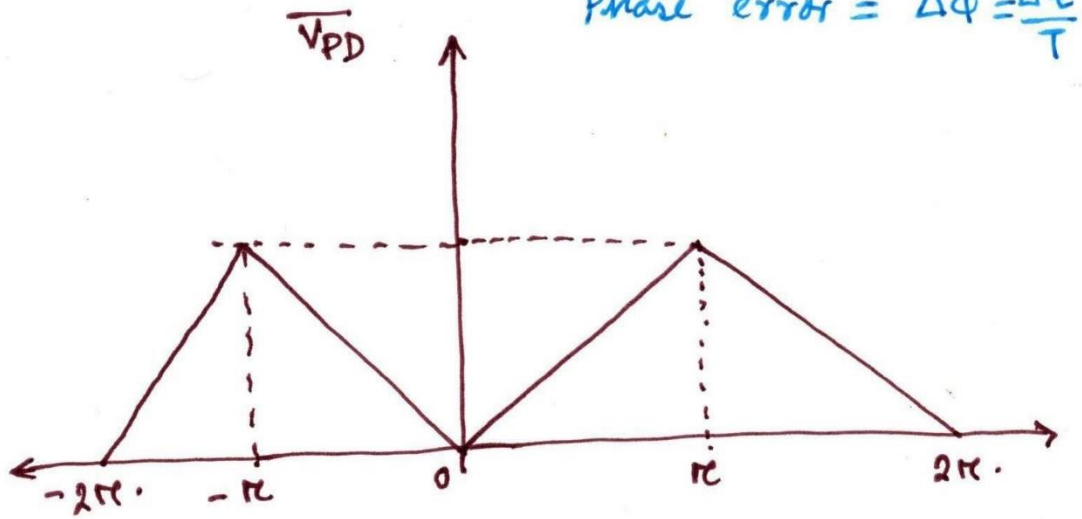
$$V_{PD} = v_1 \oplus v_2$$
$$= v_1 \bar{v}_2 + v_2 \bar{v}_1$$

v_1	v_2	v_{PD}
0	0	0
0	1	1
1	0	1
1	1	0

$T \rightarrow 2\pi$
$\Delta t \rightarrow \frac{2\pi}{T}\Delta t$.



Phase error $= \Delta\phi = \frac{\Delta t}{T} \cdot 2\pi$.



Static characteristic of PD.

PLL waveforms under Locked Condition

- Generalised expression :-

1) VCO :-

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$

ω_0 = free running freq. when $V_{cont} = 0$.

K_{VCO} = Gain of the VCO.

2) PD :-

$$\overline{V_{PD}} = V_{cont} = K_{PD} \Delta\phi_0$$

K_{PD} = Gain of the PD.

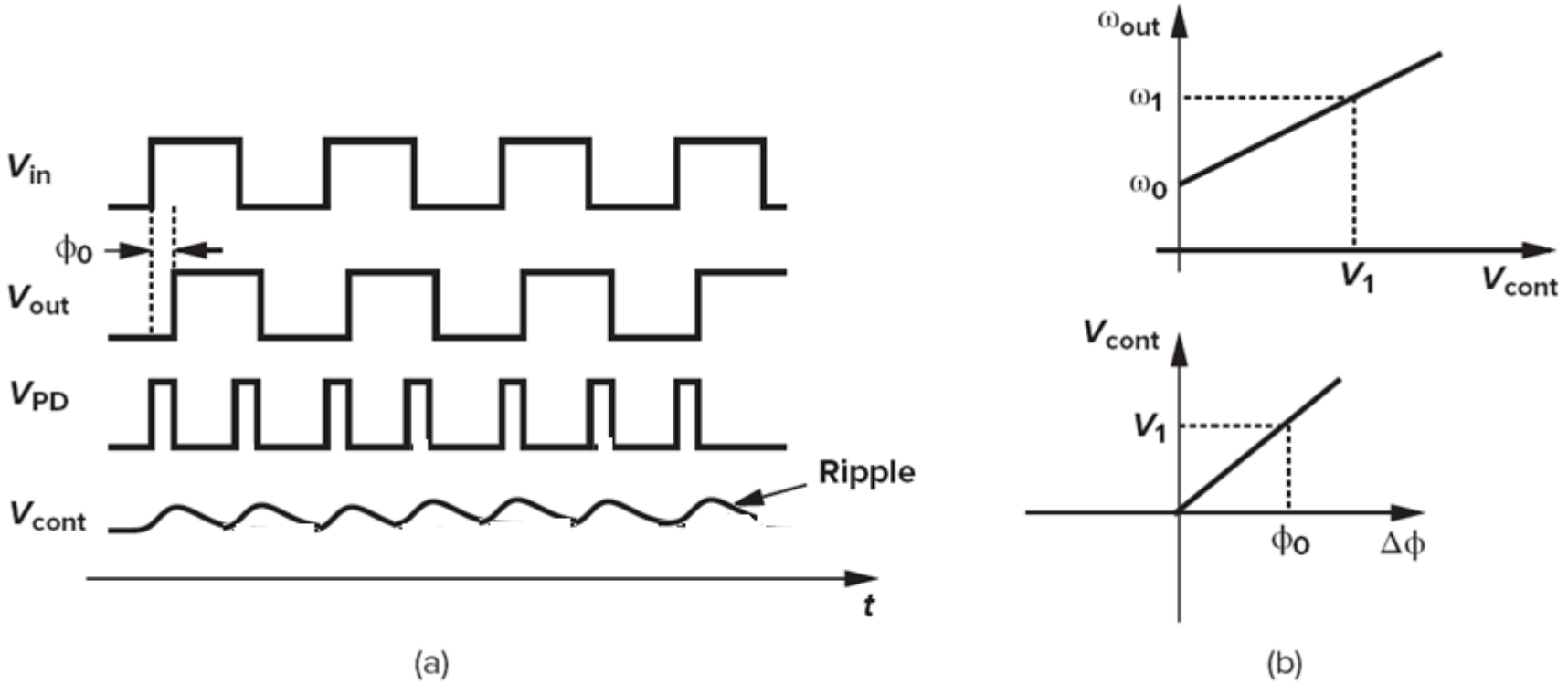
- If $\omega_{in} = \omega_1$, then $\omega_{out} = \omega_1$ under locked condition.

$$\omega_1 = \omega_0 + K_{VCO} \cdot V_1$$

or, $$V_1 = \frac{\omega_1 - \omega_0}{K_{VCO}}$$

and $$V_1 = K_{PD} \Delta\phi_0$$

So, $$\boxed{\Delta\phi_0 = \frac{\omega_1 - \omega_0}{K_{VCO} K_{PD}}}$$



(a) Waveforms in a PLL in locked condition; (b) calculation of phase error.

Observations :-

1) To minimise phase error, K_{VCO}, K_{PD} must be high.
2) Phase error can't be zero, for $\omega_1 \neq \omega_0$.
3) Phase error varries with input frequency.

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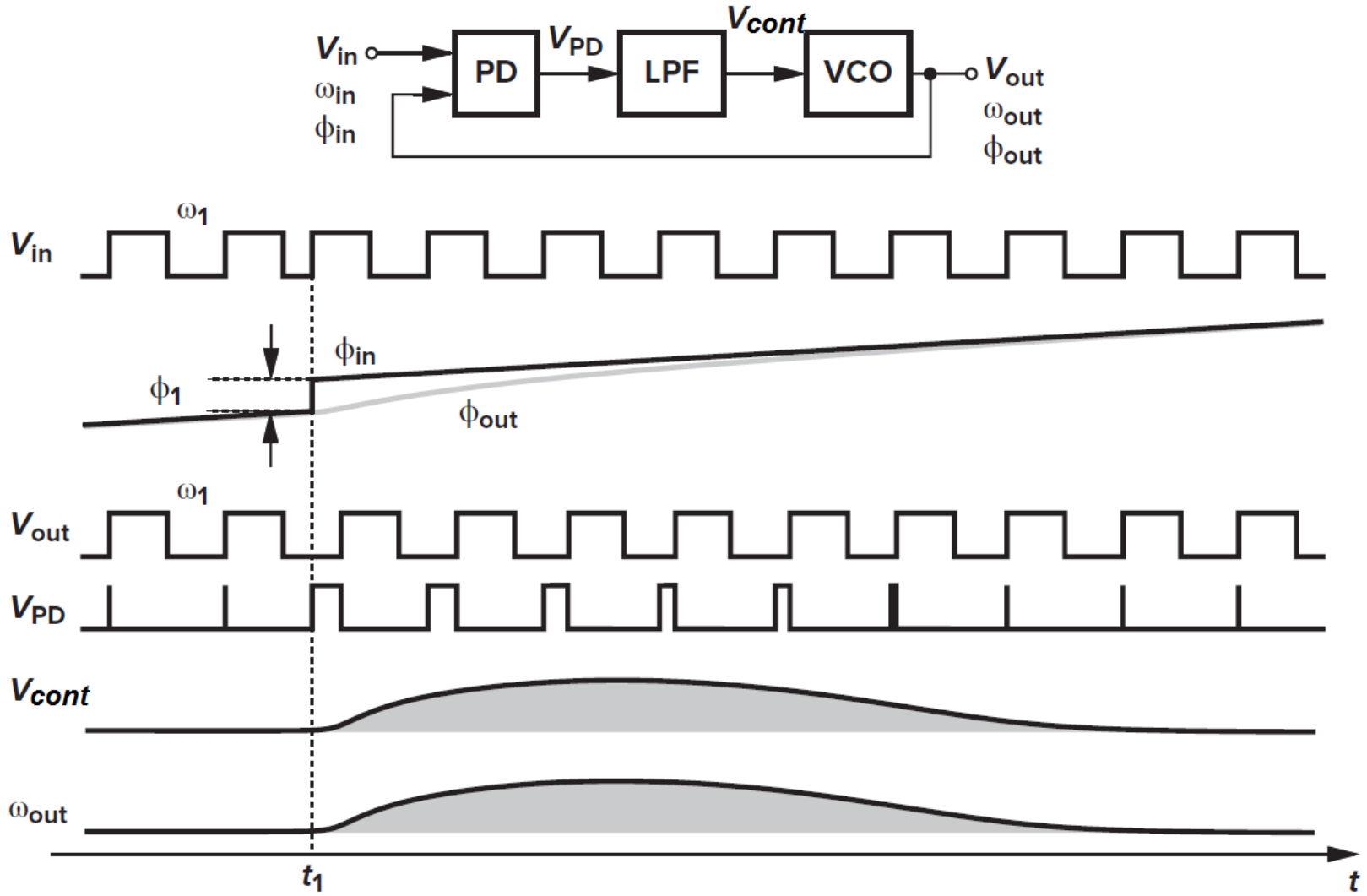
Process of Locking/Capturing

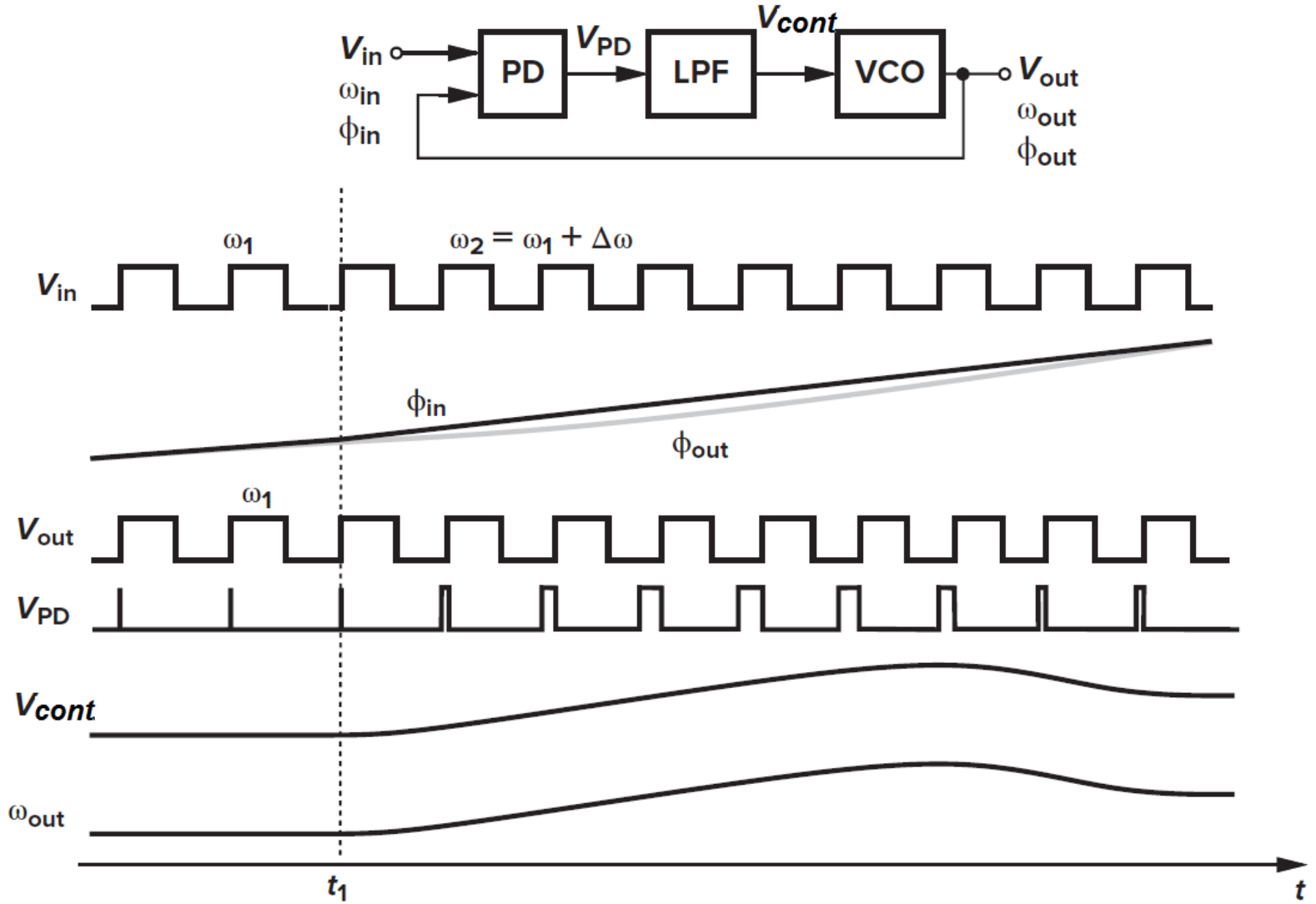
1. When a phase step is given, the phase detector accumulates the phase difference and changes $V_{control}$
2. VCO changes the frequency to vary phase. $\varphi = \int \omega_{out} dt$
3. Once phase error reduces, the input frequency gets equal with output frequency and the loop becomes locked again.



Response of a PLL to a phase step.

Process of Locking/capturing

1. When a small frequency step is given, the phase detector accumulates the phase difference and changes $V_{control}$
2. VCO changes the frequency to vary phase. $\varphi = \int \omega_{out} dt$
3. Once frequency error reduces, the PD produces narrower pulse and V_{cont} settles to a new value to track the new input frequency gets equal with output frequency and the loop becomes locked again.



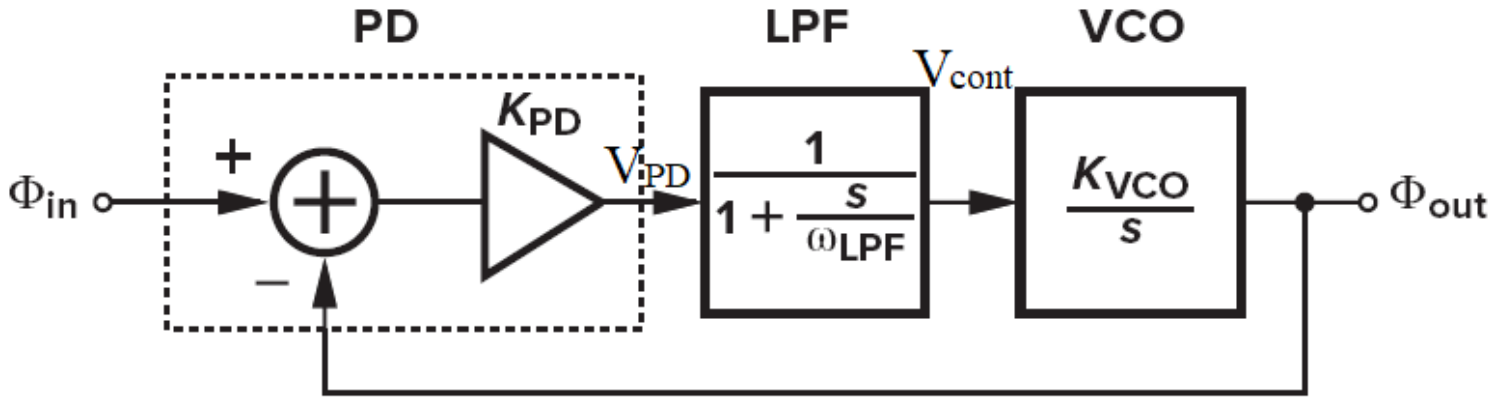
Response of a PLL to a small frequency step.

Dynamics of PLL

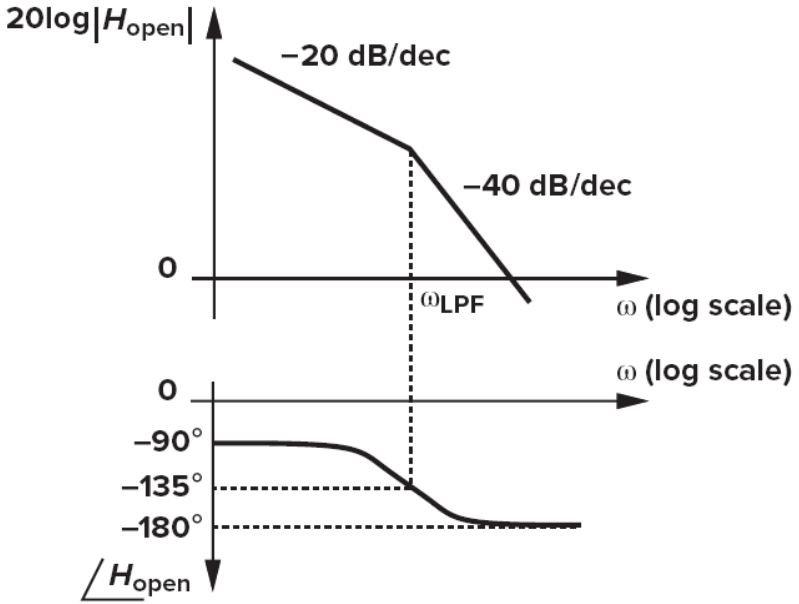
Negative feedback system compares φ_{out} with φ_{in}.

$$H(s)|_{\text{open}} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{\text{open}}$$

$$= K_{PD} \cdot \frac{1}{1 + \frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$



Linear model of type I PLL.



Bode plots of type I PLL.

- To minimise the phase error, K_{PD} and K_{VCO} should be high, but stability degrades.
- Pushing ω_{LPF} to high frequency may improve stability; however, it introduces more ripple in V_{cont} and introduces jitter in ω_{OUT}.
- Since the loop gain contains one pole at origin, it is called Type-1 PLL.

$$\omega = \frac{d\varphi}{dt} \text{ and } \varphi = \int \omega dt$$

$$\Delta\varphi = \frac{\Delta\omega}{s}$$

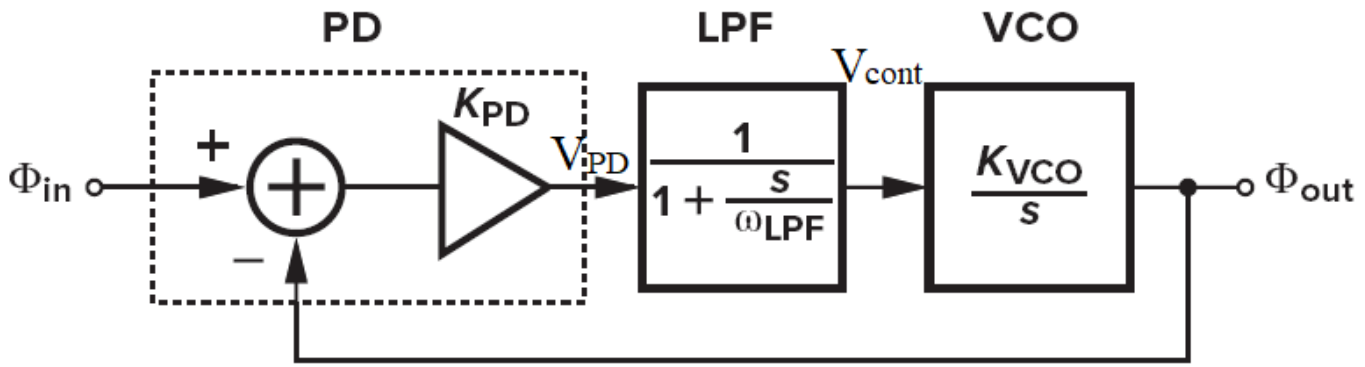
$$K_{VCO} = \frac{\Delta\omega_{out}}{\Delta V_{cont}} = \frac{\Delta\varphi_{out}.s}{\Delta V_{cont}}$$

$$\frac{\Delta\varphi_{out}}{\Delta V_{cont}} = \frac{K_{VCO}}{s}$$

Dynamics of PLL

$$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

$$= \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + s\omega_{LPF} + K_{PD}K_{VCO}\omega_{LPF}}$$



Linear model of type I PLL.

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$$

$$= (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n$$

1. If ω_{in} changes very slowly, s→o, then ω_{out} tracks ω_{in}.
2. If ζ >1. poles are real and overdamped response
3. If ζ <1. poles are complex and underdamped response
4. If ζ =1. critically damped response

Dynamics of PLL

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

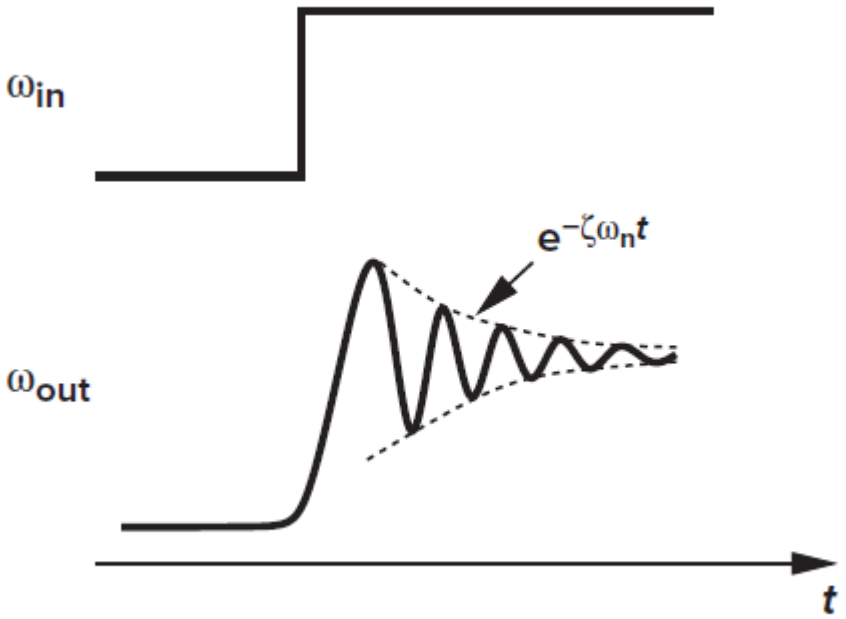
$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}}$$

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2}$$

$$= (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n$$

$$\boxed{\zeta\omega_n = \frac{1}{2}\omega_{LPF}}$$

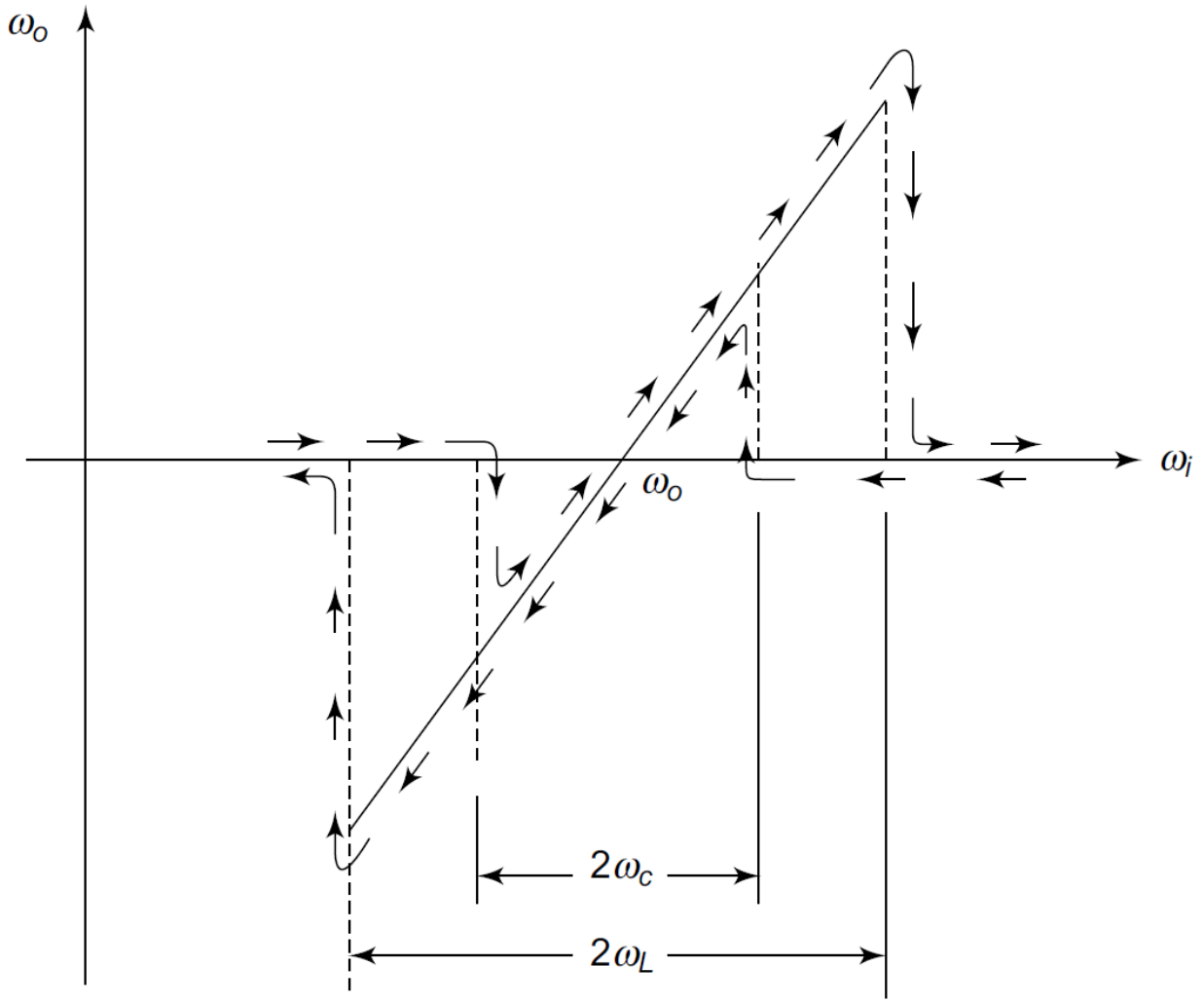


Underdamped response of PLL to a frequency step.

1. Settling speed of PLL is an important parameter. Maximizing ζ·ωn decreases settling time.
2. To maximize $\zeta\cdot\omega_n$, ω_{LPF} has to be increased and it increases ripple of V_{cont}, ω_{OUT} drifts.
3. If $\zeta\cdot\omega_n$ is decreased, PLL takes longer time to settle, a lower value of ω_{LPF} reduces ripple in V_{cont}, but stability decreases.
4. Trade-offs exist between settling time, ripple in V_{cont} and stability.

Lock-range and capture-range of PLL

1. Lock range: When PLL is in locked condition, the lock-range represents the range of frequencies for which the PLL maintains the locked condition.
2. Capture range: When PLL is unlocked condition, the capture-range is the range of input frequencies within which an initially unlocked loop will get locked with an input frequency.
3. Capture range is smaller than lock-range.



Lock and capture processes of PLL

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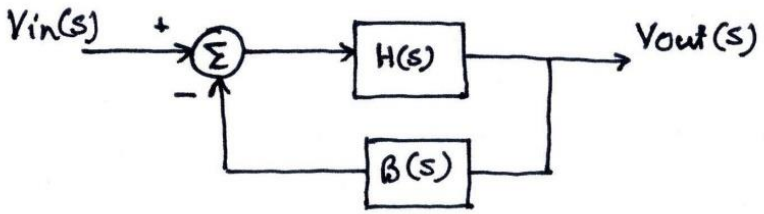
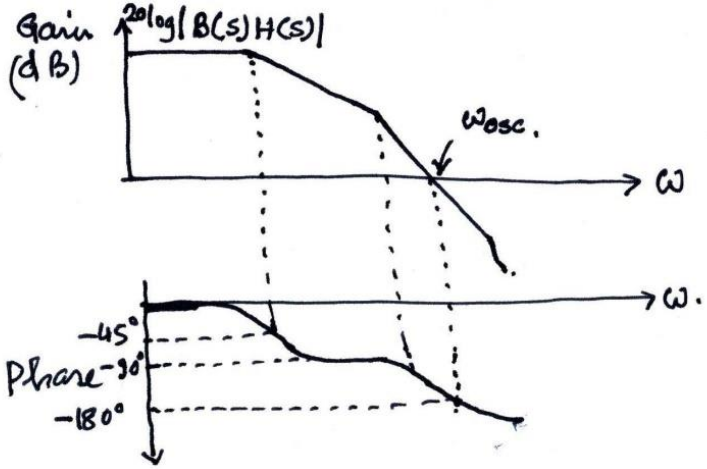
Oscillator

An oscillator is a BADLY designed negative feedback amplifier.



$$\left.\frac{V_{out}}{V_{in}}(s)\right|_{Closed} = \frac{H(s)}{1+\beta(s)H(s)}$$



If for $s = j\omega_{osc}$,

$$\beta(j\omega_{osc})H(j\omega_{osc}) = -1,$$

then $\frac{V_{out}}{V_{in}}(s) = \infty$.

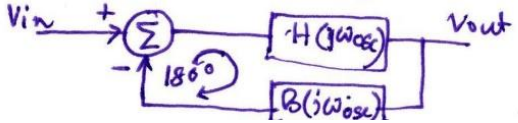
To get a sustained oscillation, the loop gain should be slightly greater than unity

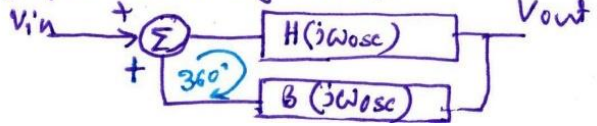
A negative feedback system will oscillate, if $|H(j\omega_{osc})\beta(j\omega_{osc})| \geq 1$.

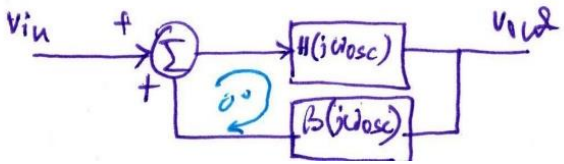
$$\angle H(j\omega_{osc})\beta(j\omega_{osc}) = 180°$$

This is called as "Barkhausen Criteria".

- This conditions are necessary but not sufficient.
- To get a sustained oscillation across PVT variation, the loop gain should be at least twice or thrice.
- Different views of oscillatory feedback system:-

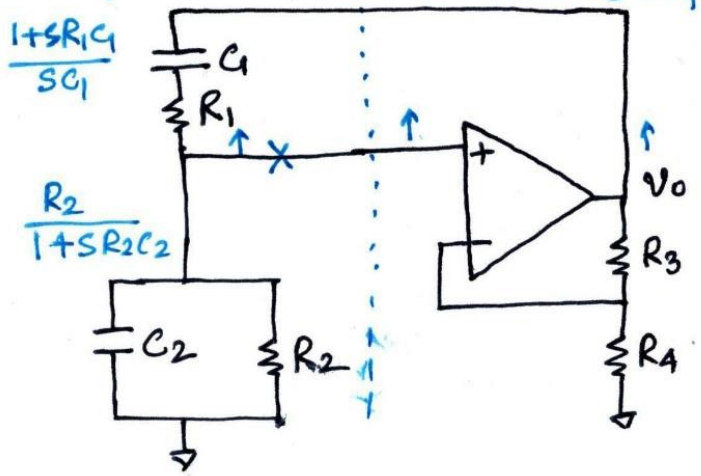






Wein Bridge Oscillator :- produce a sinusoidal waveform.

feedback network : non-inverting amp.



$$\text{Loop gain} = \left(1+\frac{R_3}{R_4}\right)\frac{R_2/(1+sC_2R_2)}{\frac{R_2}{1+sC_2R_2}+\frac{1+sR_1C_1}{sC_1}}$$

Assuming $R_1 = R_2 = R$, $C_1 = C_2 = C$.

$$= \left(1+\frac{R_3}{R_4}\right)\frac{R/(1+sRC)}{\frac{R}{1+sRC}+\frac{1+sRC}{sC}}$$

$$= \left(1+\frac{R_3}{R_4}\right)\frac{1}{3+sRC+\frac{1}{sRC}}$$

To get a sustained oscillation, the phase-shift across the loop should be $0°$, or $360°$.

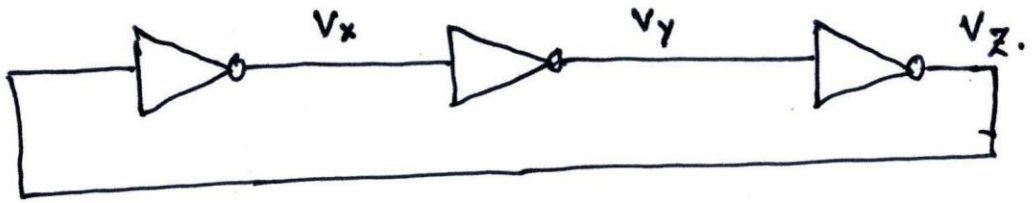
$$sRC = -\frac{1}{sRC} \Rightarrow s^2 = -\frac{1}{RC} \Rightarrow \omega_{osc} = \frac{1}{RC} \Rightarrow \boxed{f_{osc} = \frac{1}{2\pi RC}}$$

To meet the gain criteria, $\left(1+\frac{R_3}{R_4}\right)\frac{1}{3} = 1. \Rightarrow \boxed{R_3 = 2R_4}$

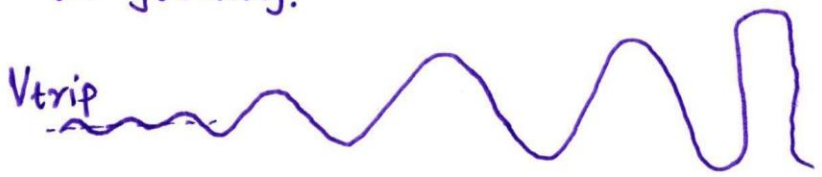
Note :-
- At very low frequency, the feedback loop is broken, not a positive feedback system.
- At ω_{osc}, it only becomes a positive feedback system.
- There is no input to the ckt. How do we get o/p.?

Ring Oscillator :-

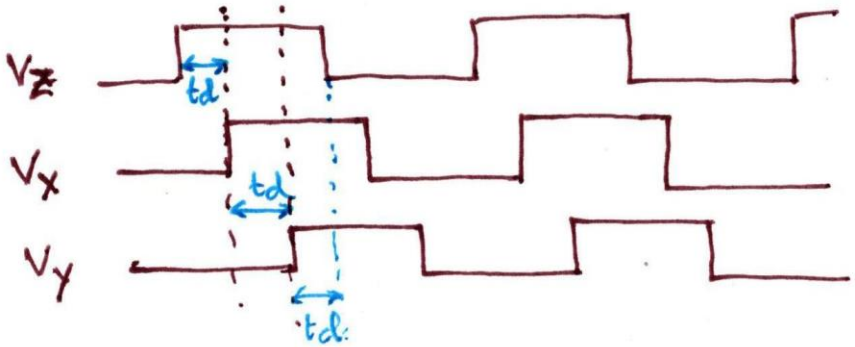
Connect odd number of inverters in the ring.



* If there is no noise, then
  $V_x = V_y = V_z = V_{trip}$.
  no oscillation.
* With noise, this state will be disturbed and oscillation will be growing.



Steady state response.



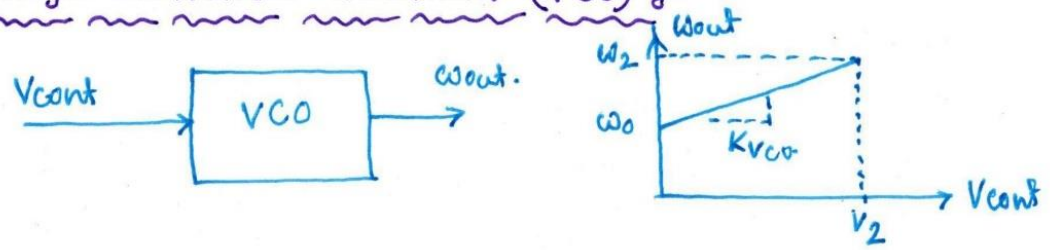
t_d is the delay of inverter.

Frequency of oscillation $f_{osc} = \frac{1}{6\,t_d}$.

For N no. of inverters, $f_{osc} = \frac{1}{2N\,t_d}$ where N = odd no.

How we can develop VCO from this ?

Voltage Controlled Oscillator (VCO) :-



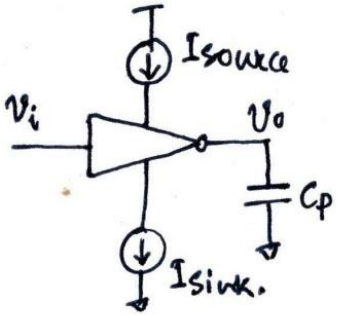
$\omega_{out} = \omega_0 + K_{VCO} \cdot V_{cont}$.

$K_{VCO} = \dfrac{\omega_{out} - \omega_0}{V_{cont}}$.

$(\omega_2 - \omega_0)$ → linear tuning range.

Implementation of VCO :-

A current-starved inverter delay is controlled by the bias current.



Inverter trip voltage = V_{trip}.

1) when V_o is charging from low-to-high, the next stage will trip from high-to-low, once the V_o reaches V_{trip}.

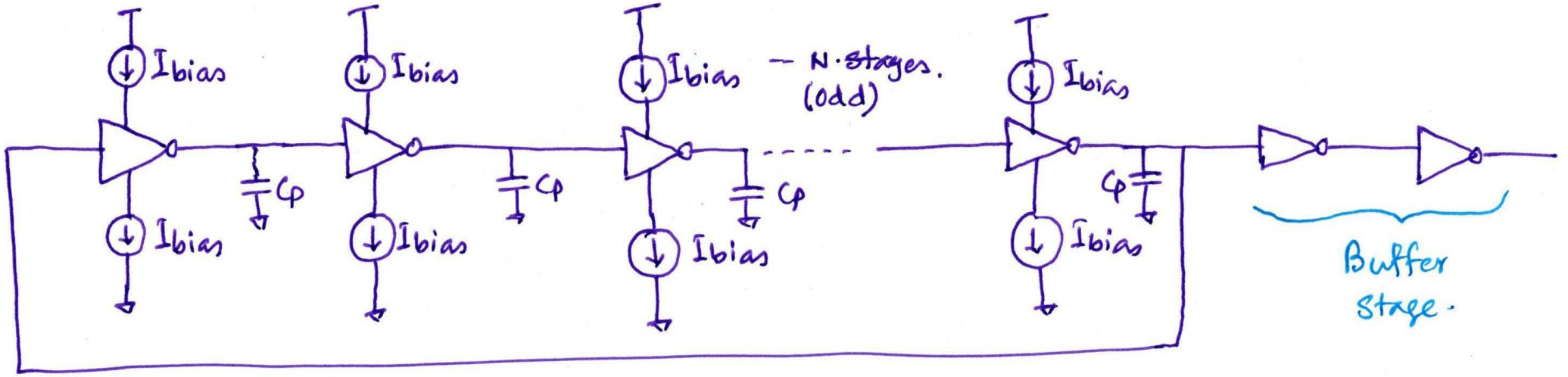
$$t_{PLH} = \frac{C_p \times V_{trip}}{I_{source}}$$

2) Similarly, when V_o is discharging from high-to-low, the next stage will trip from low-to-high, once V_o reaches to $(V_{DD} - V_{trip})$ from V_{DD}.

$$t_{PHL} = \frac{C_p \times (V_{DD} - V_{trip})}{I_{sink}}$$

If $I_{source} = I_{sink} = I_{bias}$, then $t_p = \dfrac{t_{PHL} + t_{PLH}}{2} = \dfrac{C_p V_{DD}}{2 I_{bias}}$

If $I_{bias} = f(V_{control})$, then $t_p = f(V_{control})$



Frequency of oscillation $f_{osc} = \frac{1}{2N.t_p} = \frac{I_{bias}}{\frac{1}{2} N C_\phi V_{DD}}$

Ibias can be generated from a voltage-to-current converter.