Pratyush Jaiswal 18EE30021

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1.	Logic levels:	
	In dealed exercite a liver land or mand	
	I but winher of class if the desired	
	In digital Ascuits, a logic level is one of a finite number of states that a digital signal can inhabit.	5
	Types of Care livelie	
	Types of logic levels:	
	2- level logic: In binary logge the two levels one	6
	logical high and logical low- which generally	E,
	corouspond to bringry numbers 1 to respectively.	6
	2-level logic: In binary logic the two levels are logical high and logical low; which generally correspond to binary numbers 1 to respectively. Signals with one of these two levels can be med in hadron alarters love decided about it	ART
	Ged en boslion algebra for digital cercuit	-
	design or analysis.	T
		6
	Leneury Signal Representations. Logic level Active-Bigh Active-bond	4
	Logic level Active - Figh Active - bons	
	logic low 0 1	
		5
	3- level logic:	-
and the later apply for the second	In three-state logic, an ordfut dovice can be. In one of the three possible states = 0,1 f Z. with the last meaning high implance.	-
	in one of the flore possible status . 0,1 + Z	
	1/0 0. 1 / ast meaning high implance.	
The Principle of the Street	This is not a logic level, but means that the	
erco-servorinajo dinositik	output is not controlling the state of the connected circuit.	
	Louvelle ayear.	
		10
		-

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4-livel logic adds a fornith state, (x) - don't come, meaning the value of the signed is unsuportant tundefined. It means that an input is undefined, or an output signal may be hosen for implementation convenience (k map, don't came) g-lend byic: IEEE 1164 defines 9 logic states for use in electronic design automation which includes strong and weakly driven signals, high impedance fundaments and withalised states. Amulti-level logic:
A multi-level all stores data using multiple voltages. Types of Standard digital serial communications6. Synchronous Communications= Asynchronous communications & the standard neans of serial data communication for PC compatibles and PS/2 computers. Serial data communications Emplies that indevidual bits of a character are transmitted consecutively to a receiver and that assembles the bits back juto a character. Sevial asynchronous communications is prically Puplemented with a Recommended Standburd (B).

	Date:/ Page:
Syntronous Communications:	
This type of communication is	used An
applications that require higher data	rates 4
greeter exist dicting mountings.	1 Variatel
guerora sawar and not duration	ane hemself
Than asynchronous commu	mications.
Bit divation in Eynelwonous comm	to the
is not necessarily modelined	both the
Toursmilling and societing enels.	- Total
Electrical, Standowds &	
Electrical, Standowds &	
RS-232:	-
General and I be nost widely sised	communication
Jonie of JI-252. The most com	mon
implementation of RF-282 is on a	standard
s pur & sub connector althory .	TOM DE
computer. CS-222 is capable of opera	tiny at
Cata votes upto 20 apps 5aft.	
RS-422=	
This specification is defined the electronistics of bolanced voltage dig Circuity.	trical
Characteristics of balanced voltage dig	ital interface
Greath.	
RJ-423:	
Ho 2011 to	
This specification defines the electrical of unbalanced voltage digetal int	characteristis
of unsarenced us teage digetel int	erfan cht.
· V	

RS 449, BS 485, PS-530 Current loop: This specification is based on the absence of presence of currents, not voltage lands, over to communication line There are major fine major types of ADIs En use todays. Succession Approximation (SAR) ADC: It offers an excellent balance of speed and resorbition and handles a wide variety of signals with excellent fidelity. They can be configured for both low-end A/D cards, where a rignal ADCo chip is shared by multiple channels [multiplexed A/D boards), Ir in configurations where each Enjut channel has Its own ADC for frue comultaneous Sampling. Delta - Hyma (22) ADC: A newer disign is Alta - Sigma ADC, which takes advantages of DIP technology & or order to Purprove the ampletude axis resolution and veduce the high frequency quantization noin Infrerent in SAK cleriques.

Dual Slope AD convertes: These are accurate but not tessibly fast. The premipal ivery they correct analog of digital Values in hy using an lantegration. The vo Hage is Propert and allowed to "run up" for a period of time. Then a brown voltage of the opposite polarity is applied and allowed to run back down to zero. When it reaches zero, The System calculates short the gripert No Haye hard been by comparing the run lip time with run down Applied ADC. In this, the analog signed is not latched by all comparators at the same time, spreading analog & a digital value This has the high herefit of allowing higher resolutions he achieved without high energy. Flash pacs are fast & operate vistually without lateray, Aich is why they are the architecture of choice when the highest possible sample vates core needed. They convert analog to a digital signal by companing it with known references. The mon known references are und, the more accuracy is achieved.



