

# Lect 2

# Where From Have the Performance Improvements Come?

- **Technology**

- More transistors per chip
- Faster logic

- **Processor Organization**

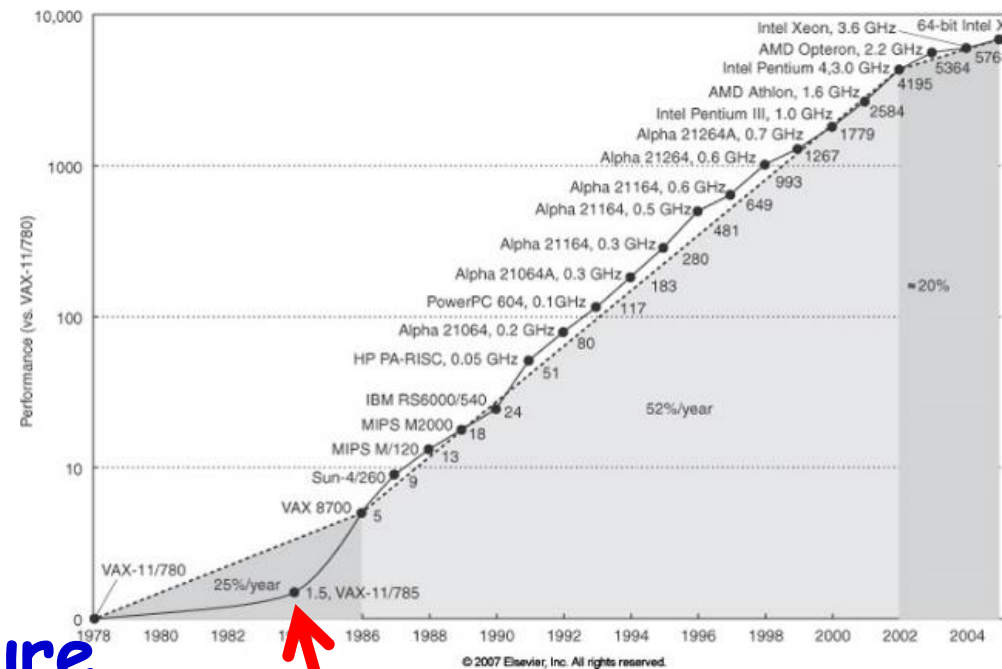
- Effective and deep pipelines
- Parallel execution units

- **Instruction Set Architecture**

- Reduced Instruction Set Computers (RISC)
- Multimedia extensions
- Explicit parallelism

- **Compiler technology**

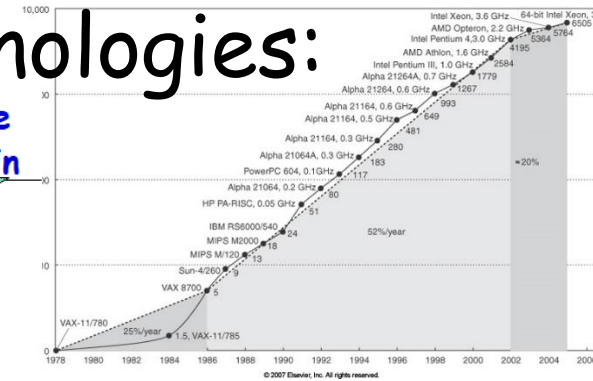
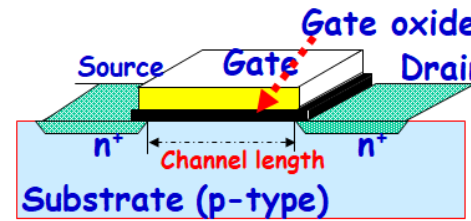
- Finding more parallelism in code
- Greater levels of optimization



# How Did Processor Performance Improve?

- Till 1980s, most performance improvements came from innovative manufacturing technologies:

- VLSI
- Reduction in feature size



- Improvements due to innovating manufacturing technologies have slowed down since 1980s:

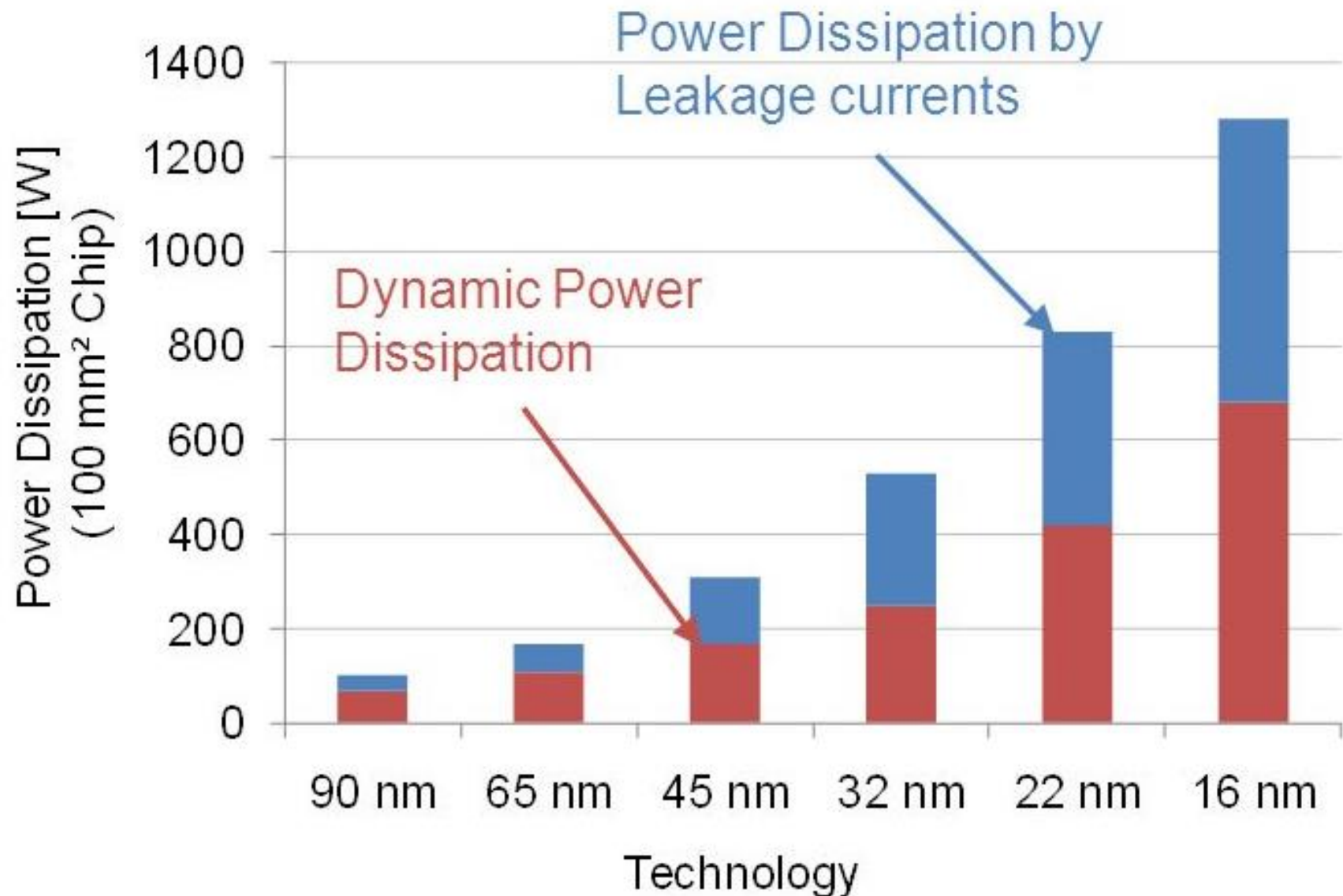
- Smaller feature size gives rise to increased resistance, capacitance, propagation delays **and leakage**.
- Larger power dissipation.



What is the power consumption of core i7 processor?

Roughly 100 watts when in use and 40 watts idle...

# IC Power Consumption Trends



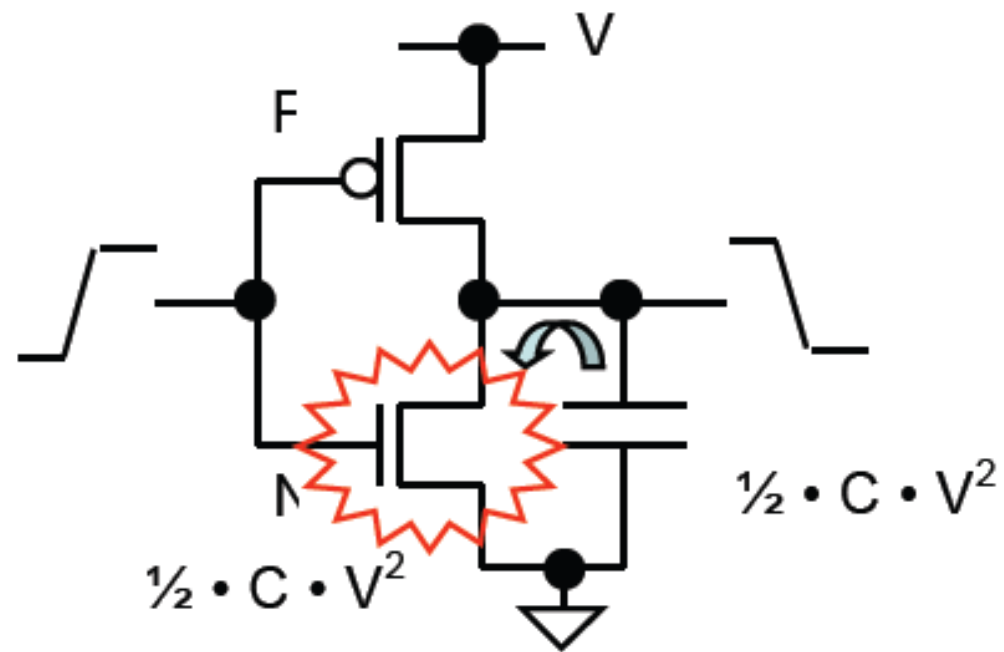
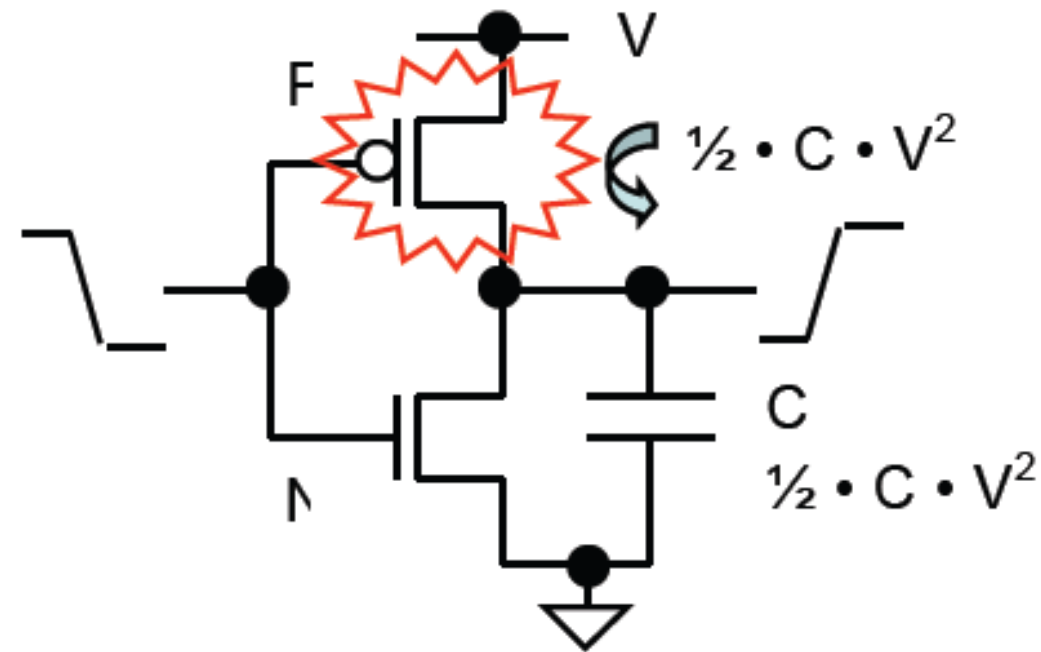
# Power Consumption in a Processor

- Power = Dynamic power + Leakage power
- Dynamic power = Number of transistors x capacitance x voltage<sup>2</sup> x frequency
- Leakage power is rising and will soon match dynamic power.

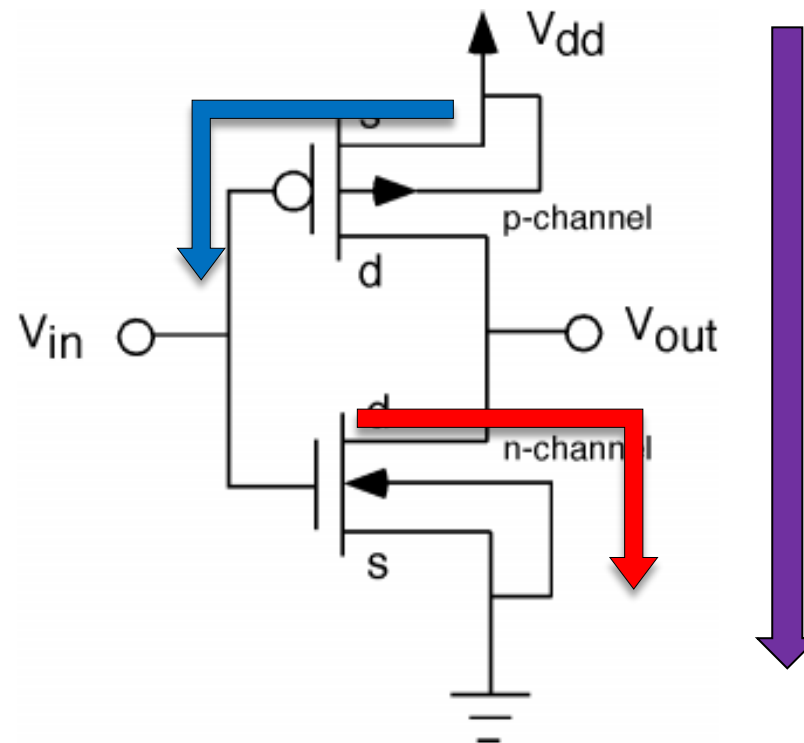
	Pentium	P-Pro	P-II	P-III	P-4
Year	1993	95	97	99	2000
Transistors	3.1M	5.5M	7.5M	9.5M	42M
Clock Speed	60M	200M	300M	500M	1.5G

# Switching Power

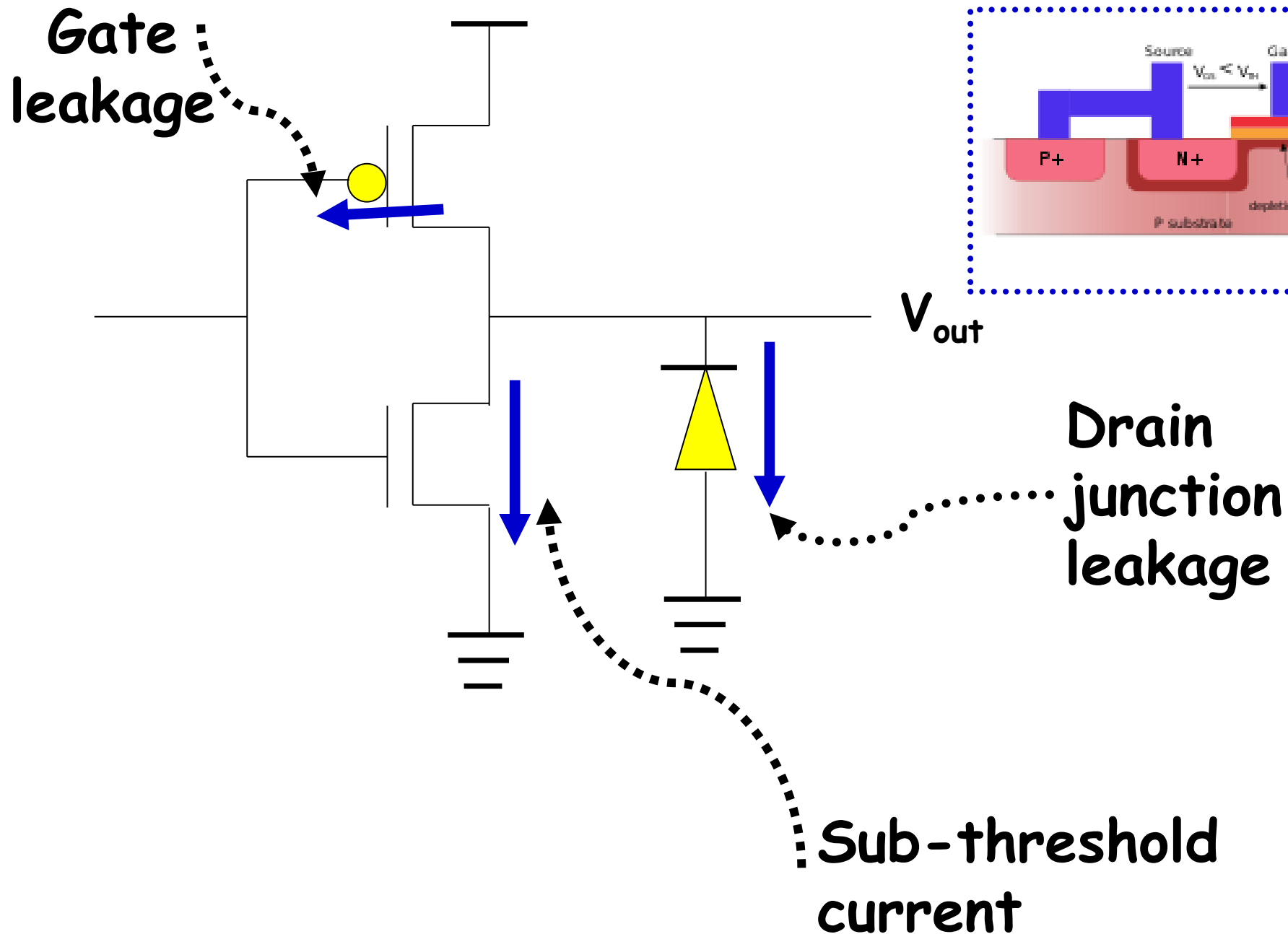
$$P = a \cdot C \cdot V^2 \cdot f$$



# Static power

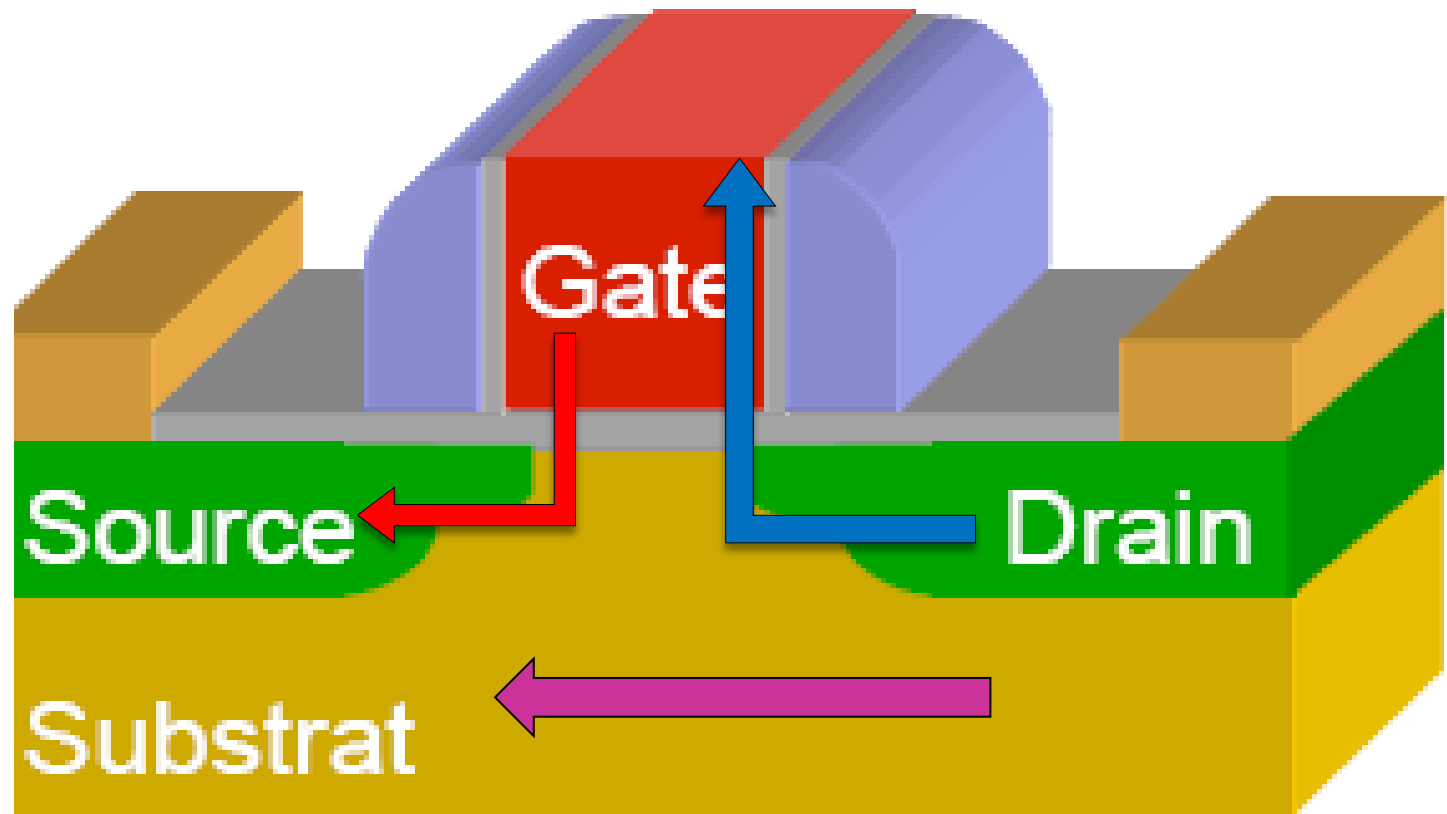


# Static Power



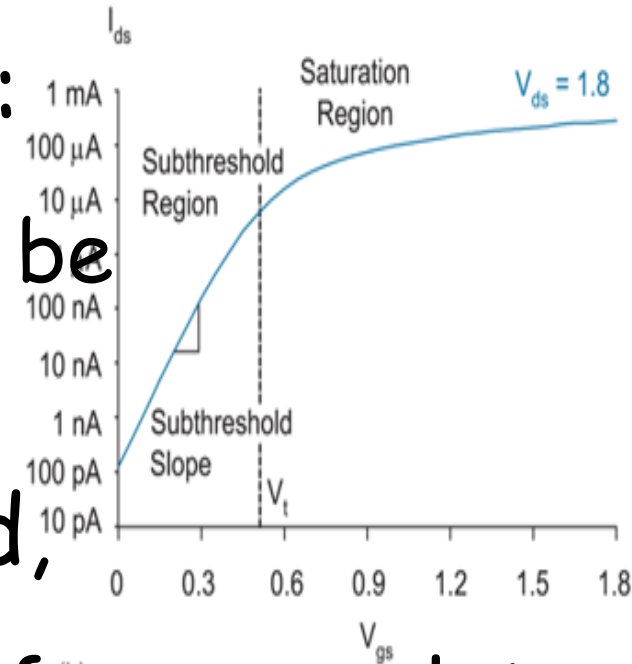


# Leakage Currents



# Sub-threshold Leakage

- As MOSFET geometries shrink:
  - Voltage applied to the gate must be reduced to maintain reliability.
- As threshold voltage is reduced,
  - A transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available;
  - Strong current is the "on" state and low current is the "off" state.
  - Subthreshold operation...

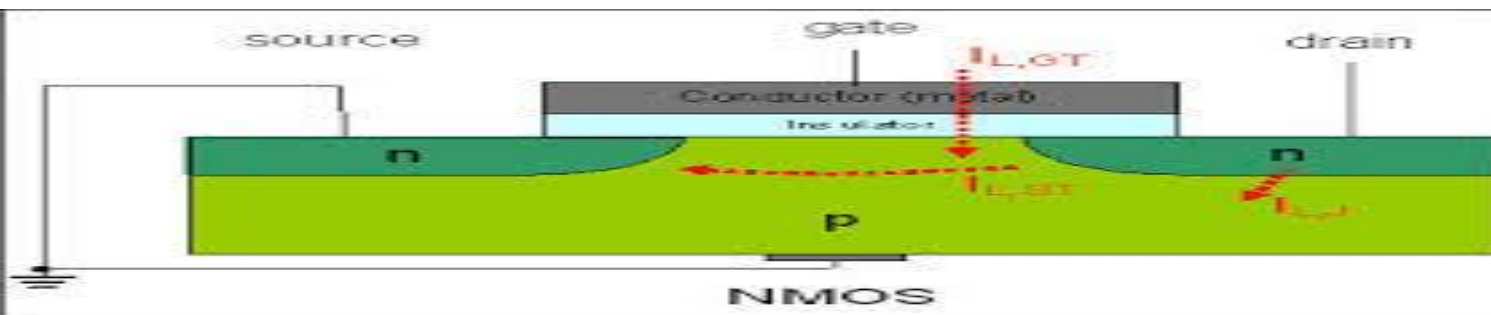


# Gate Leakage: junction leakage and tunneling

**Junction leakage:** A reverse-biased p-n junction has some leakage.

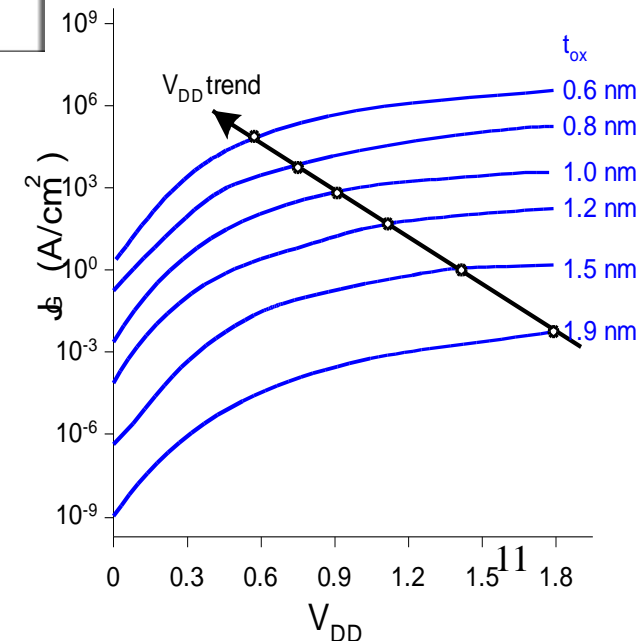
$I_s$  depends on doping levels and area and perimeter of diffusion regions

$$I_D = I_s \left( e^{\frac{V_D}{V_T}} - 1 \right)$$



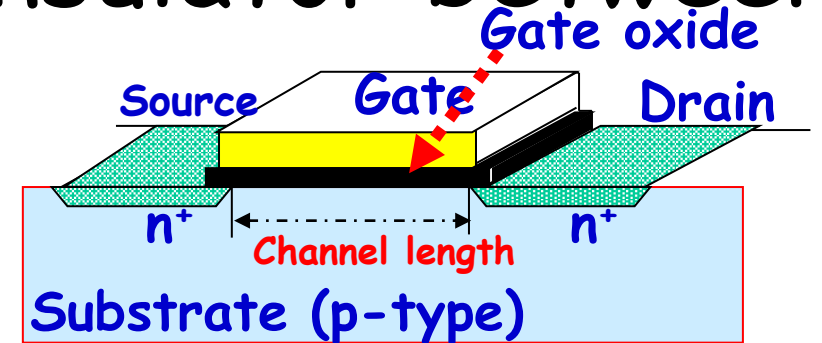
## Tunneling leakage:

- Carriers may tunnel through very thin gate oxides
- Negligible for older processes



# Tunnelling Leakage

- Gate oxide serves as insulator between the gate and channel.



- However, gate oxide now has thickness of around 1.2 nm ( about 5 atoms thick):
  - Quantum mechanical phenomenon of electron tunneling occurs between gate and channel.

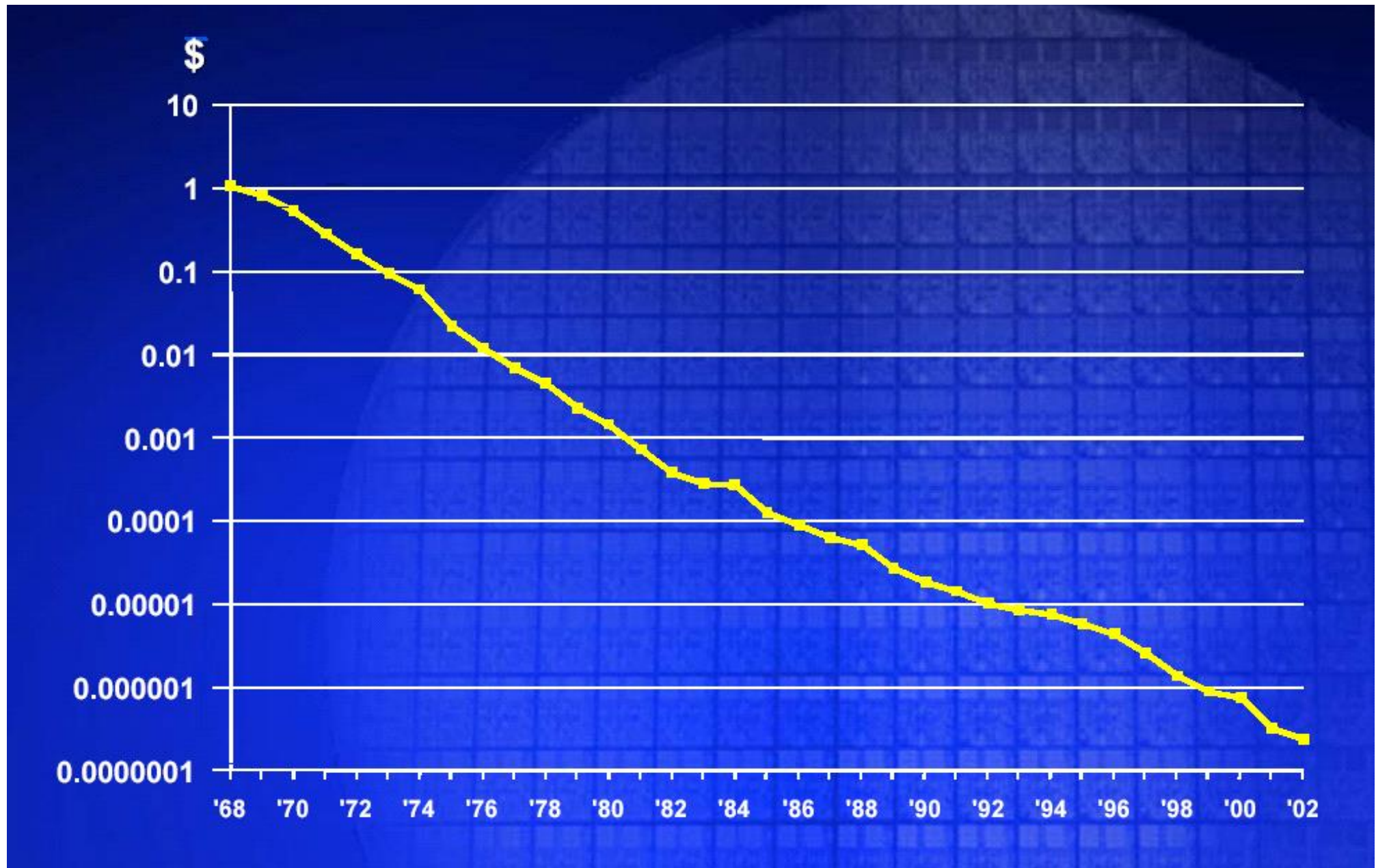
# Dynamic Power


$$P_{dyn} \approx \sum_i C_i V^2 A_i f$$

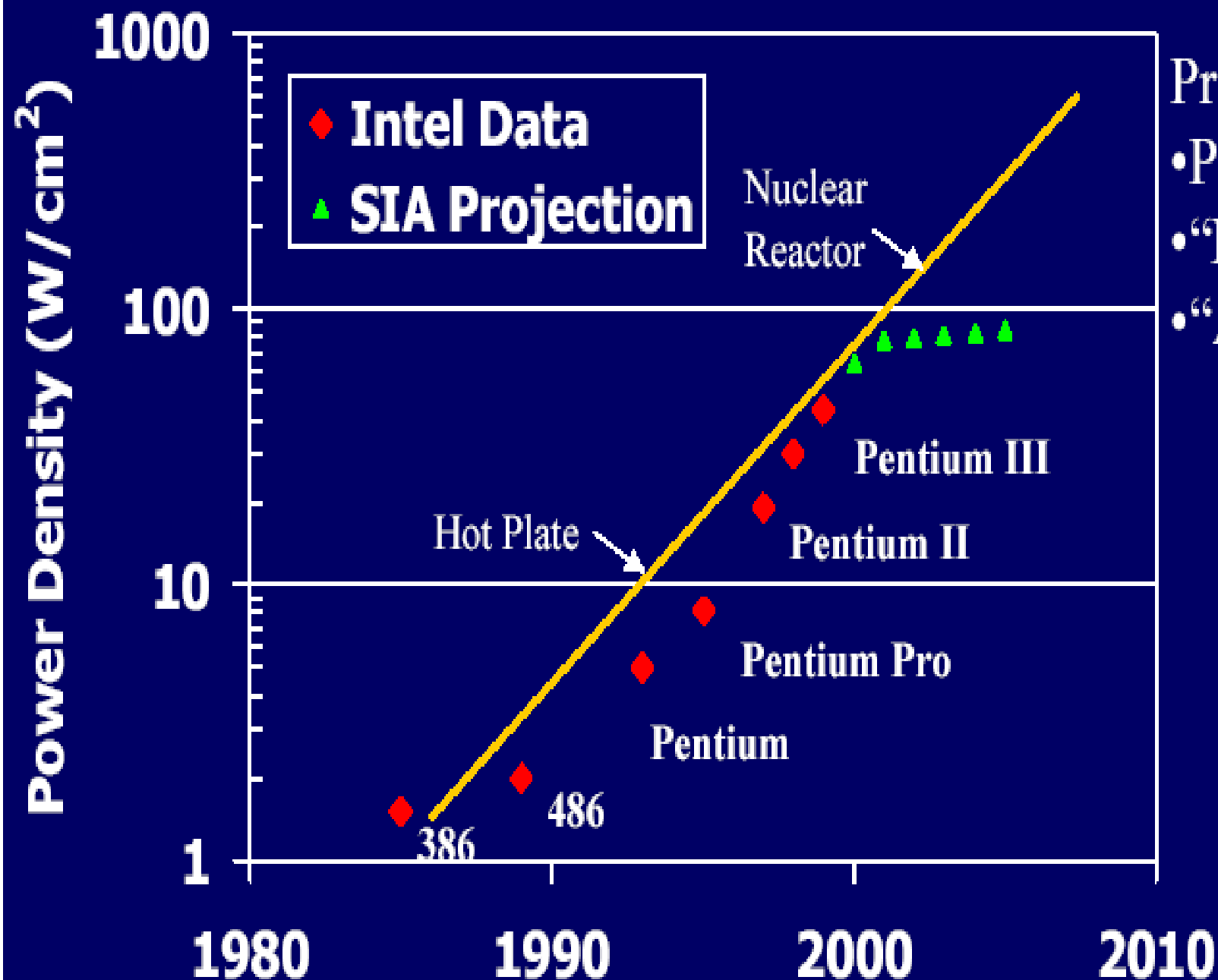
The diagram shows the equation  $P_{dyn} \approx \sum_i C_i V^2 A_i f$  with four colored arrows pointing to the terms: a blue arrow pointing up to  $C_i$ , a purple arrow pointing down to  $V^2$ , a green arrow pointing down to  $A_i$ , and a red arrow pointing down to  $f$ . Below the equation, the text *units* is written.

- **Dynamic power in CMOS** : Due to a transistor switching on and off
- **Terms**
  - $C$ : capacitance of circuit
    - wire length, number and size of transistors
  - $V$ : supply voltage
  - $A$ : activity factor
  - $f$ : frequency
- **Future: Power dissipation a major factor**

# Average Transistor Cost Per Year



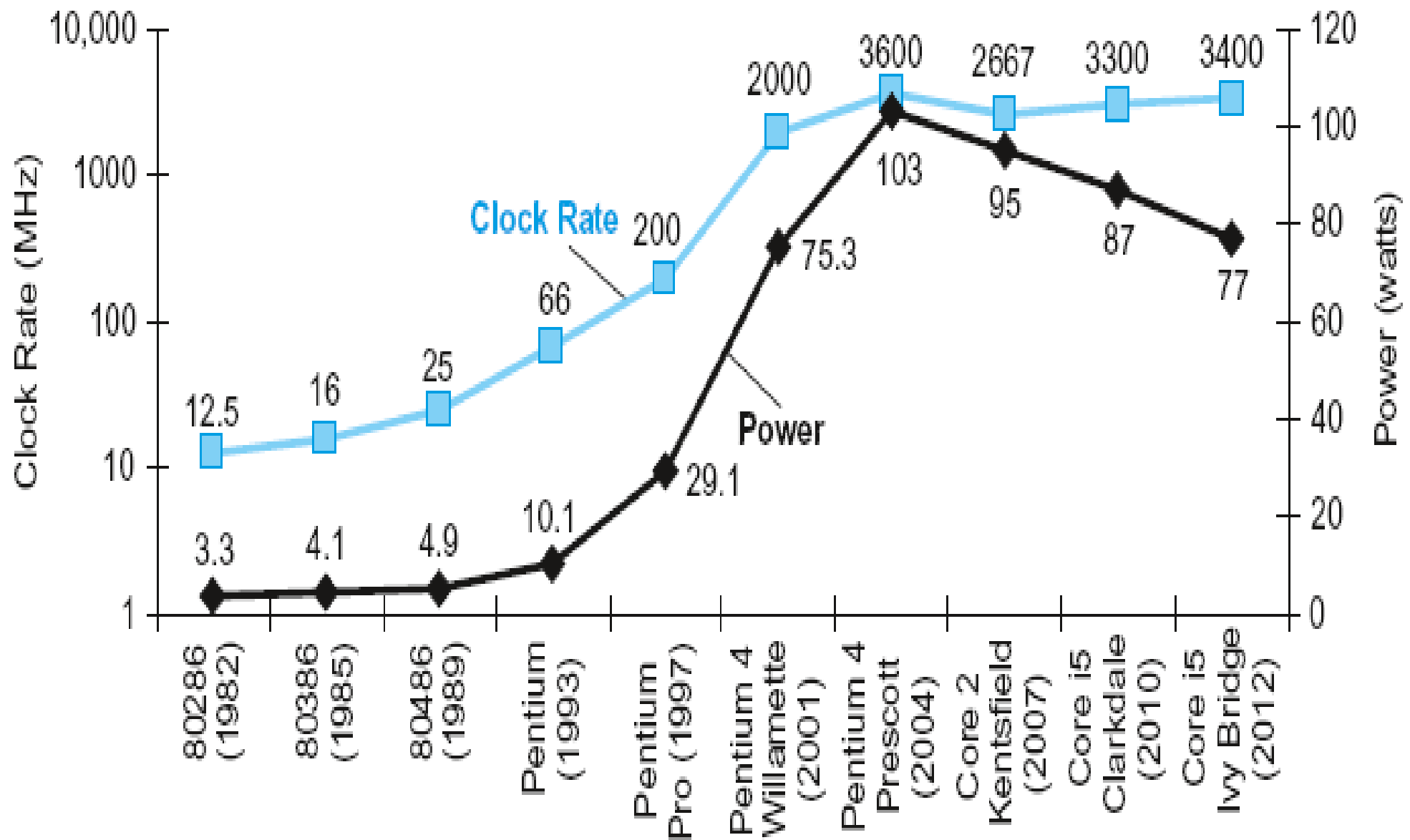
# Power Density Trend



Problems:

- Power Delivery
- “Max” Power
- “Avg” Power

# CMOS IC Power Trends





# Watch This...

