Pratyush Jaiswal
18EE30021

```
.INCLUDE    "M32DEF.INC"

.ORG   0x00

   .EQU   PA = R18
   .EQU   PB = R19
   .EQU   PC = R20
   .EQU   PD = R21
   .EQU   CCTR = R22
   .EQU   RCTR = R23.


INIT:
      LDI   R31, HIGH (200)   # SRAM location
                               containing image data

      LDI   R30, LOW (200)  # Data arranged
                               where image resides

      RET


# INPUTS & OUTPUTS
      LDI   R16, 0xFF      # Setting ports high
      OUT   DDRA, R16      #PORTA serves as address
                            line for 8255 to select
                            PORT
      OUT   DDRB, R16      # PORTB: serves as
                            data line to 8255
      OUT   DDRC, R16      # PORTD: serves as
                            write enable for
                            8255.
```

MAIN

```
MAIN:
    R1:    SBI  PORTA, 0
           LDI  PA, 0
           LOOP:
                   LDI   CCTR, 3
                   INC PA
                   OUT  PORTA, PA
                   LOOP1:
                           LDI  RCTR, 32
                           LD   PB, Z+
                           OUT  PORTB, PB.
                           DEC  RCTR
                   BRNE LOOP1
                   DEC CCTR
           BRNE LOOP.
    R2:
           SBI PORTD, 0
           CBI PORTA, 1
           LDI  PA, 0
           LOOP:  LDI CCTR, 3.
                  INC  PA
                  OUT  PORTA, PA
                  LOOP1: LDI RCTR, 32
                         LD   PB, Z+
                         OUT  PORTB, PB
                         DEC  RCTR
                  BRNE LOOP1
```

```
DEC CCTR
BRNE LOOP
RJMP  MAIN
```