Nethavath Praveen

Undergraduate Student at IIIT Hyderabad

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Education

International Institute of Information Technology, Hyderabad (IIIT-H) **Aug 2023 – Jul 2027**
B.Tech in Electronics and Communication Engineering (ECE) *Current CGPA: 6.25*

Jawahar Navodaya Vidyalaya (JNV) **Jun 2021 – Jul 2023**
Senior Secondary (CBSE) – Class XII, Percentage: 93.6% *Puducherry, India*

Jawahar Navodaya Vidyalaya (JNV) **Up to May 2021**
Secondary School (CBSE) – Class X, Percentage: 95% *Warangal, Telangana*

Relevant Coursework

Data Structures and Algorithms | C Programming | Digital Systems and Microcontrollers | VLSI Design | Intro to Processor Architecture | Signal Processing | Analog Electronic Circuits | Communication Theory | Mechatronics System Design | Real Analysis | Linear Algebra | Networks, Signals and Systems|Probability and Random Processes

Projects

AI-Enhanced Buy-Sell Marketplace | *MERN Stack, Hugging Face, FAISS, JWT, OTP Authentication* **March 2025 - Present**

- Built a MERN-based marketplace with OTP authentication for secure buying and selling.
- Implemented JWT authentication and product management for registered users.
- Integrating AI-driven product search using Hugging Face and FAISS for better discovery.

AI-Powered News Research Assistant | *Python, LangChain, FAISS, Hugging Face, Streamlit* **Feb 2025**

- Developed an AI-powered research tool using LangChain and Hugging Face to extract and analyze news articles. Implemented FAISS-based search and an LLM for contextual answers with source attribution.

Advanced C-Shell | *C, POSIX* **December 2024**

- Developed a custom shell (CLI) in C with features including command execution, I/O redirection, piping, process management, custom commands, and networking functions. Implemented signal handling, and a history mechanism.

Network File System | *C, POSIX, Socket API, DSA* **December 2024**

- Designed and implemented an Distributed File System using Socket Programming. Key features include file operations (CRUD), copy / move, concurrent client access, LRU caching, data redundancy, and replication.

Processor Architecture | *Verilog* **January 2025**

- Developed a 5-stage Pipelined processor architecture design based on the RISC-V ISA using Verilog. The design also includes the data hazards and control hazard specification.

FOUR BIT CLA | *Ngspice,Verilog,Magic* **November 2024**

- Designed and analyzed a 4-bit Carry Lookahead Adder (CLA) using Dynamic CMOS, CPL, and traditional CMOS technologies. Evaluated performance in terms of speed, power consumption, and area efficiency for high-performance digital systems.

Technical Skills

Languages: JavaScript, Python, C, C++, HTML/CSS, SQL,Ngspice ,Verilog
Developer Tools: VSCode, Postman,Canva, Git, Manim , Matlab, LaTeX
Technologies/Frameworks: Linux, GitHub, React.js, Express,Arduino,Mongodb,Langchain,FAISS,Streamlit,Magic

Achievements / Extracurricular

- Secured All India Rank of 2107,3894 in JEE Mains ,JEE Advanced respectively .
- secured rank 180 out of 2.5 lakh in TS-EAMCET (2023)
- Participated in Athletics National level in my secondary school)
- A certificate in National cadet corps

National Service Scheme **Spring 2025 – Present**
Co-ordinator *IIIT Hyderabad*

Felicity **Spring 2025 – Present**
Member of Marketing Team *IIIT Hyderabad*