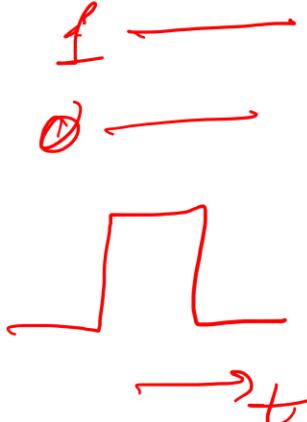
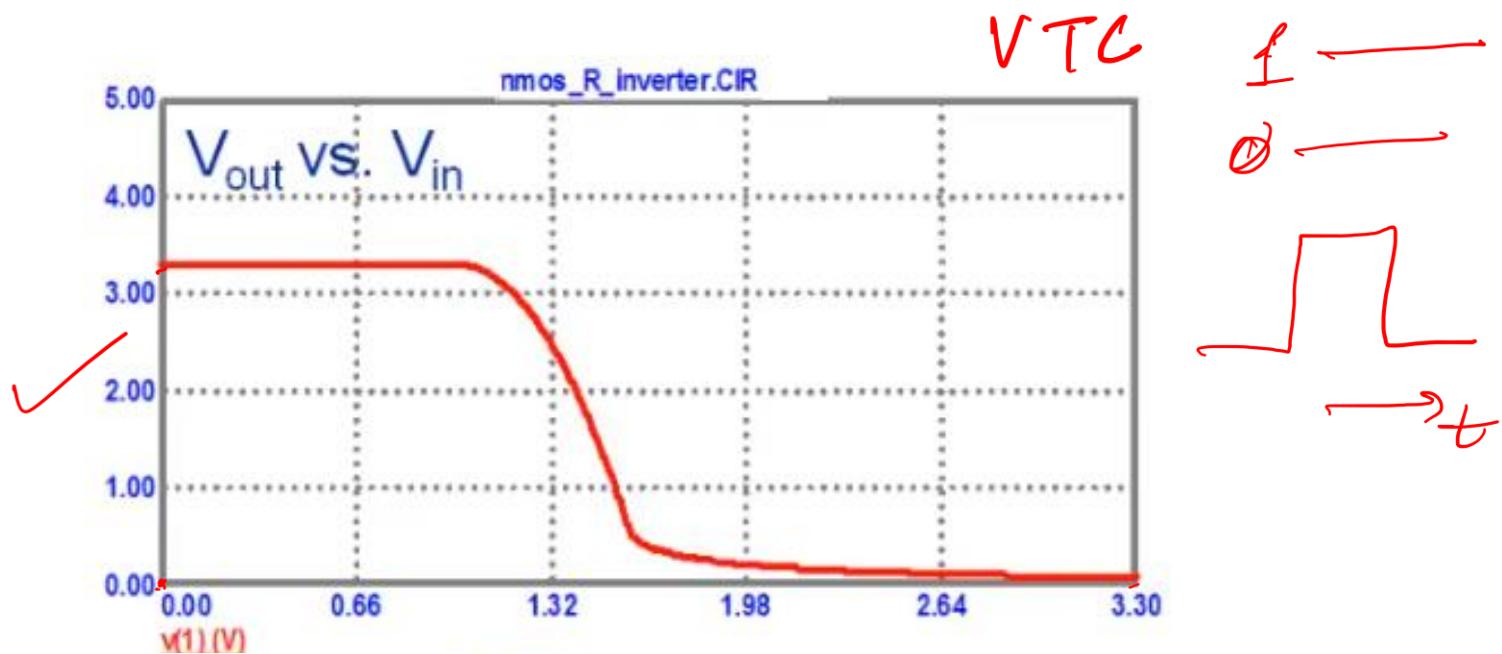
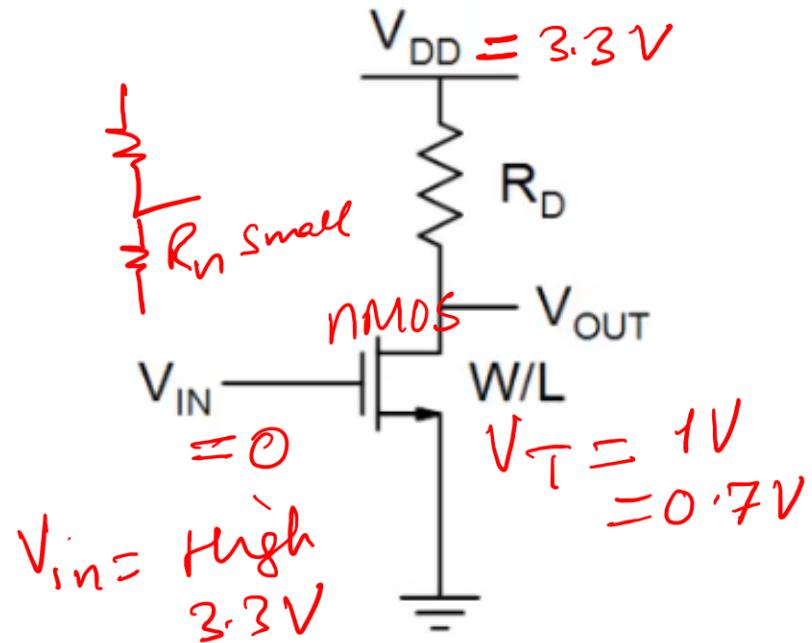


Circuit Design

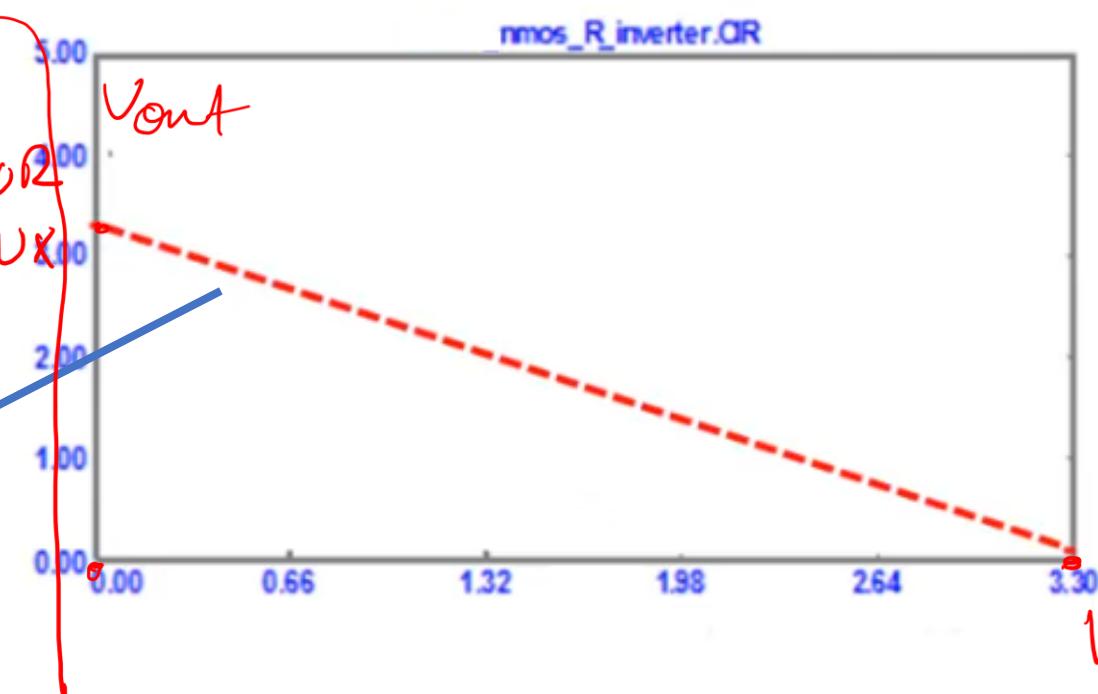
Inverter with Resistive Load



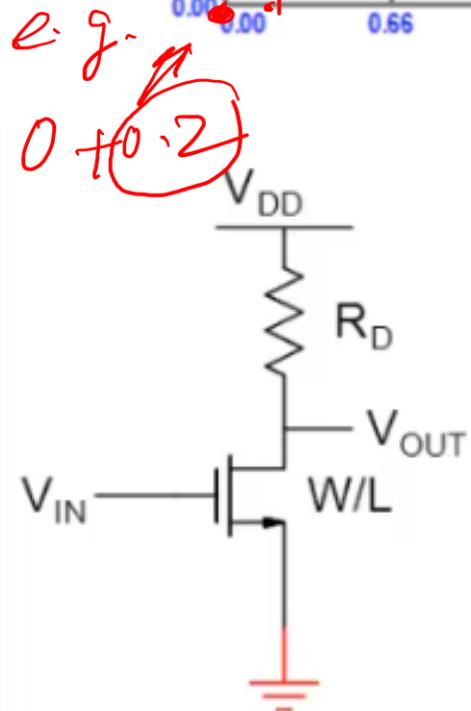
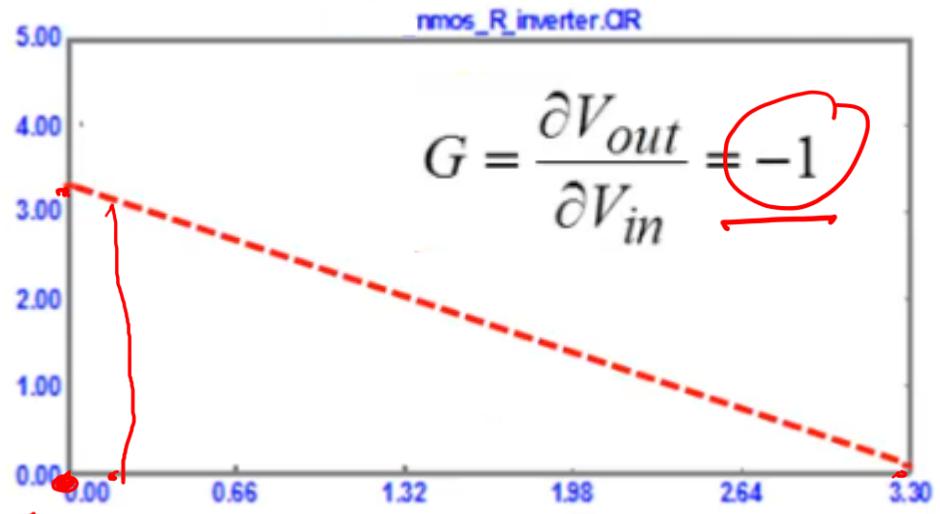
Q. Functionality

1. Area \rightarrow INV, NAND, NOR
2. Delay
3. Power \rightarrow Sstate
4. ... \rightarrow Dynamic

Is this a good inverter ?

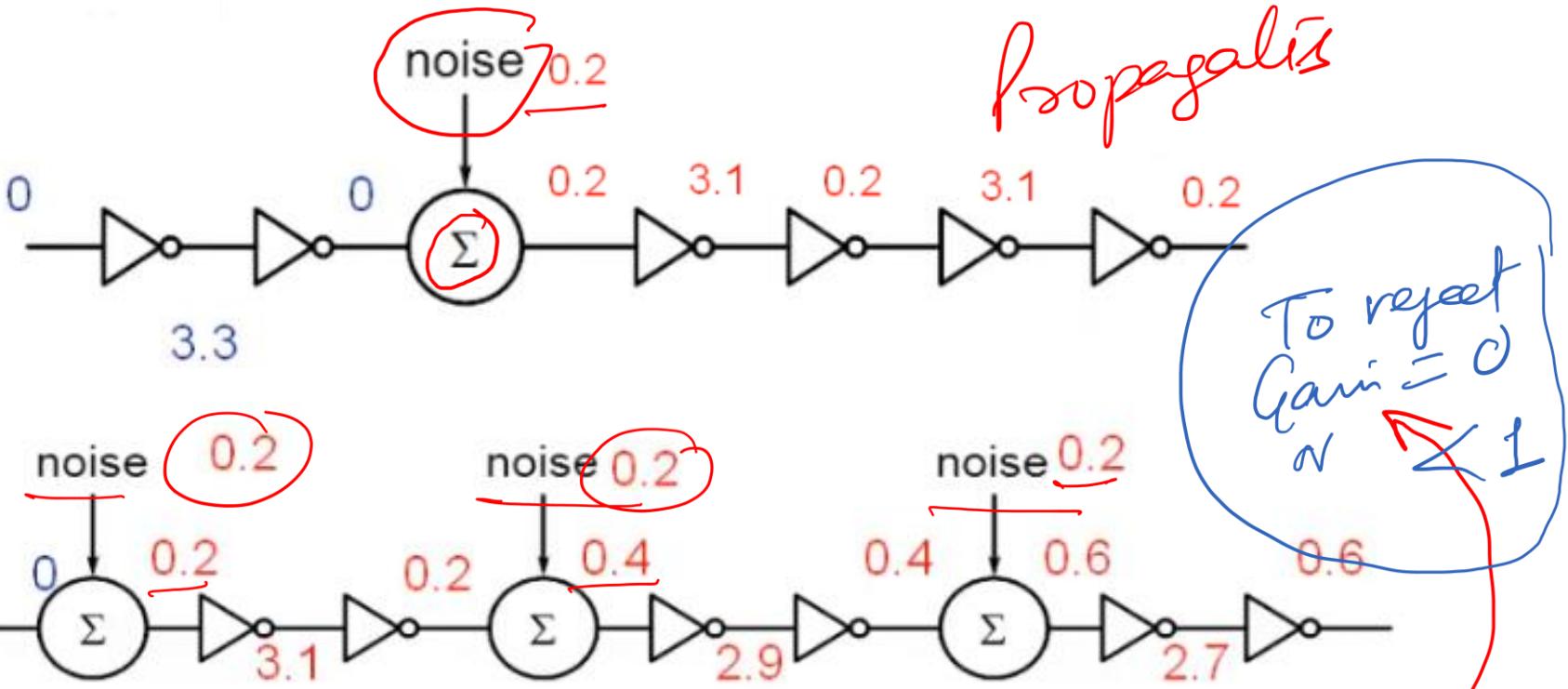


V_{in}



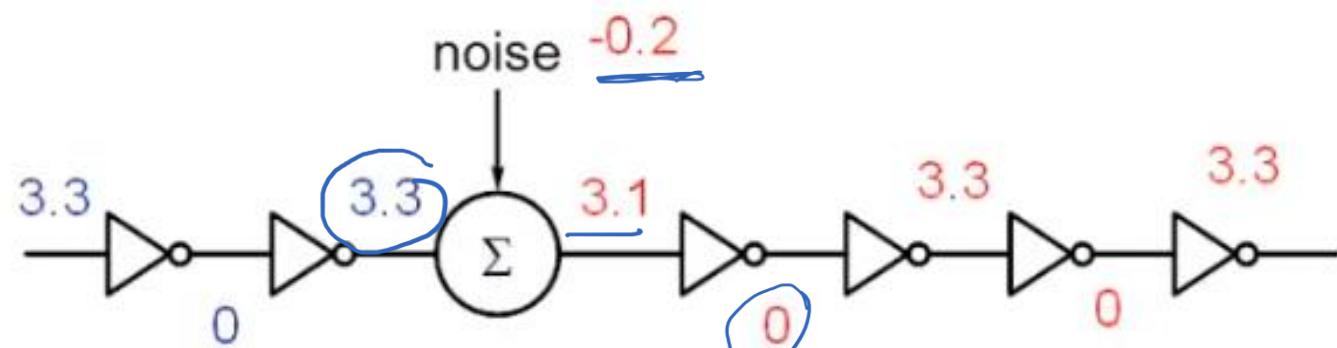
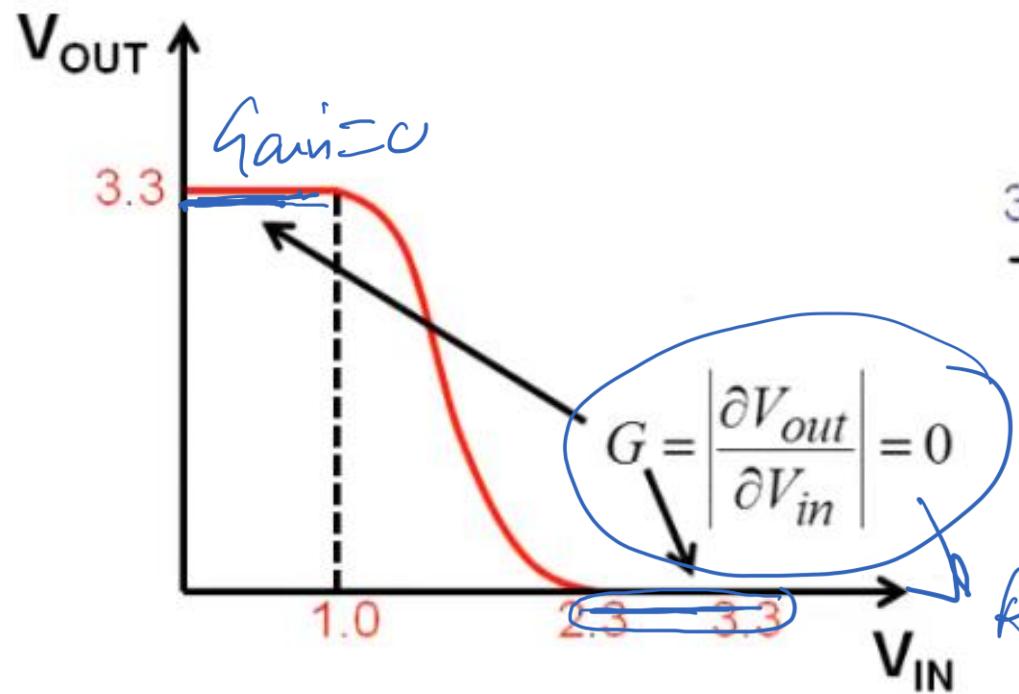
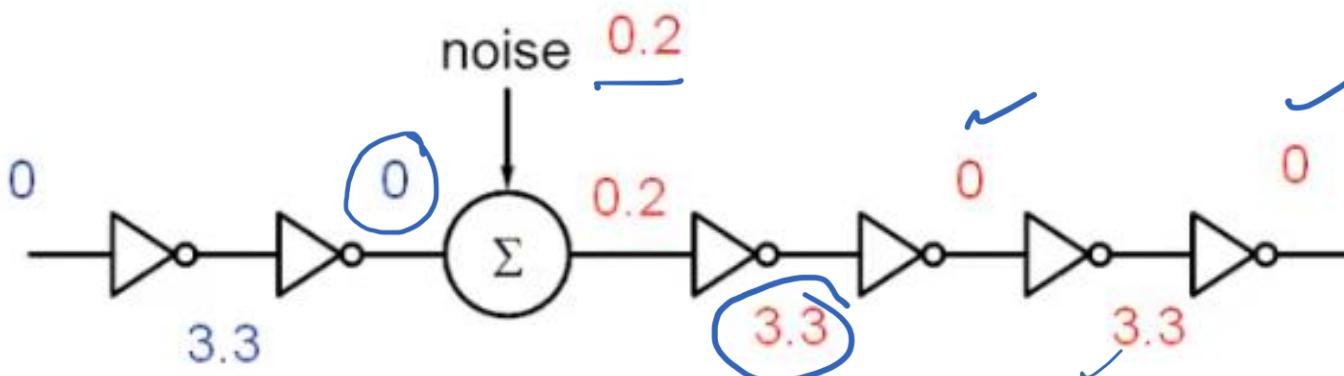
$0 \rightarrow L$] not true in
 $3.3 \rightarrow H$] real life

→ They corrupted by noise

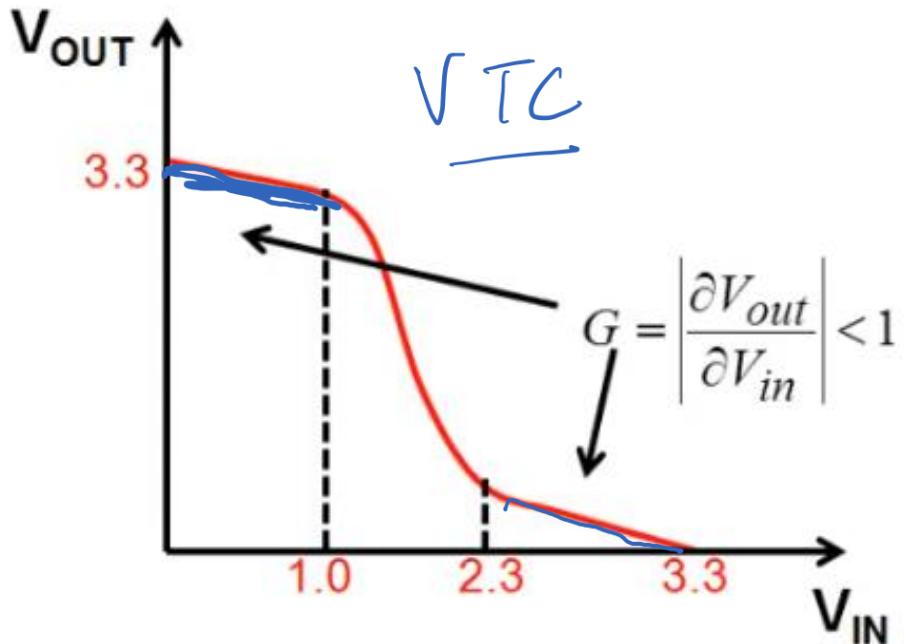


Robust System → Reject the noise or at least suppresses

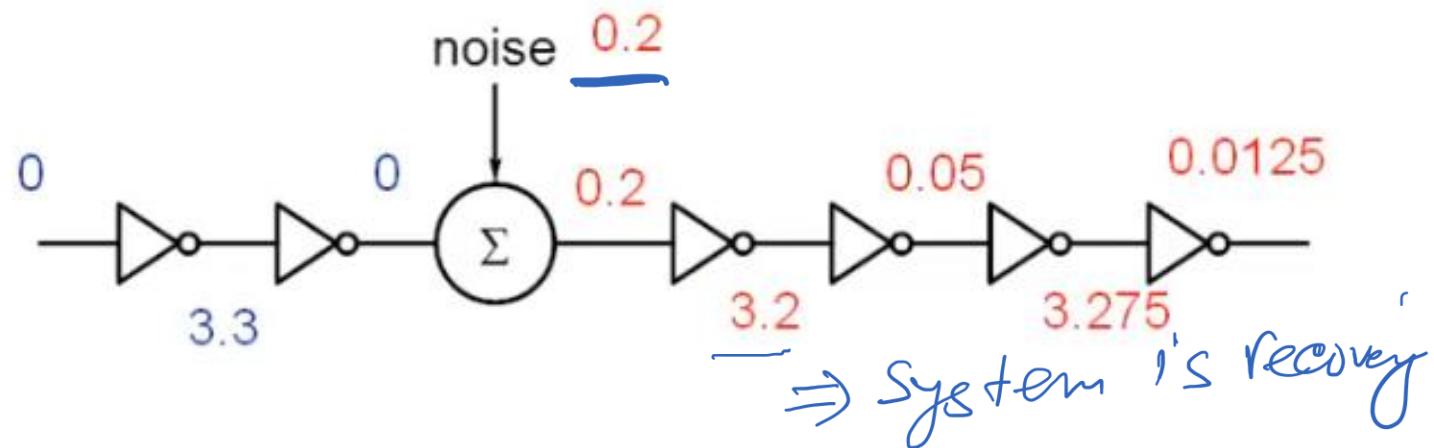
Systems that we design should be robust in presence of noise



Any perturbation
in 3.3V will
get rejected



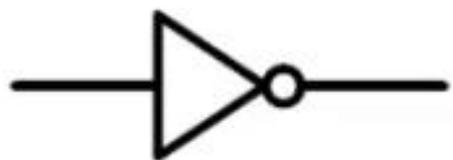
There must be a region with Gain greater than unity



- Lower gain has to be compensated with higher gain to maintain $G_{av} = 1$.

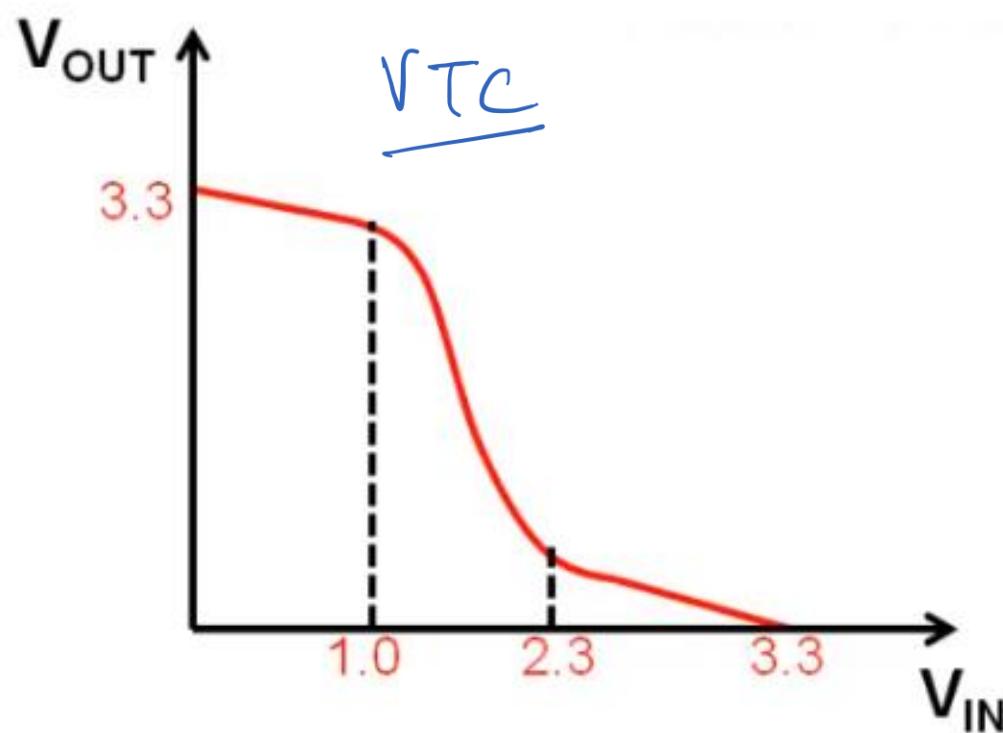
To build an inverter, we need an element that can provide gain

↳ Transistor

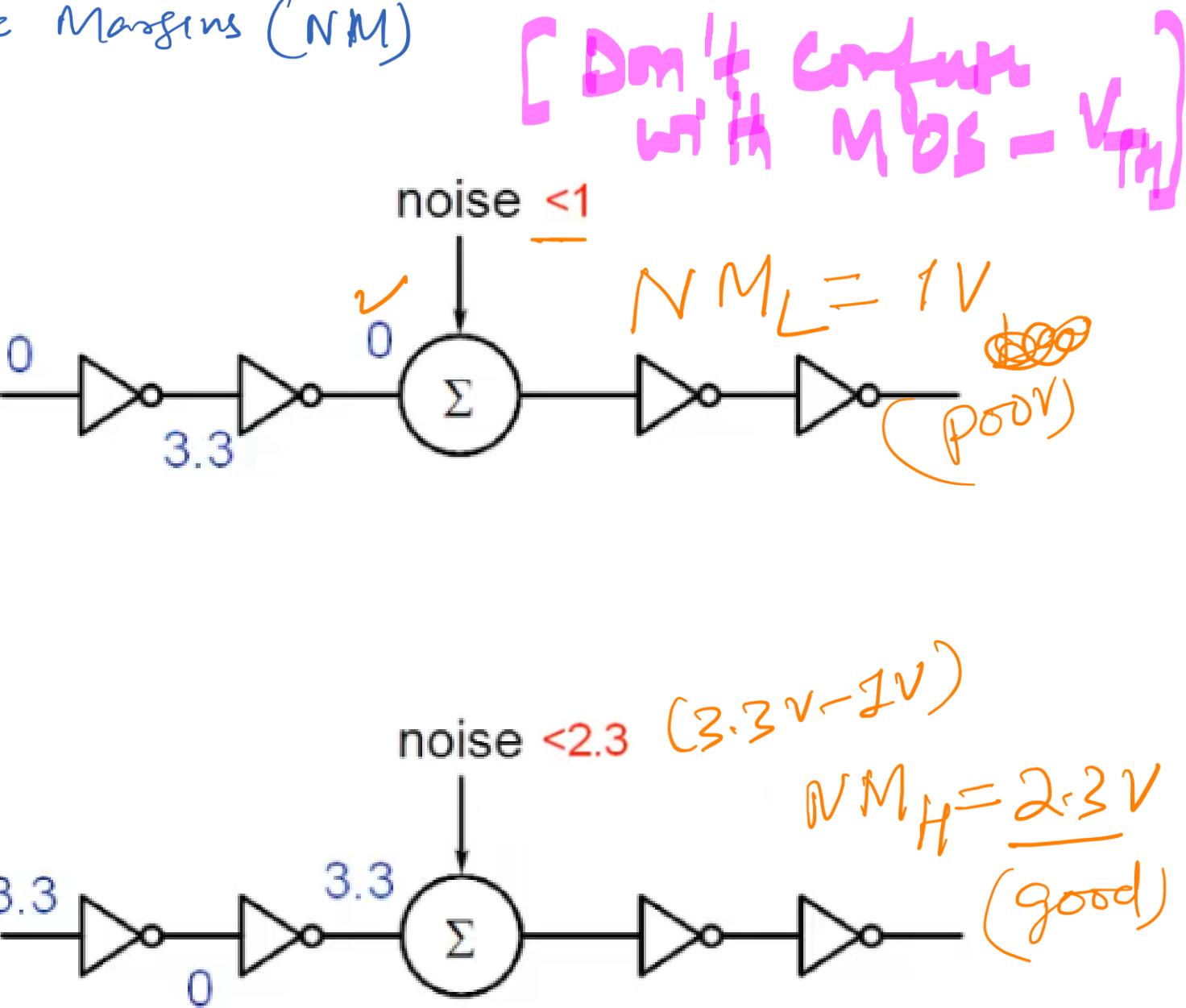
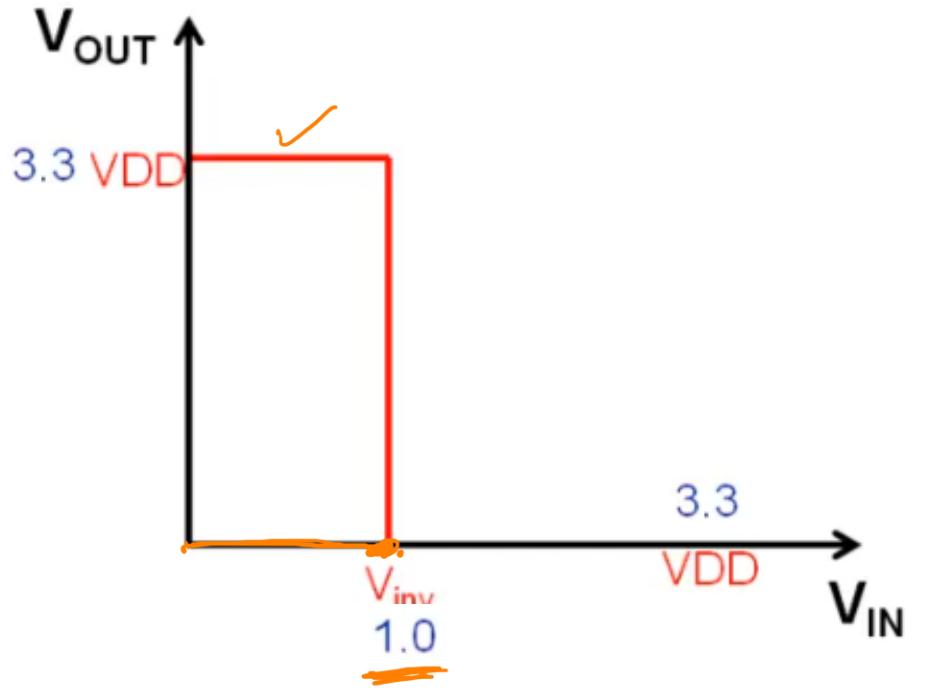


1. Area
2. Delay
3. Power
4. Noise margin

→ Robust in the presence of noise
or Immune to noise.

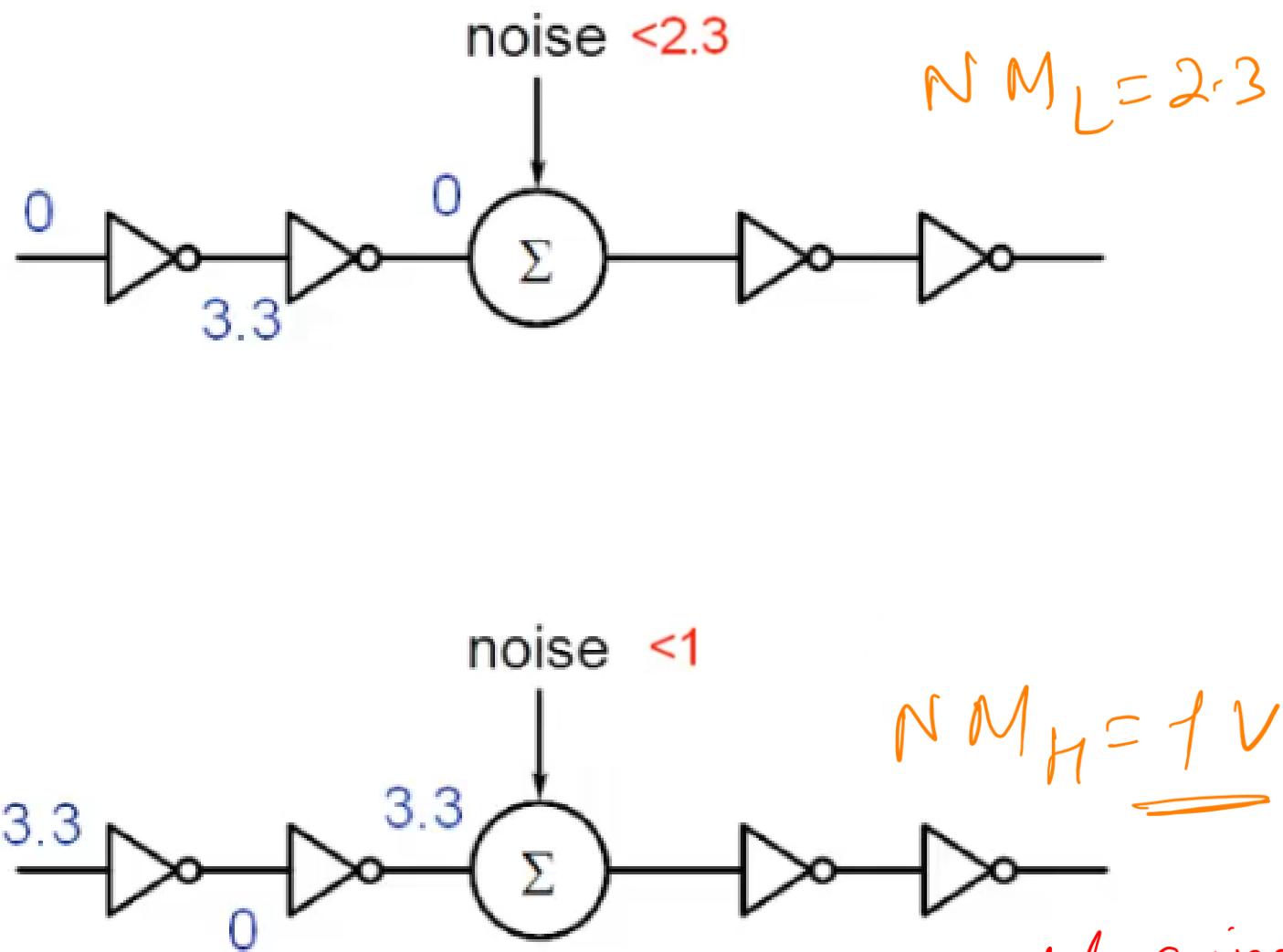
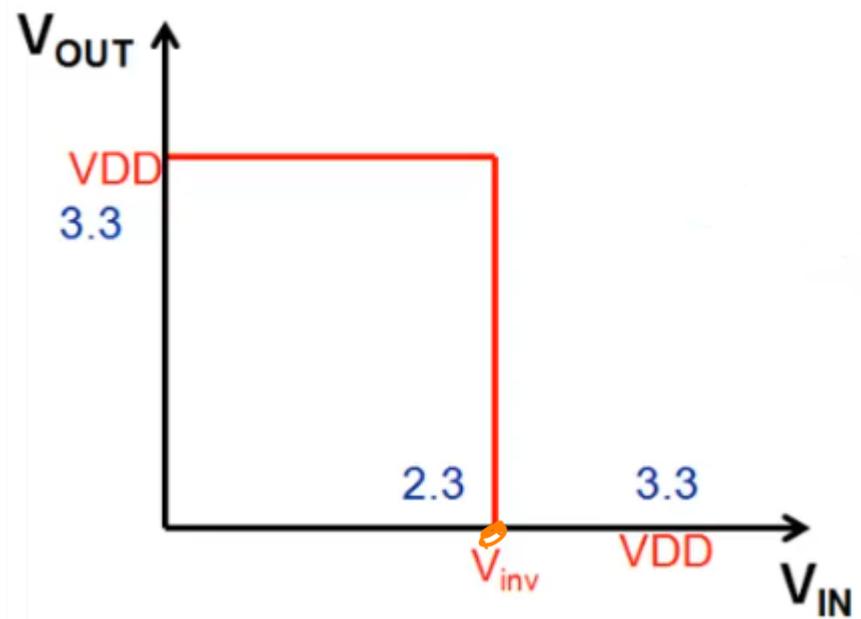


Before discussing the Noise Margins (NM)
Inverter Threshold Voltage
(Poorly)

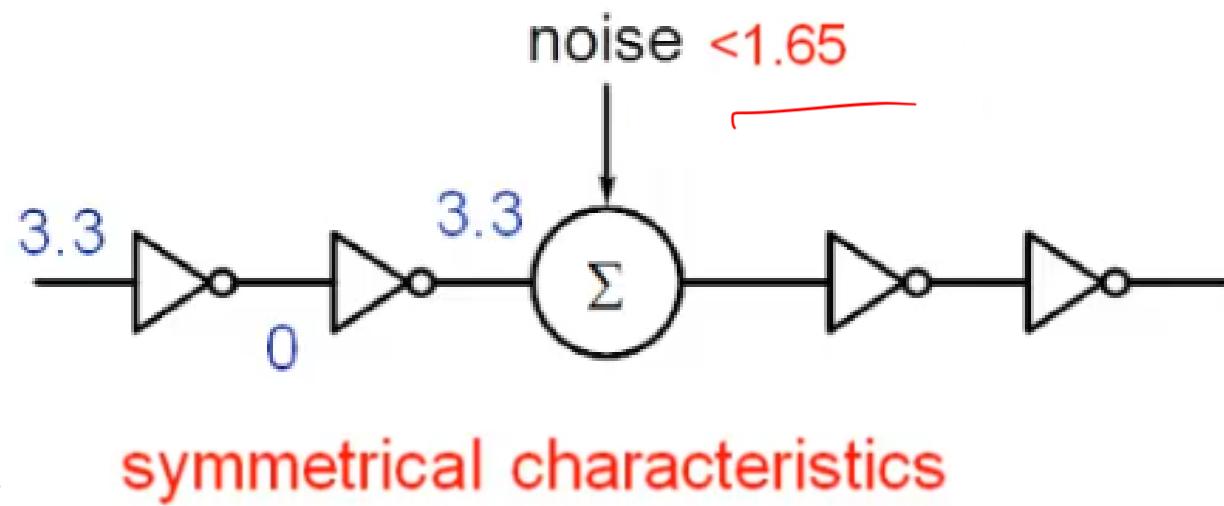
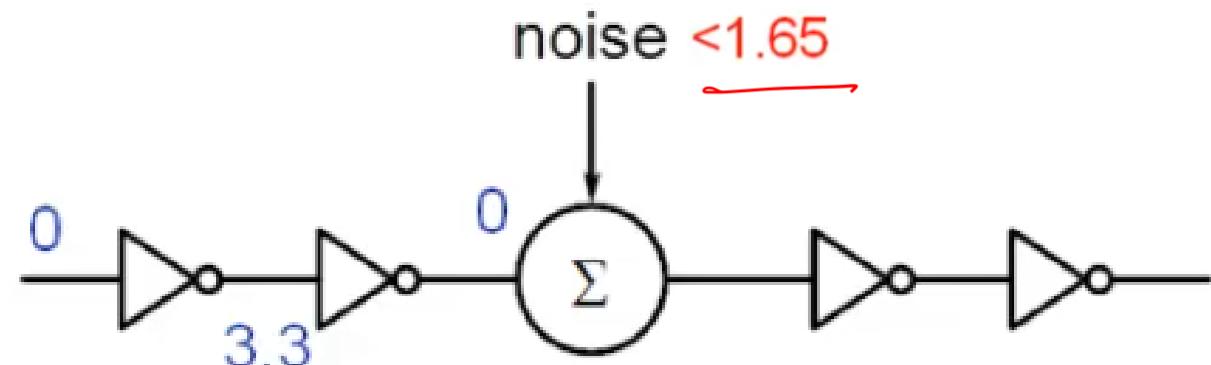
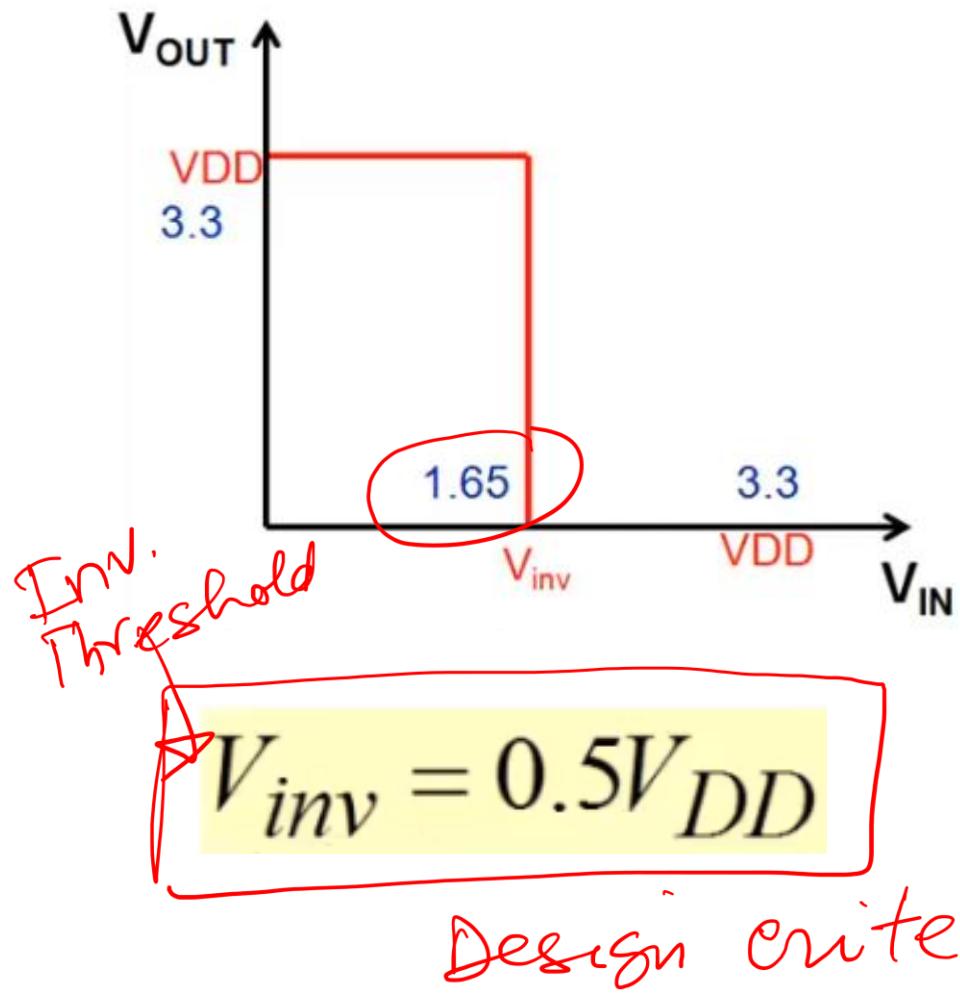


Asymmetrical characteristics

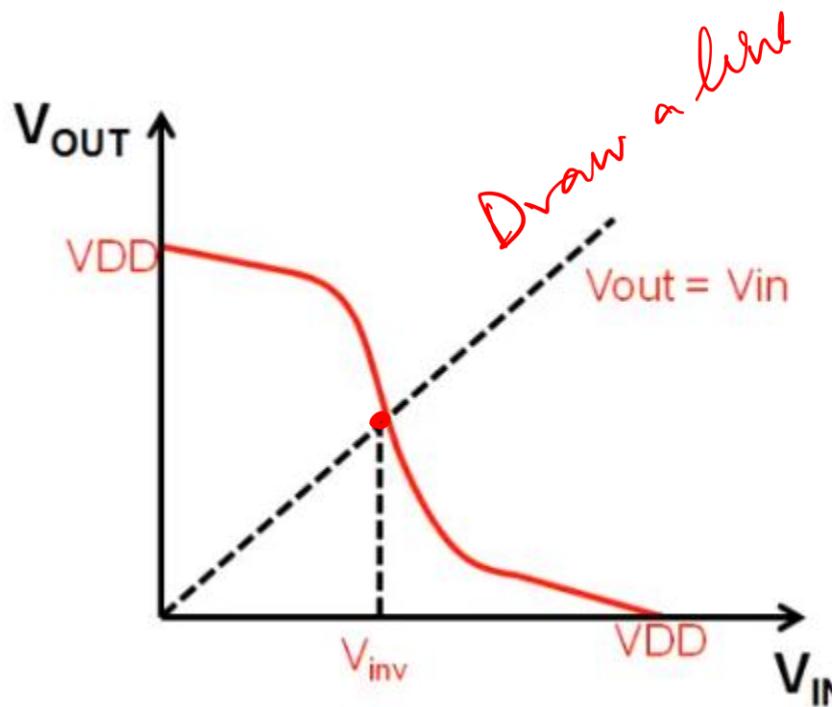
Inverter Threshold Voltage



Asymmetrical characteristics → we should aim for symmetrical characteristics



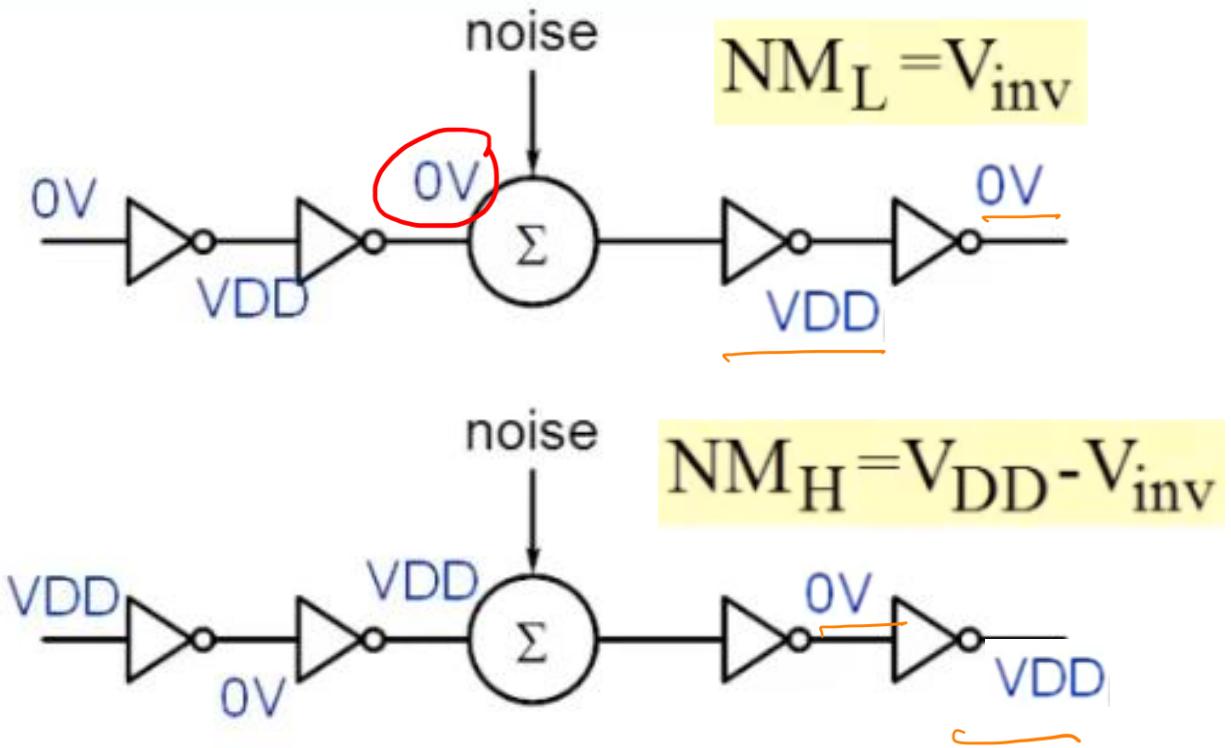
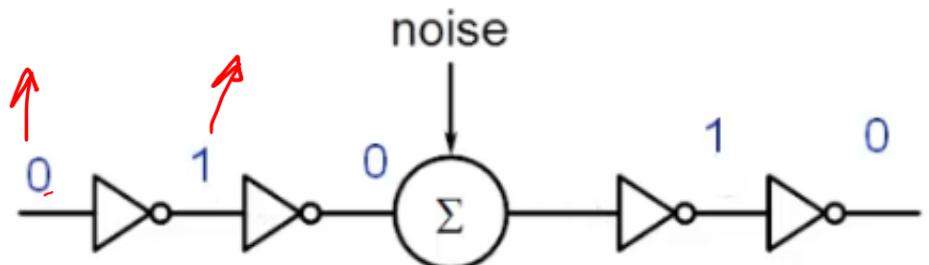
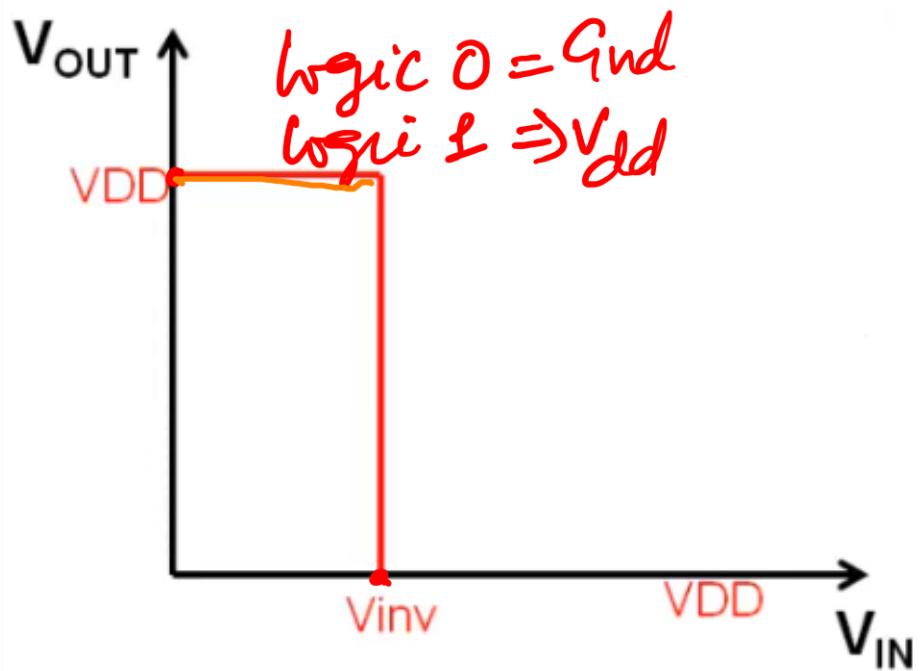
Inverter Threshold Voltage



For $\underline{V_{in}} > \underline{V_{inv}}$, the output is closer to “0”

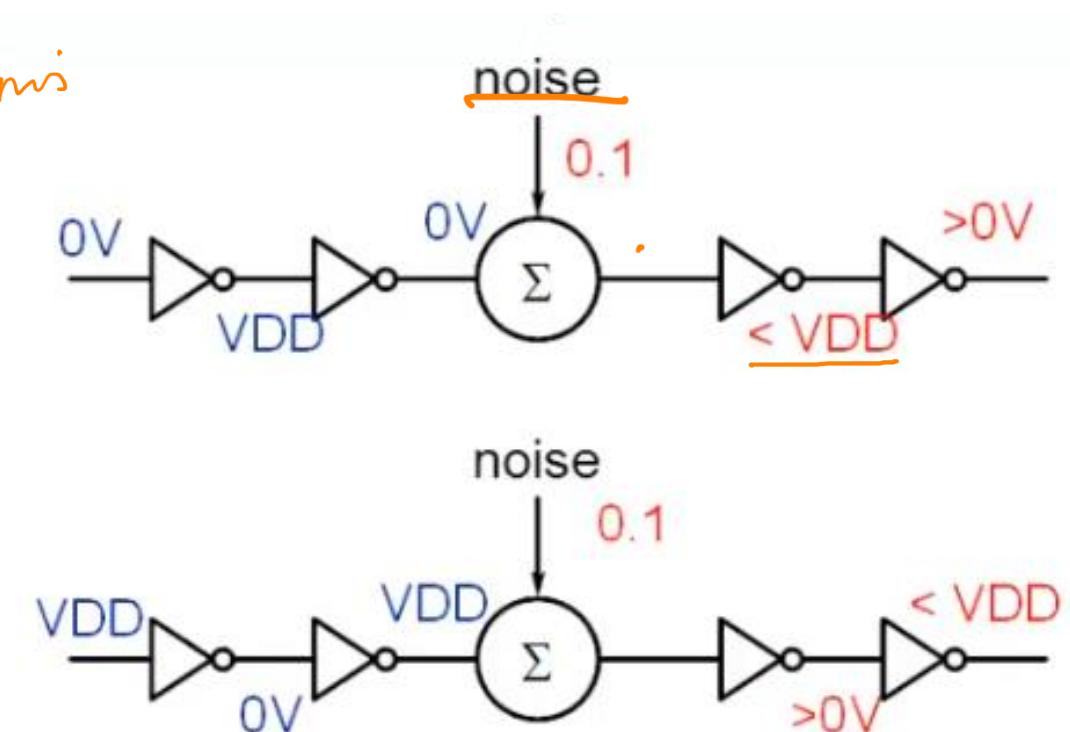
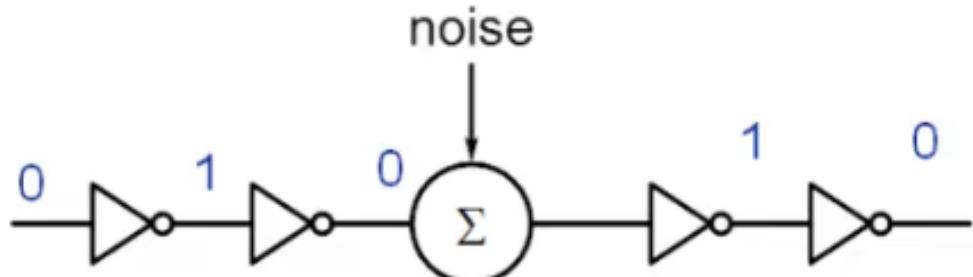
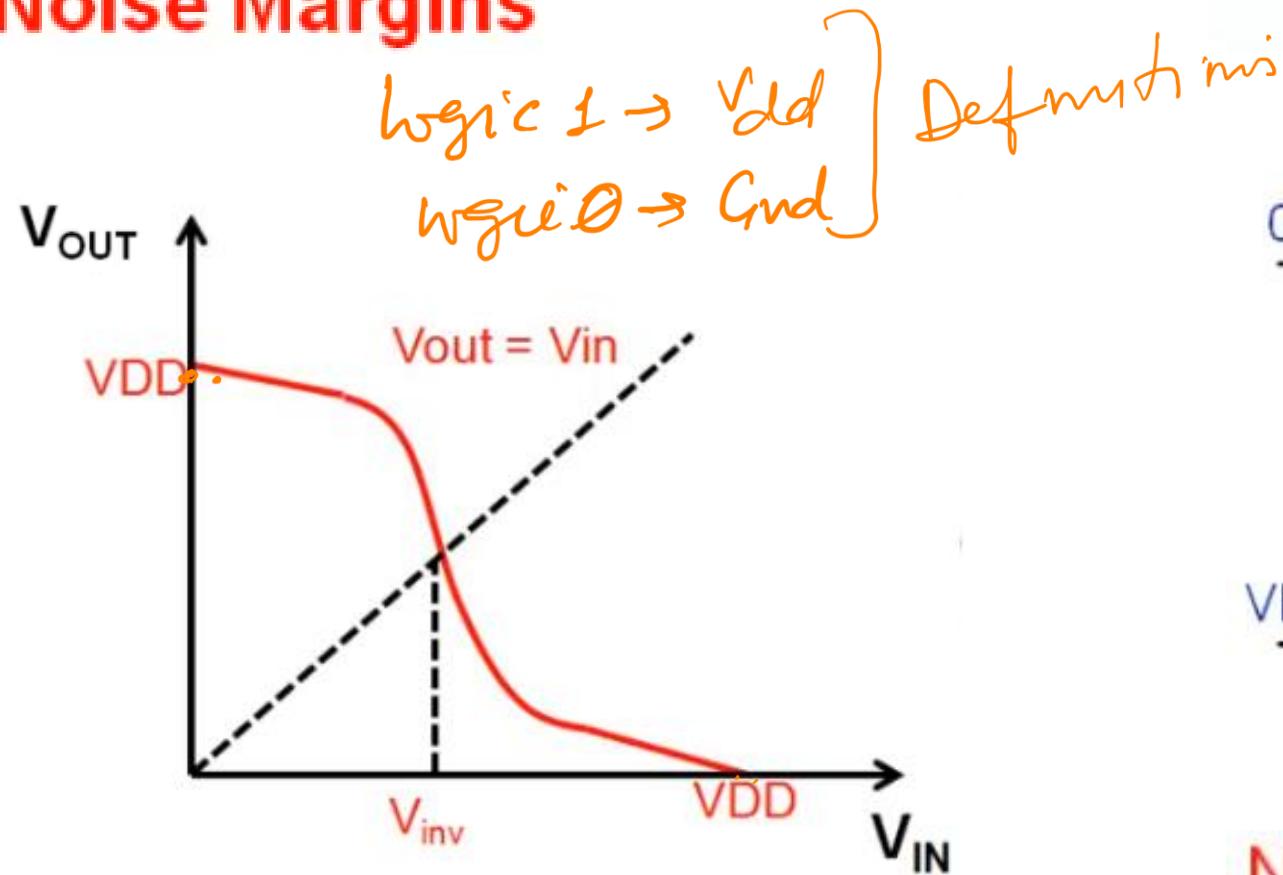
$$\underline{V_{inv}} = 0.5V_{DD}$$

Noise Margins

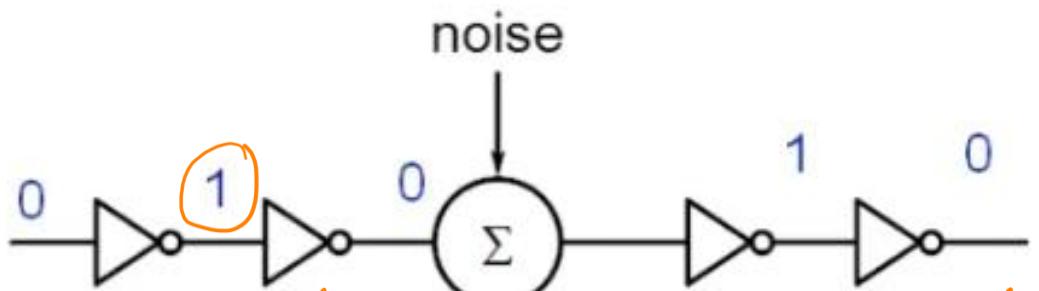
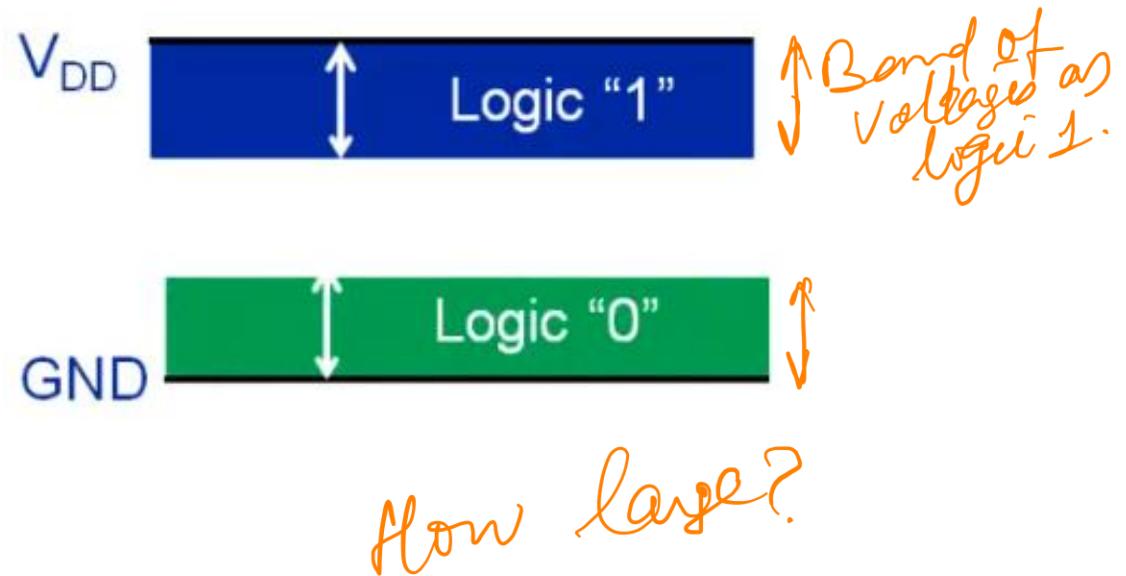
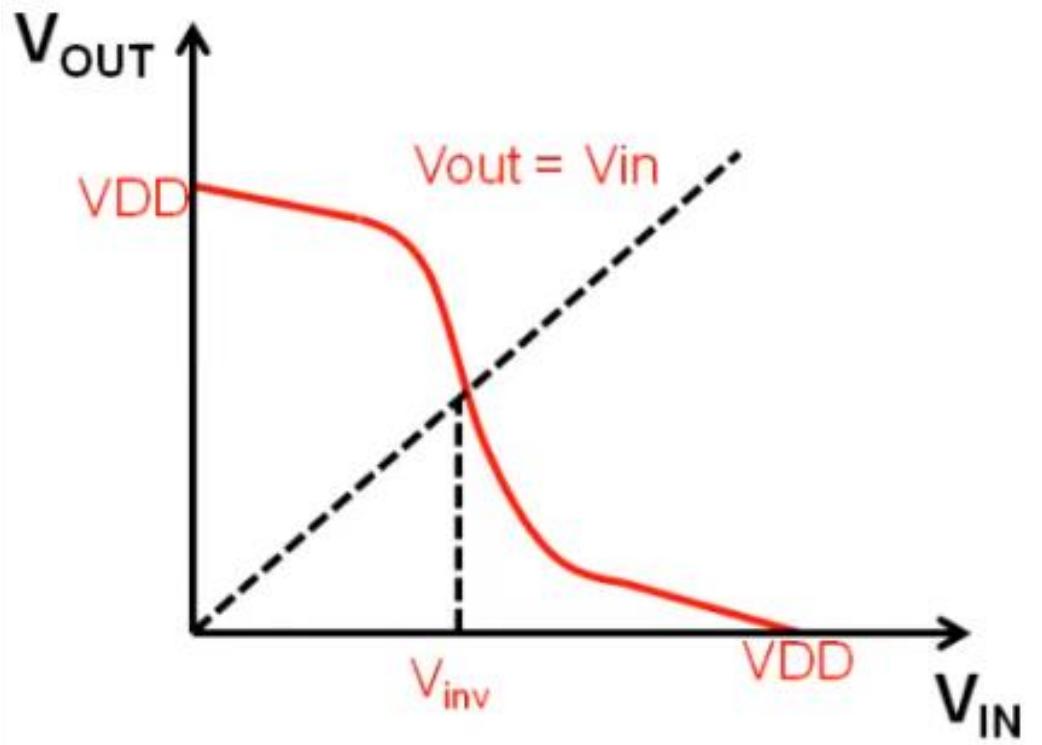


Logical correctness

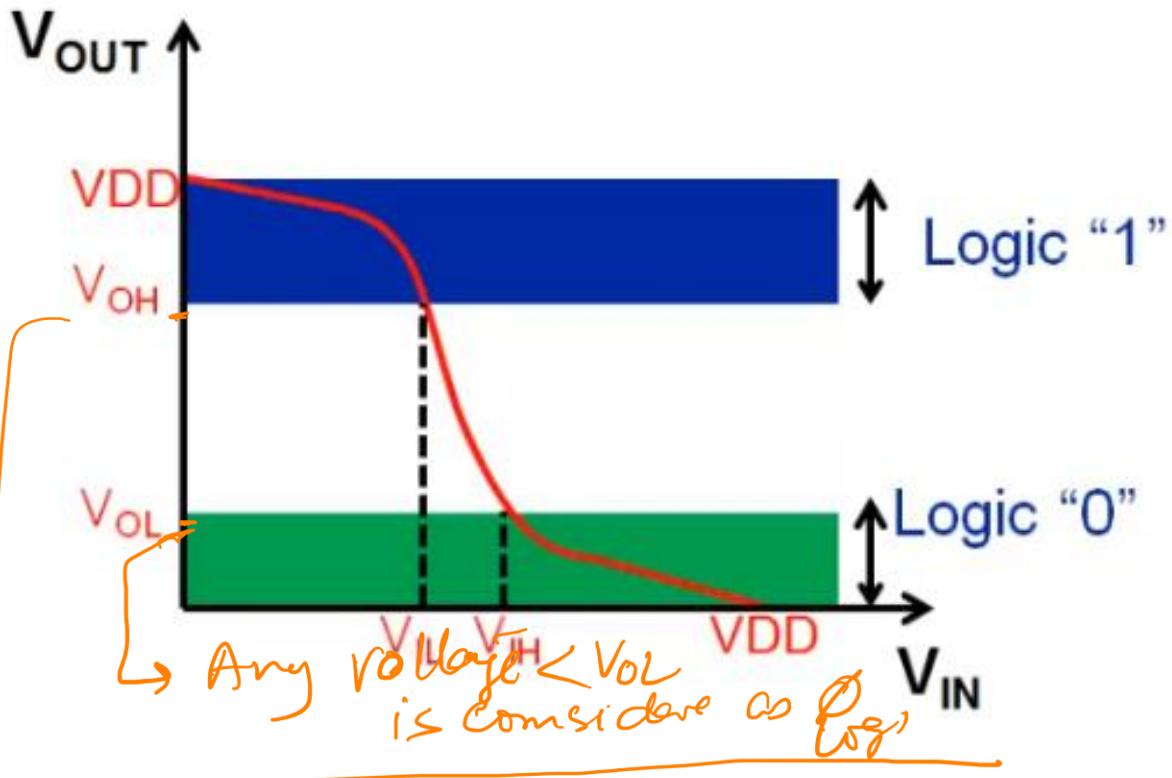
Noise Margins



Need proper definition of logic levels in terms of voltages

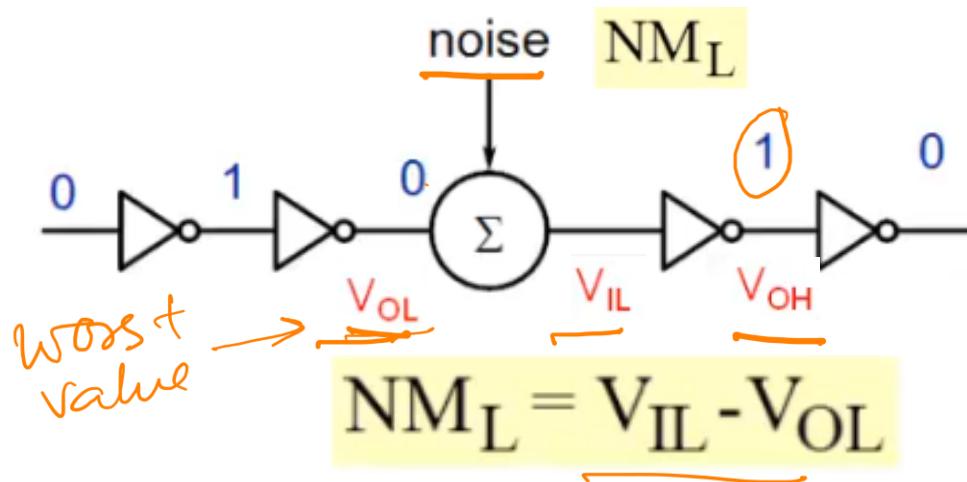


whatever values we are assigning to logic 0, logic 1 is fine, but should be consistent.

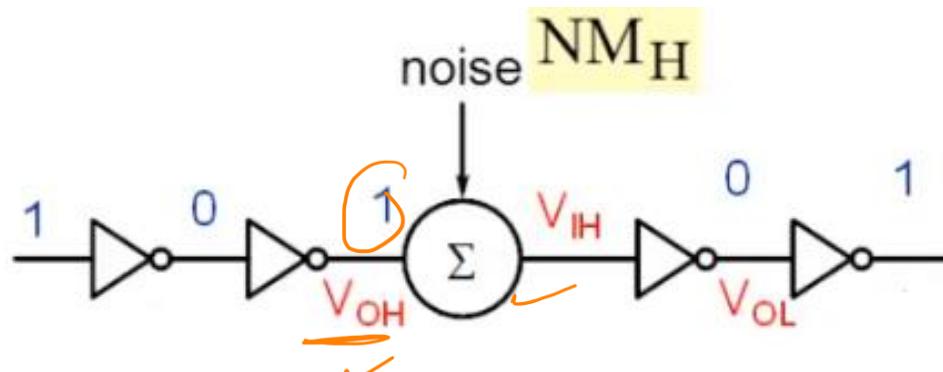


\downarrow is the min voltage that my system should be considered as logical-1.

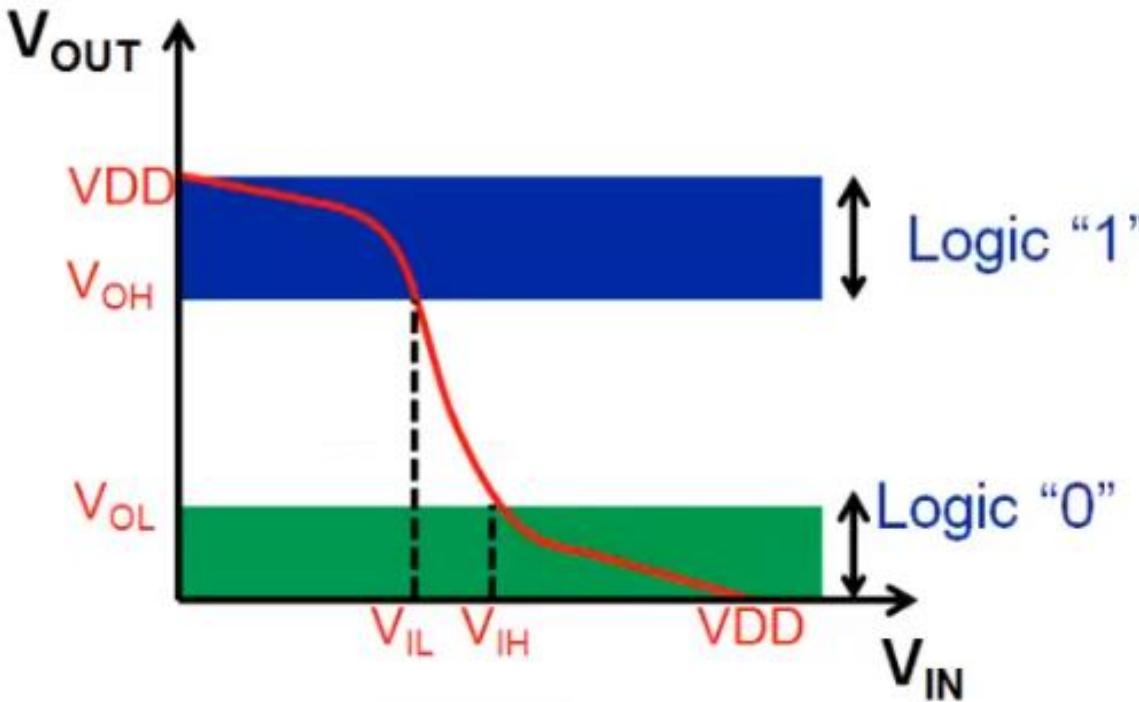
$V_{DD} > V_{OH} > V_{IH} > V_{IL} > V_{OL} > 0$



$$NM_H = V_{OH} - V_{IH}$$

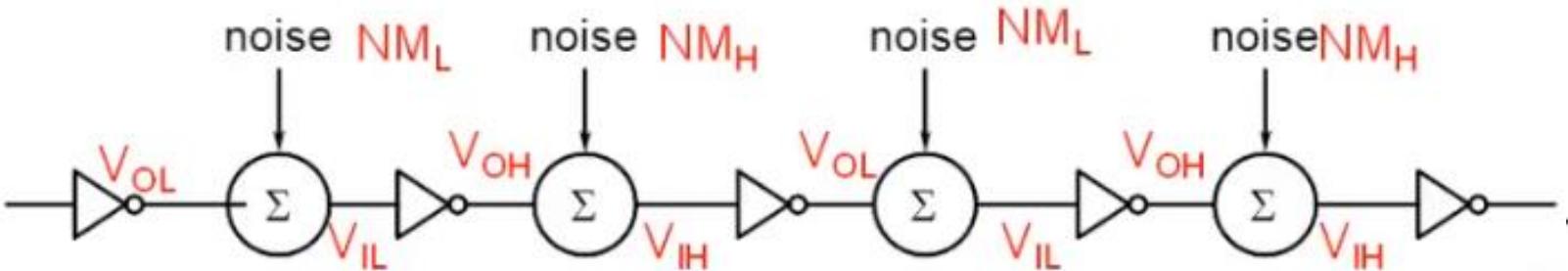


Noise Margins



$$NM_L = V_{IL} - V_{OL}$$

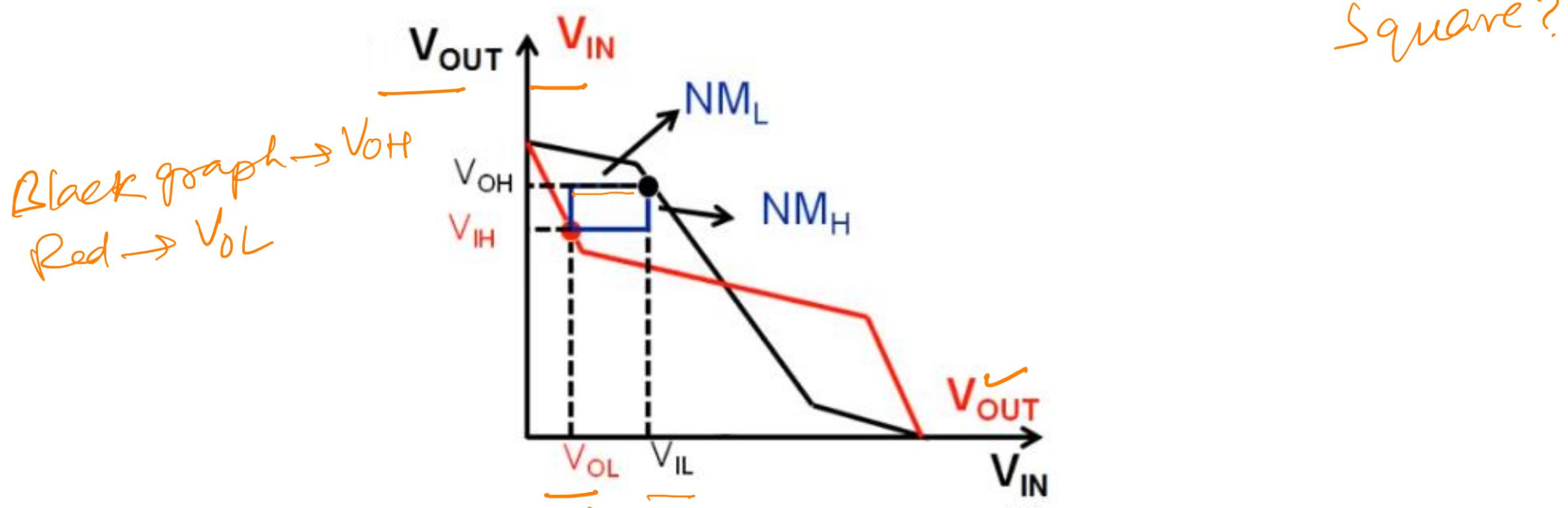
$$NM_H = V_{OH} - V_{IH}$$



How do we find these threshold values?

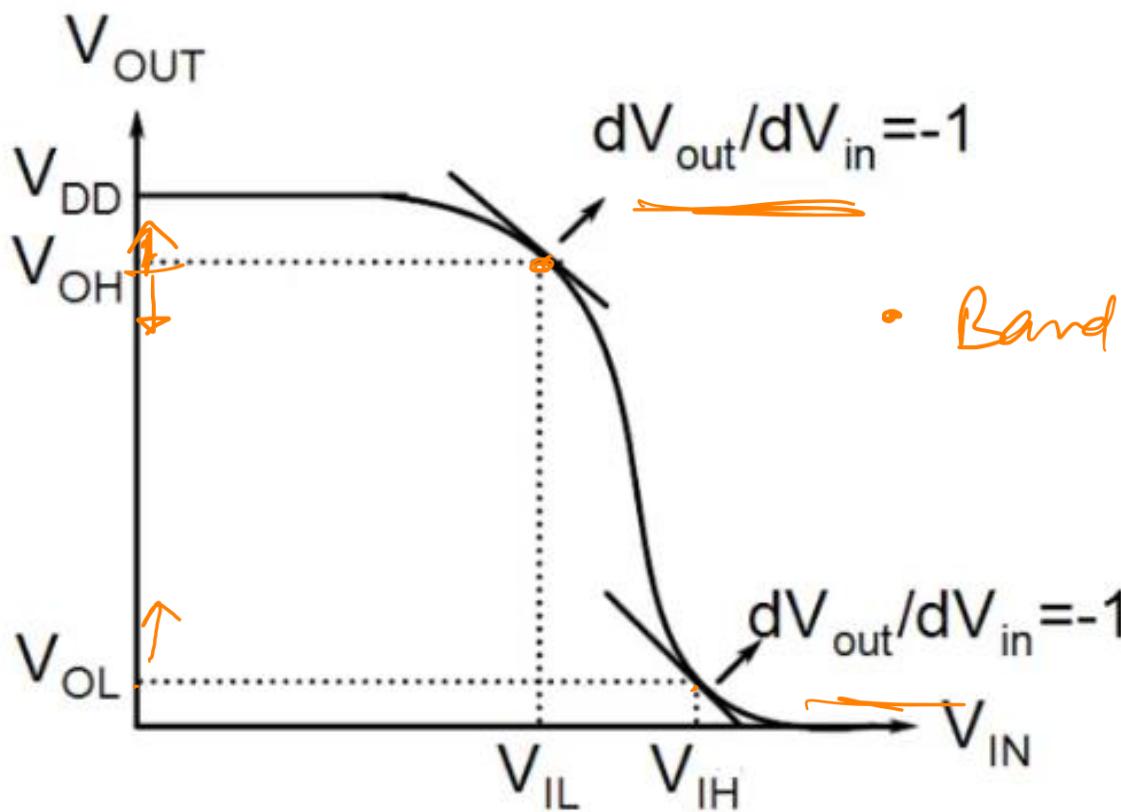
flip VTC

Maximize $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$



For $NM_H = NM_L$, find the biggest square that can be accommodated

Alternative Method For finding threshold values?



on VTC, find a point (?) on the slope, where gain = -1.

- Band ($V_{DD} - V_{OH}$) \rightarrow how low one can go to V_{OH} .
- till a point where slope is (-1)
- Beyond that NM will degrade.

-valid high and low logic levels should be defined as bands with one determined by the unity-Gain points on VTC

How do we find these threshold values?

② Decrease V_{OH} , increase V_{OL} (by the same amount)
 $\downarrow 0.1V$

What will happen to V_{IL} ?

④ Tell what point we can do this
 $\uparrow V_{OL} \uparrow \uparrow$

This will stop when we reach where $G_m = 1$

$$\uparrow NM_L = V_{IL} - V_{OL}$$

$$\uparrow NM_H = V_{OH} - V_{IH}$$

① Both noise margins are very small

① Let's take (e.g.)

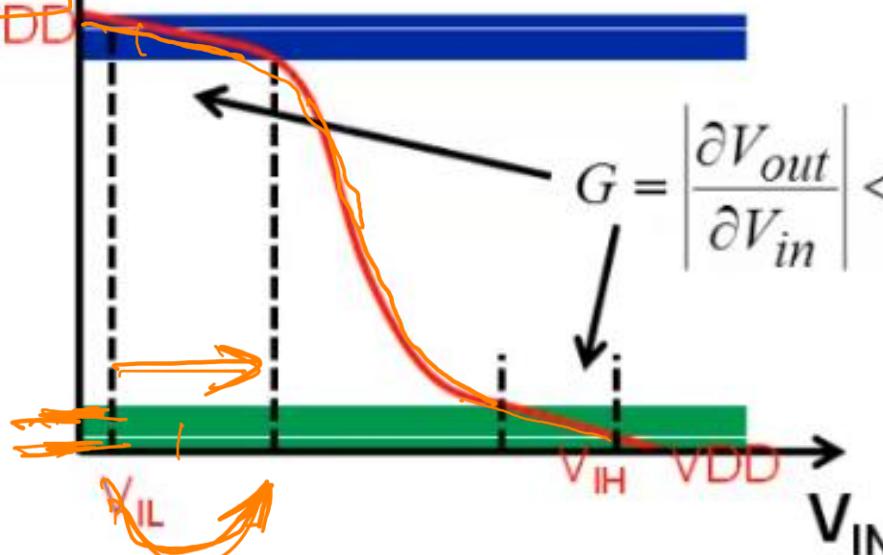
$$V_{OH} = V_{dd}, V_{OL} = 0V$$

extreme case

considering symmetric V_{TH}

• What is NM?

$$V_{IL} = 0 \\ NM = 0$$



$$G = \left| \frac{\partial V_{out}}{\partial V_{in}} \right| < 1 \Rightarrow \left| \frac{\partial V_{in}}{\partial V_{out}} \right| > 1$$

③ we increase V_{OL} by 0.1, but change in V_{IL} is much larger

→ Small change in V_{out} (V_{OL}) make large change in V_{in} (V_{IL}).

some NM_L, NM_H

$$NM_L = V_{IL} - V_{OL}$$

increase $\delta V_{OL} = -\delta V_{OH}$

This will change V_{IL}, V_{IH}

$\Rightarrow \delta V_{IL} = -\delta V_{IH}$

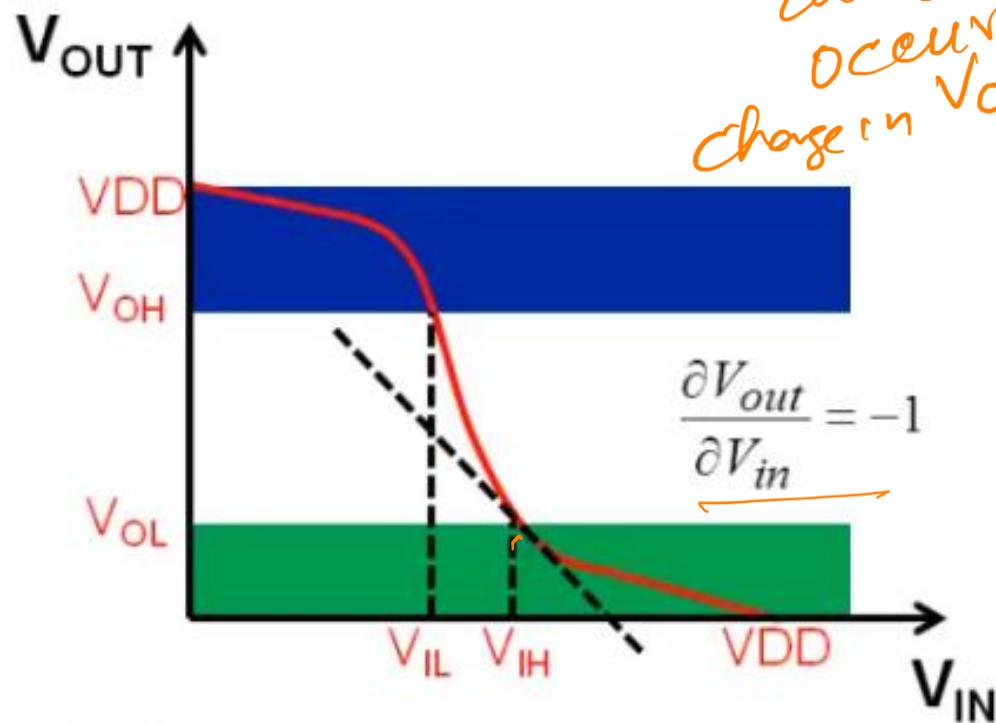
Symmetrical VTC

$$\underline{\delta(NM_L)} = \underline{\delta V_{IL}} - \underline{\delta V_{OL}}$$

$$\delta(NM_L) = \left(\frac{\delta V_{IL}}{\delta V_{OL}} - 1 \right) \times \delta V_{OL}$$

$$\frac{\delta(NM_L)}{\delta V_{OL}} = \left(\frac{1}{-\frac{\delta V_{OL}}{\delta V_{IH}}} - 1 \right)$$

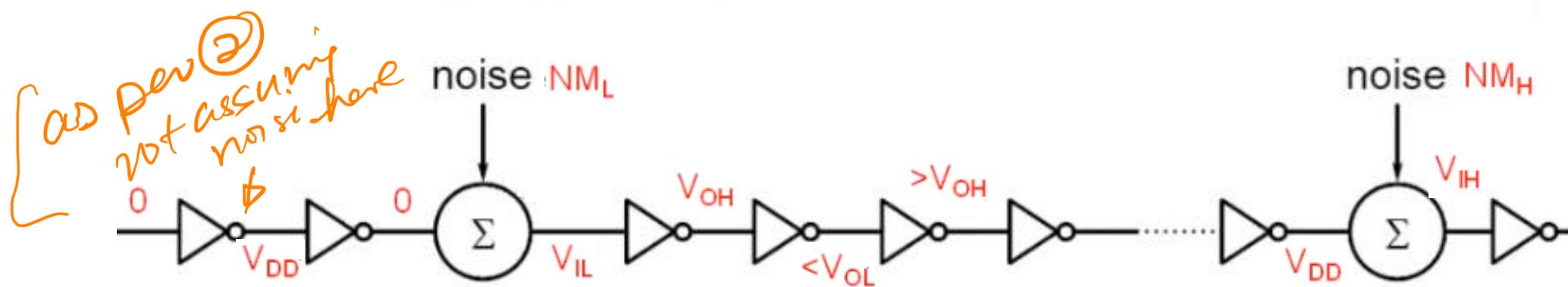
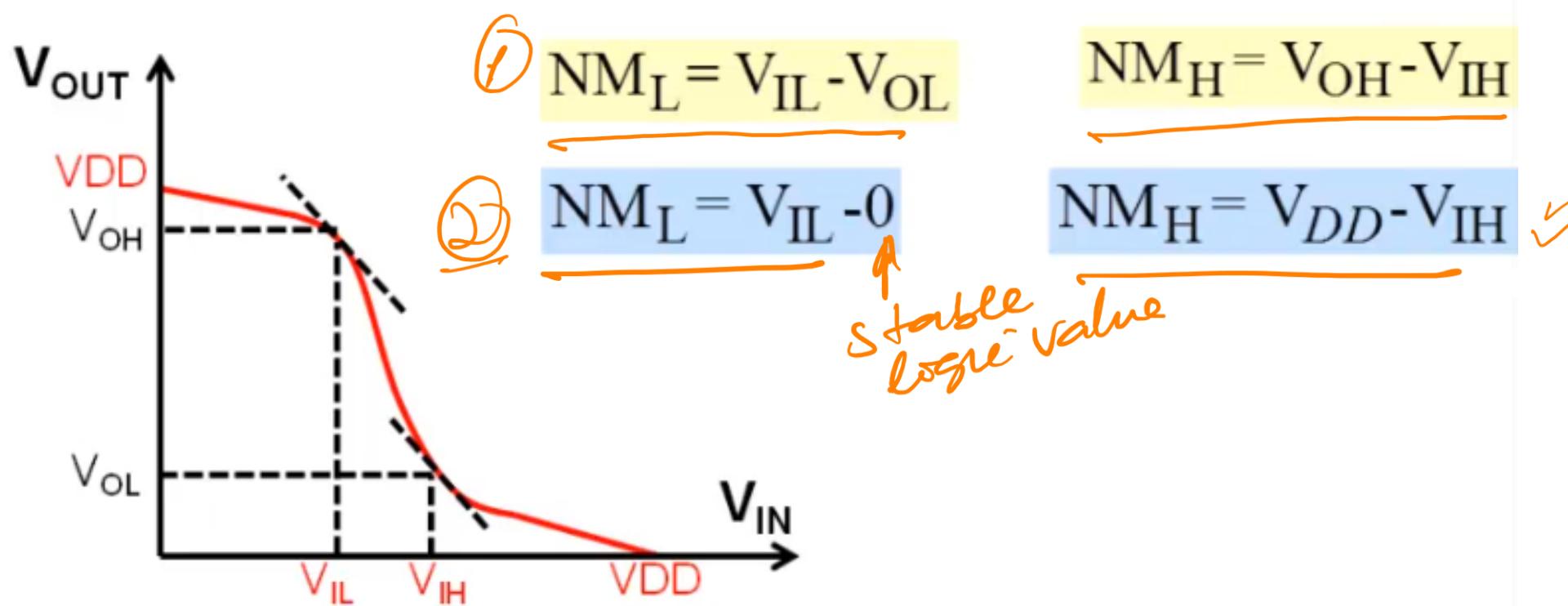
$$\delta V_{IL} = -\delta V_{IH}$$



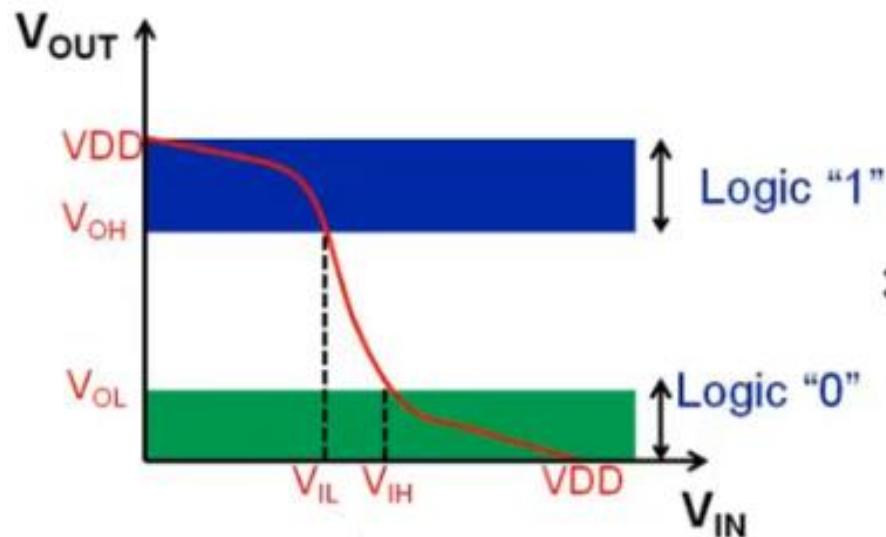
How much
change in NM_L
occur due to
change in V_{O1}

As long as $-\frac{\partial V_{out}}{\partial V_{in}} < 1$ NM_L improves

Noise Margins: Alternative definition

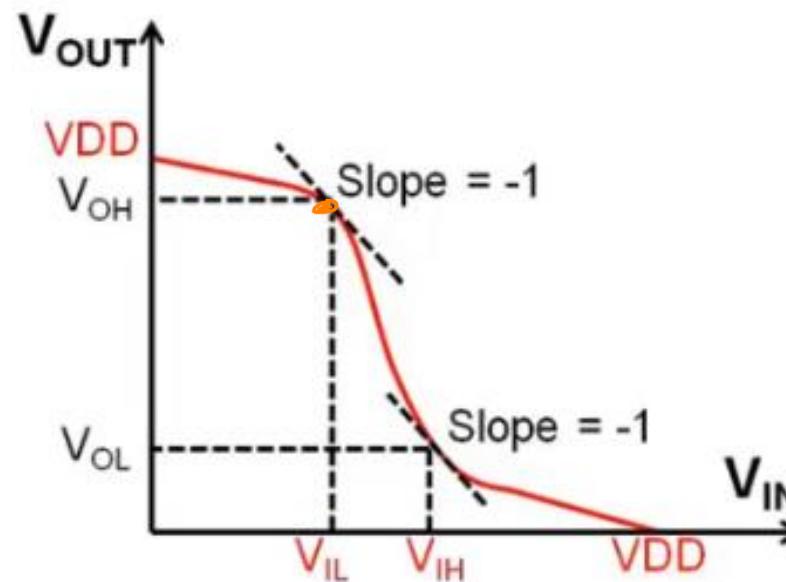
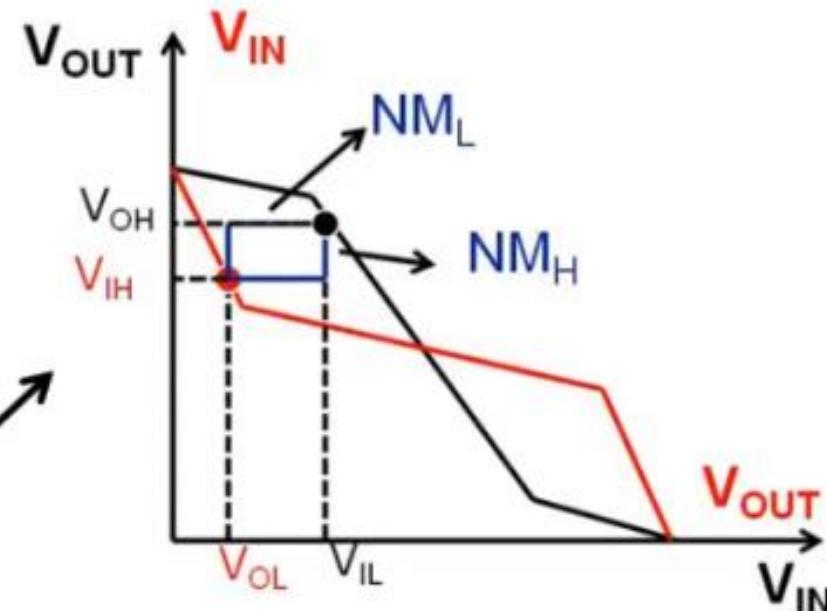


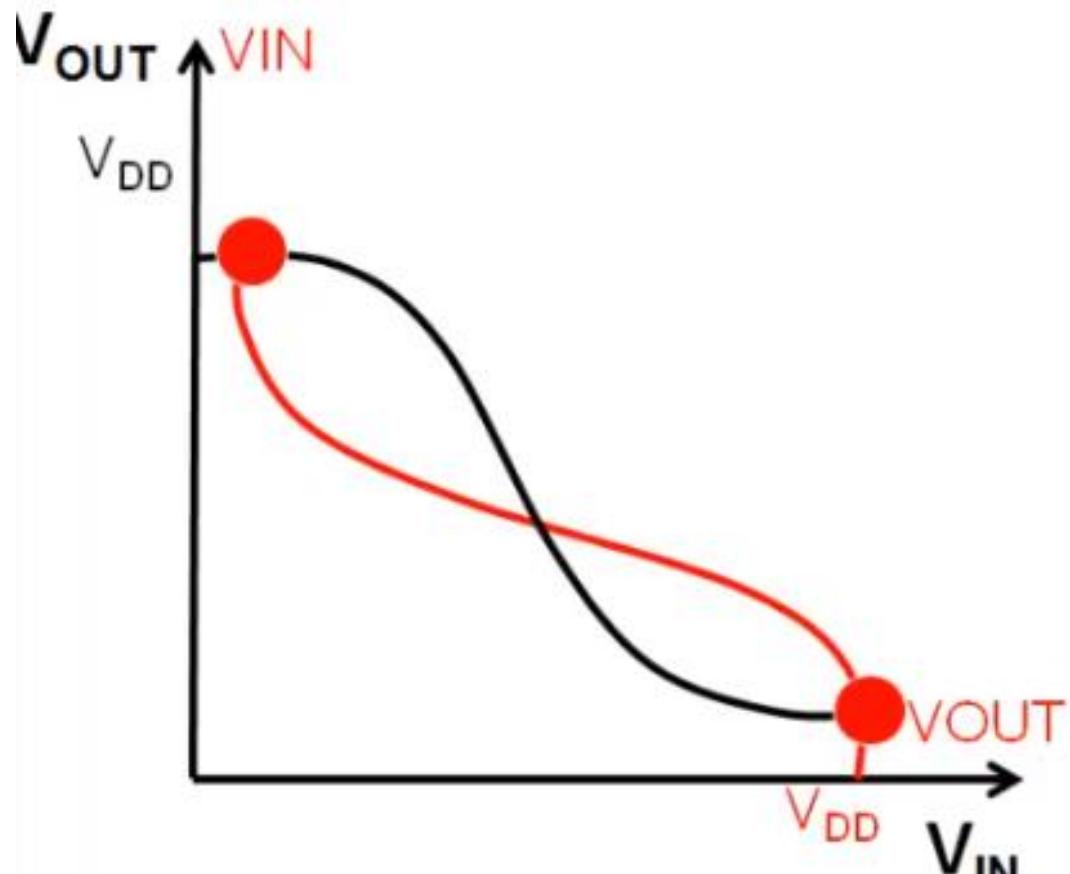
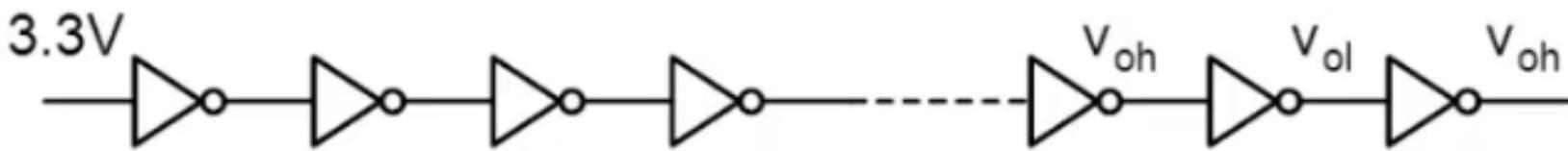
Noise Margin: Summary



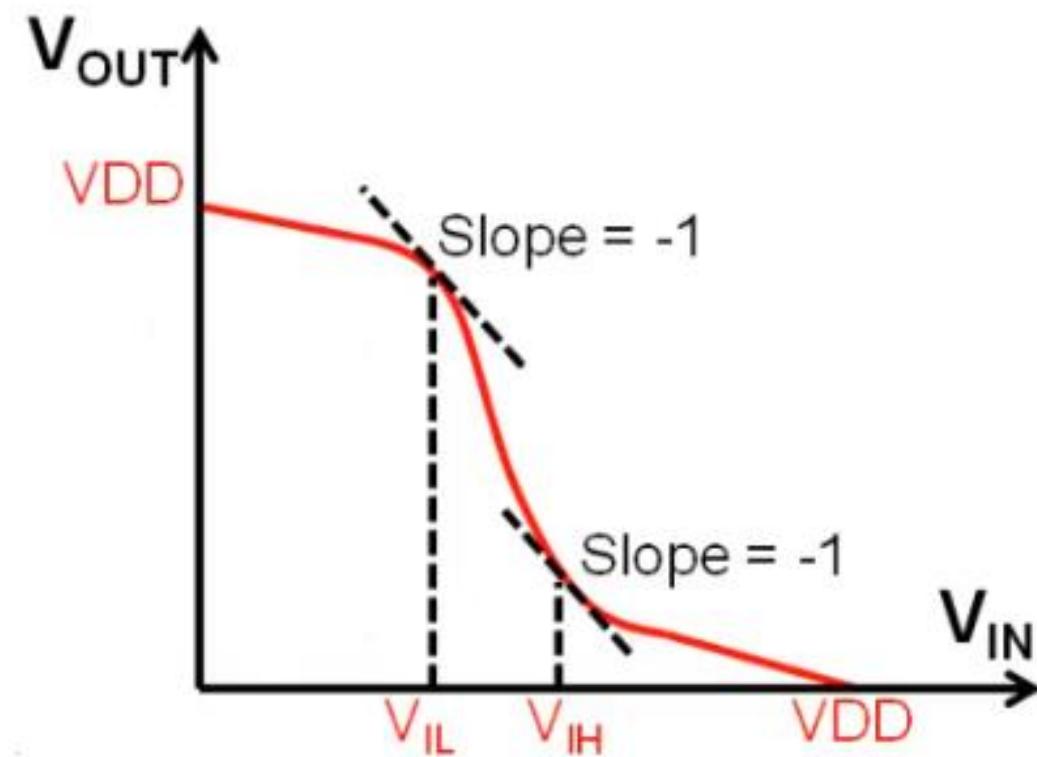
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$





$$NM_L = V_{IL} - v_{ol}$$



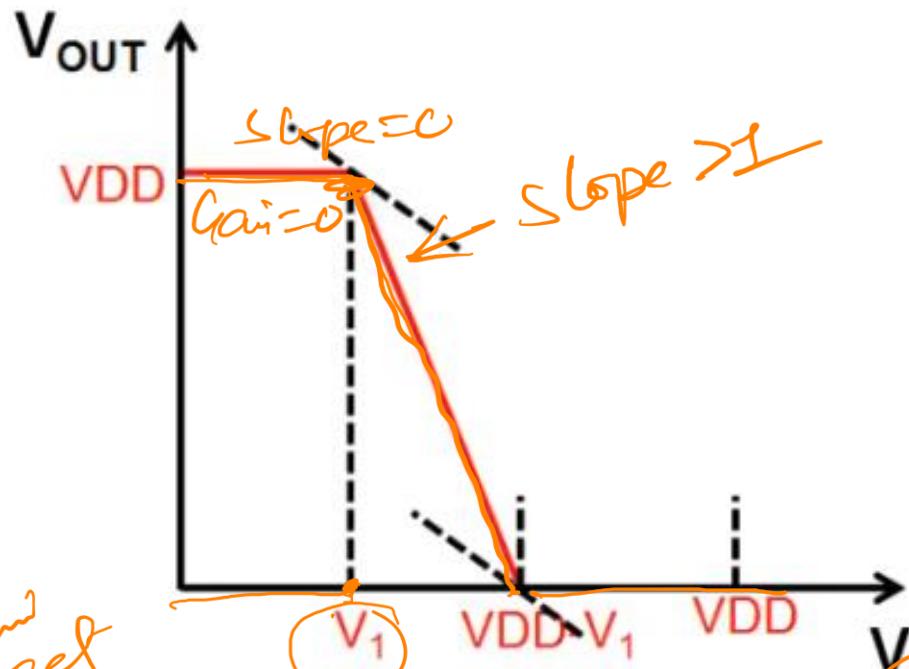
$$NM_H = v_{oh} - V_{IH}$$

Example-1

(Hypothetical VTC)

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$



more gain
↑ can get
from the INV

Max. NM you
can have is $\sqrt{V_{DD}/2}$

$$G_{max} = \left(\frac{V_{DD}}{V_{DD} - 2V_1} \right)$$

$\xrightarrow{\frac{V_{DD}-0}{V_{DD}-V_1}, \frac{V_1}{V_{DD}}} \frac{V_1}{V_{DD}} = 0.5 \left(1 - \frac{1}{G_{max}} \right)$

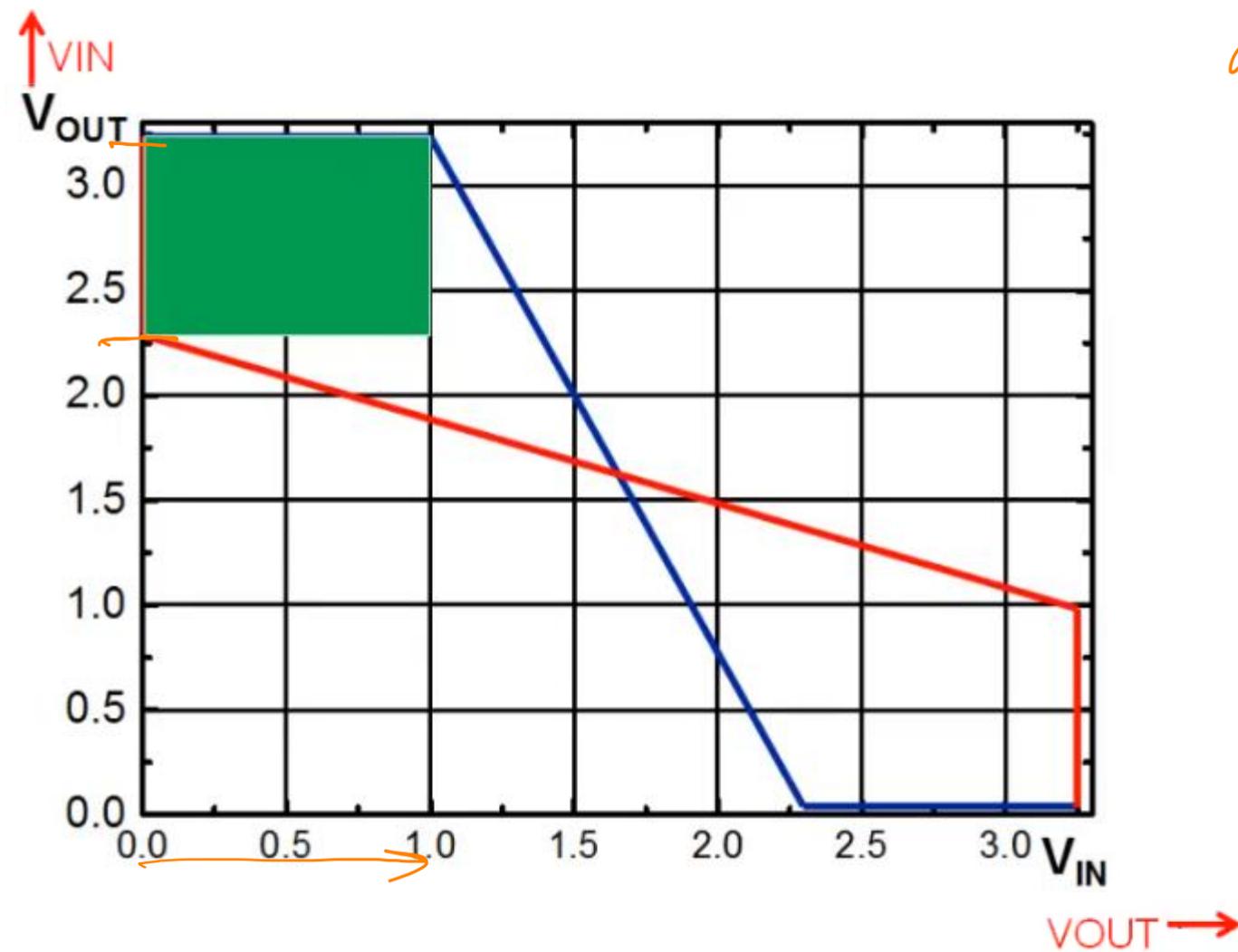
$$\frac{NM_H}{0.5V_{DD}} = \left(1 - \frac{1}{G_{max}} \right)$$

$$\underbrace{V_{OH} = V_{DD}}_{\text{---}}; \underbrace{V_{IL} = V_1}_{\text{---}}$$

$$\underbrace{V_{OL} = 0}_{\text{---}}; \underbrace{V_{IH} = V_{DD} - V_1}_{\text{---}}$$

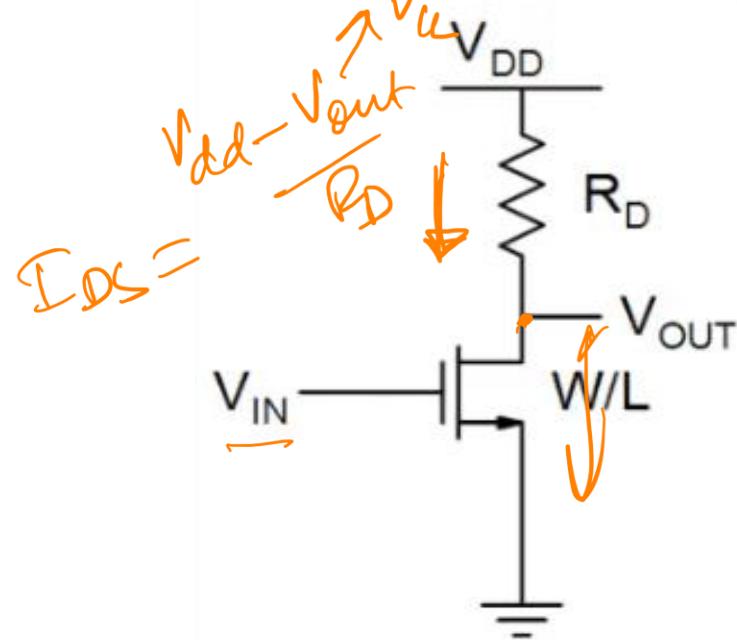
$$NM_H = NM_L = V_1$$

A kind of measure of
how close to the
max.
↳ depend on how large
is the Gain



don't need
many gain
points

Inverter with Resistive Load

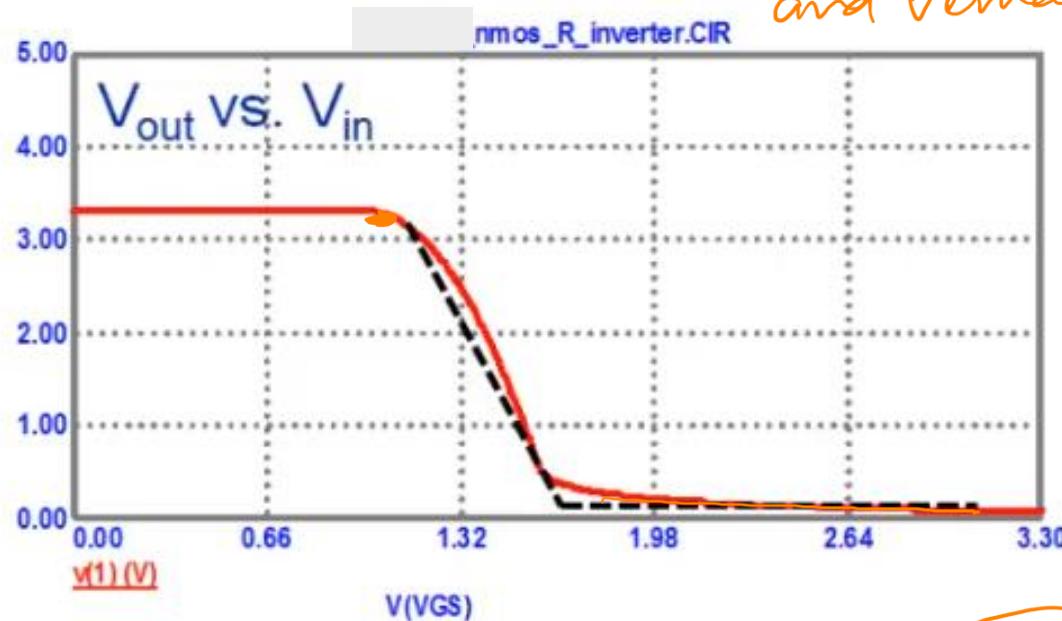


1. Area
2. Delay
3. Power
4. Noise Margins

$$V_{DD} = 3.3V$$

$$K_P N = 100 \mu A / V^2; V_{THN} = 1V$$

$V_{in}=0 \rightarrow \text{MOS is off} \rightarrow V_{out} \Rightarrow V_{dd}$
and remain V_{dd} till V_T ,
 \rightarrow begin to fall



using common
sense

$$V_{OH} = V_{DD}; V_{OL} > 0$$

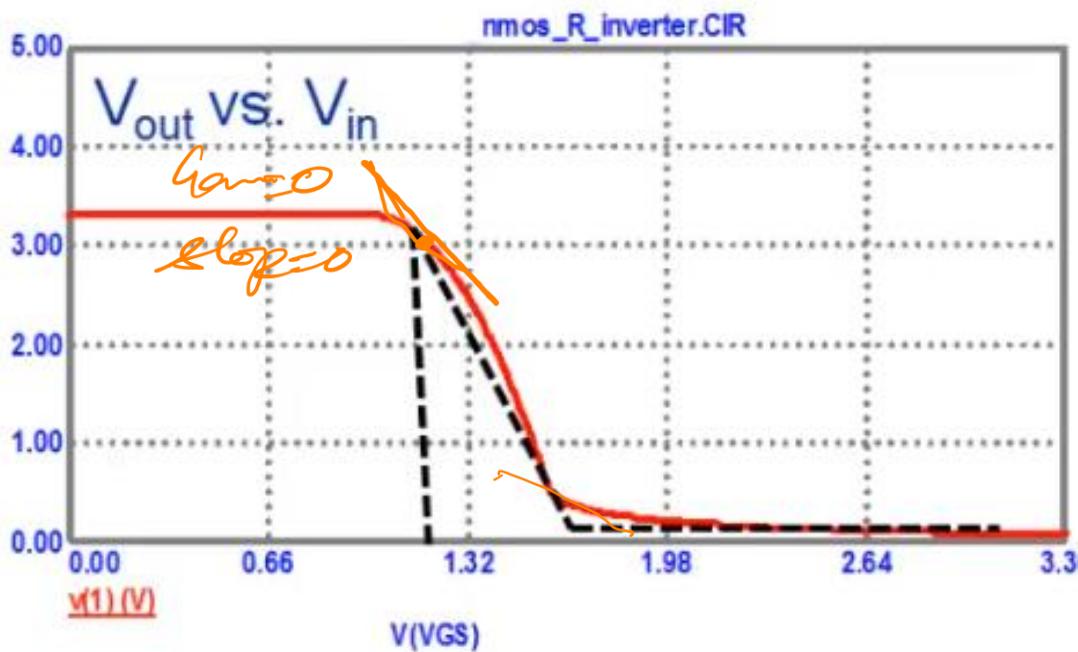
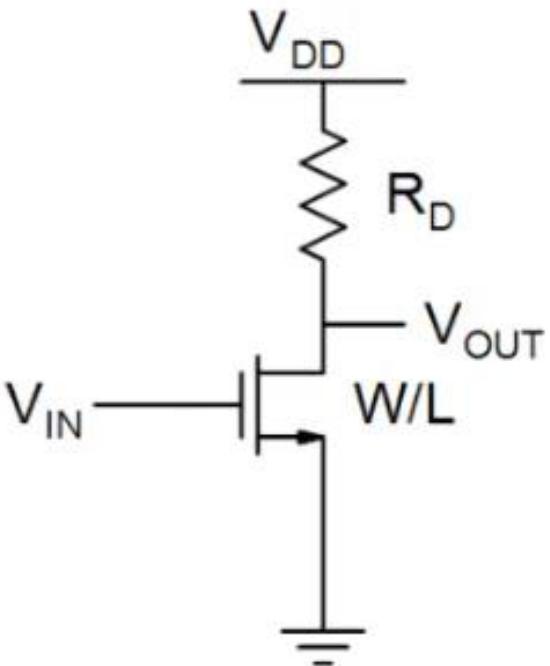
$$I_{DS} \approx \frac{V_{DD}}{R_D} \approx \beta_N \times (V_{DD} - V_{THN}) \times V_{OL}$$

$$\Rightarrow V_{OL} = \left(\frac{V_{DD}}{V_{DD} - V_{THN}} \right) \times \frac{1}{K_P N} \times \frac{1}{(W/L) \times R_D}$$

$$W/L = 4\lambda/2\lambda; R_D = 72k \Rightarrow V_{OL} \sim 0.1V$$

$R \uparrow \rightarrow V_{out}$

Find V_{IL} → place where slope = -1 ; To find $V_{IH} \rightarrow$ find another slope
 Inverter with Resistive Load



Load
1.65

$$KP_N = 100 \mu A/V^2; V_{THN} = 1V$$

$$V_{DD} = 3.3V$$

$$W/L = 4\lambda/2\lambda; R_D = 72k \Rightarrow V_{OL} \sim 0.1V$$

Solve

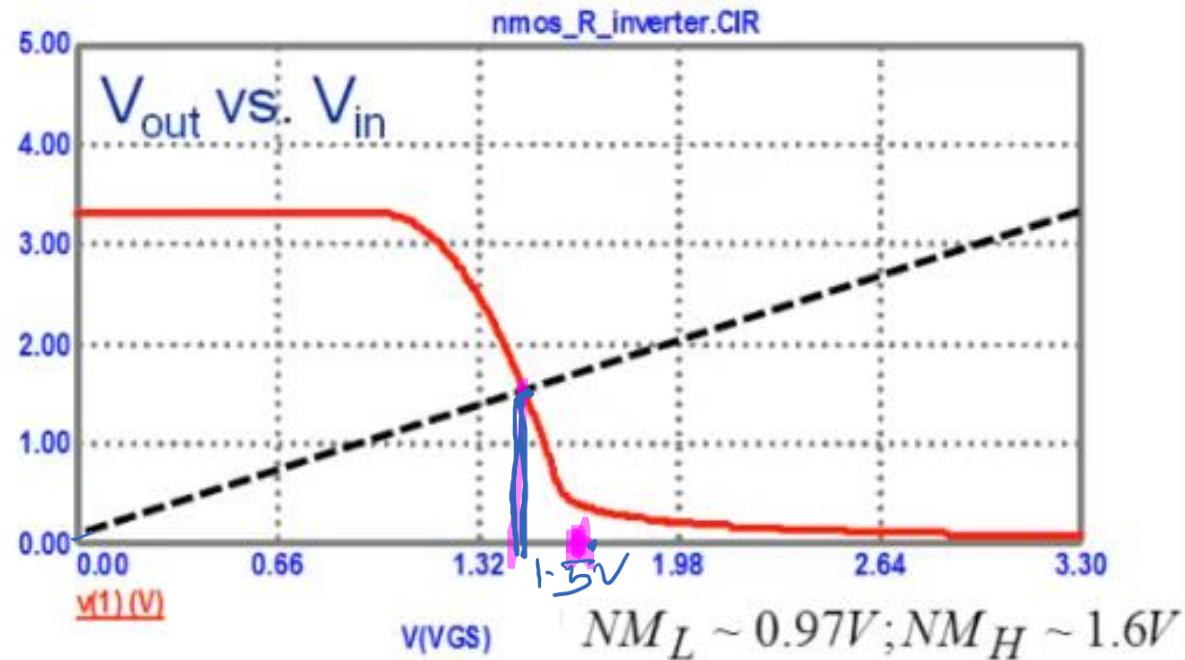
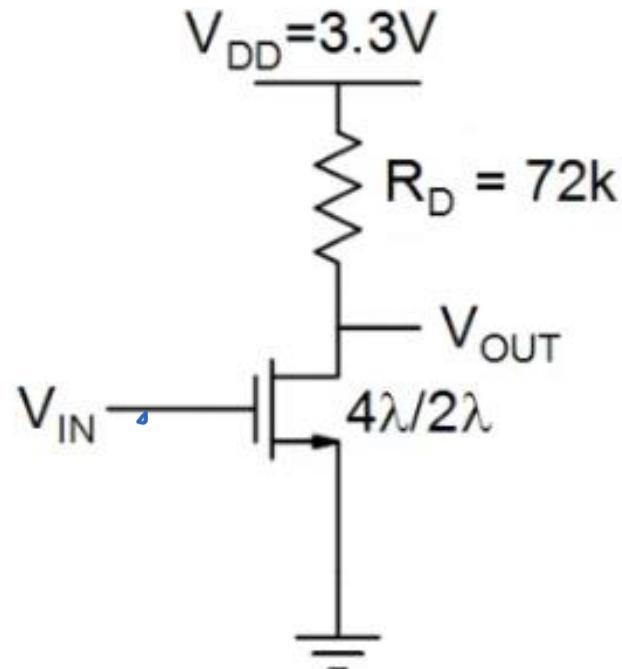
$$\frac{\partial V_{out}}{\partial V_{in}} = -1 \quad \rightarrow V_{IL} \sim 1.07V$$

$$V_{IL} \sim V_{THN} = 1V$$

$$NM_L = V_{IL} - V_{OL} \sim 0.97V$$

$$\frac{NM_L}{0.5V_{DD}} = \frac{0.97}{1.65} = 0.59$$

$$V_{IH} \sim 1.7 \Rightarrow NM_H = V_{DD} - V_{IH} \sim 1.6V$$



$$\underline{V_{out} = V_{in}}$$

Transistor in saturation

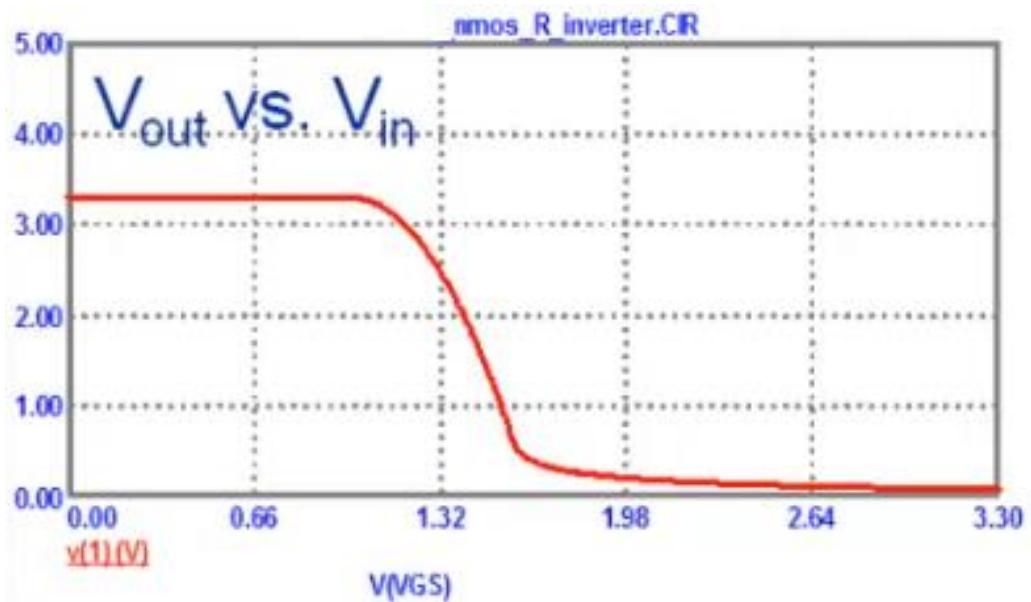
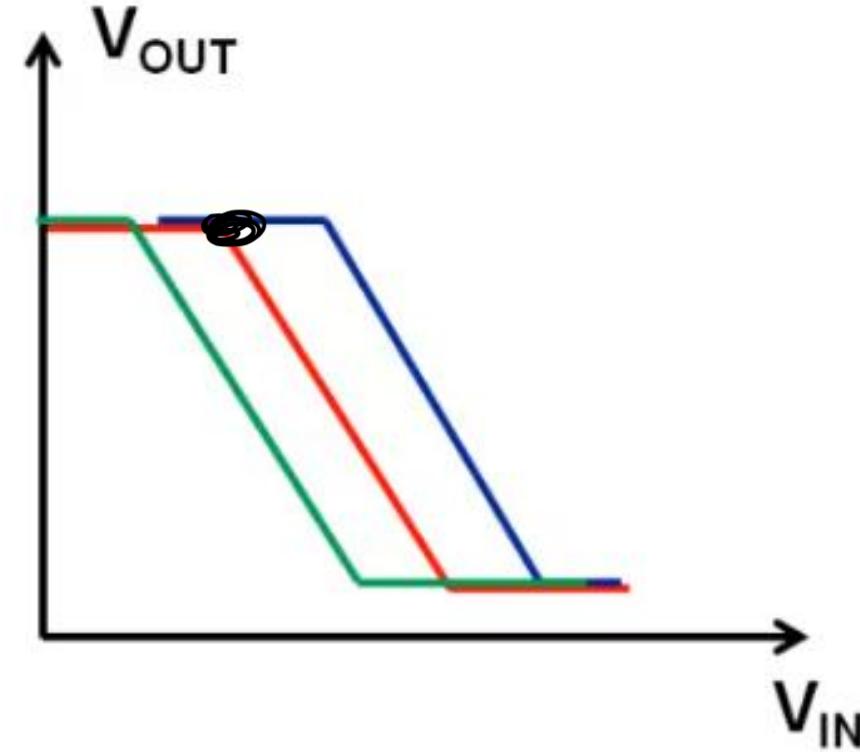
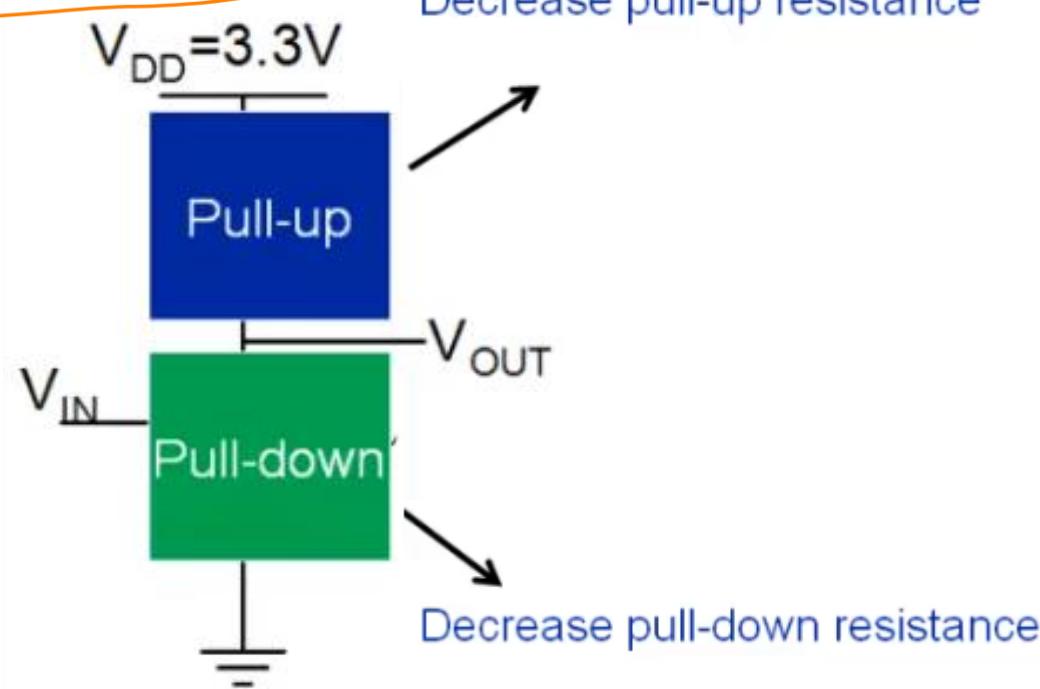
$$I_{DS} = \left(K_P N \times \frac{W}{L} \right) \times \frac{(V_{out} - V_{THN})^2}{2} = \frac{V_{DD} - V_{out}}{R_D}$$

For $R_D = 72k$, $V_{out} = V_{in} = \boxed{V_{inv} = 1.5V}$

Shift characteristics to right to improve NM_L (NM_H will decrease)

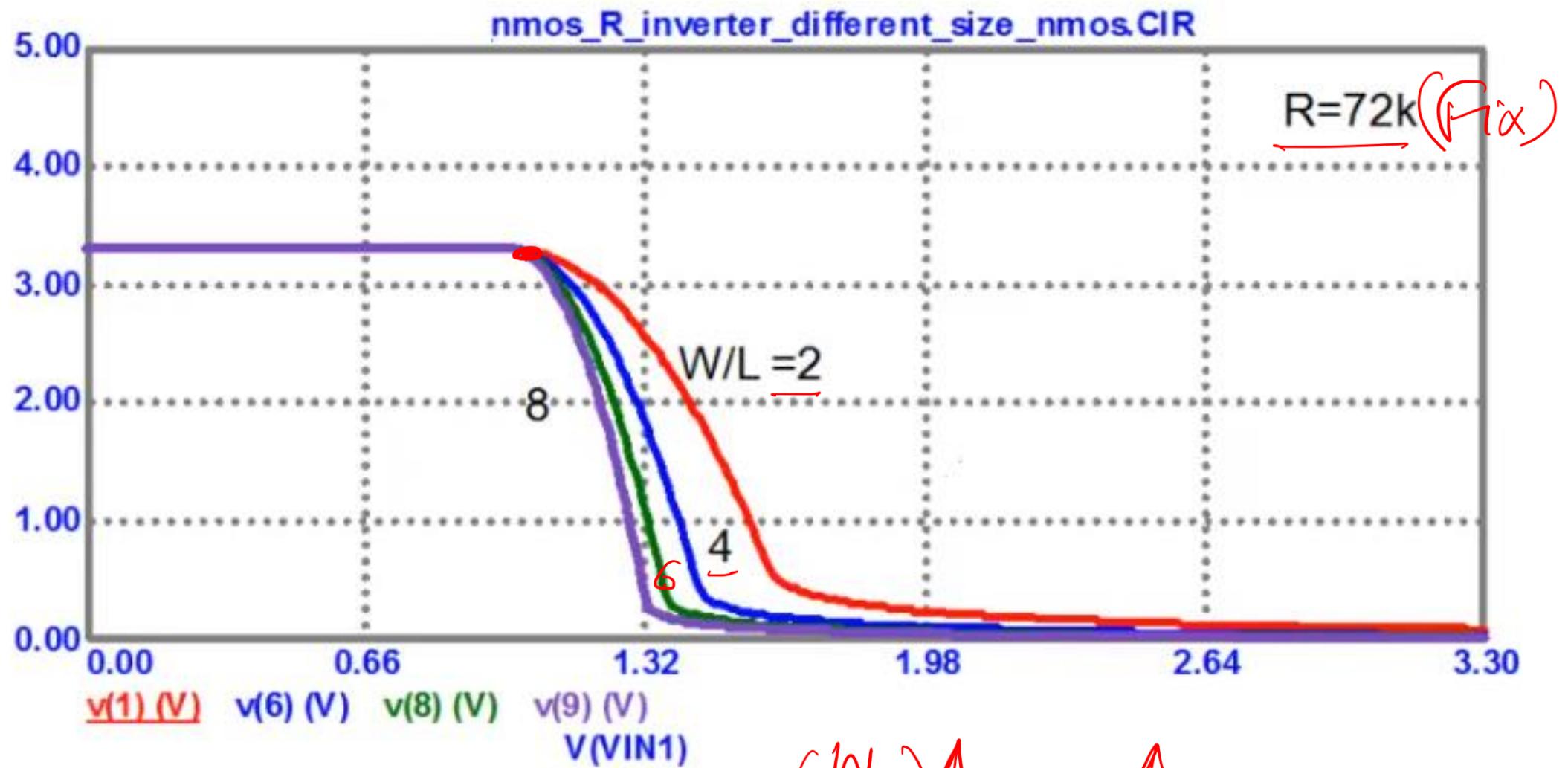
1. Decrease R_D
2. Decrease W/L

General Discussion



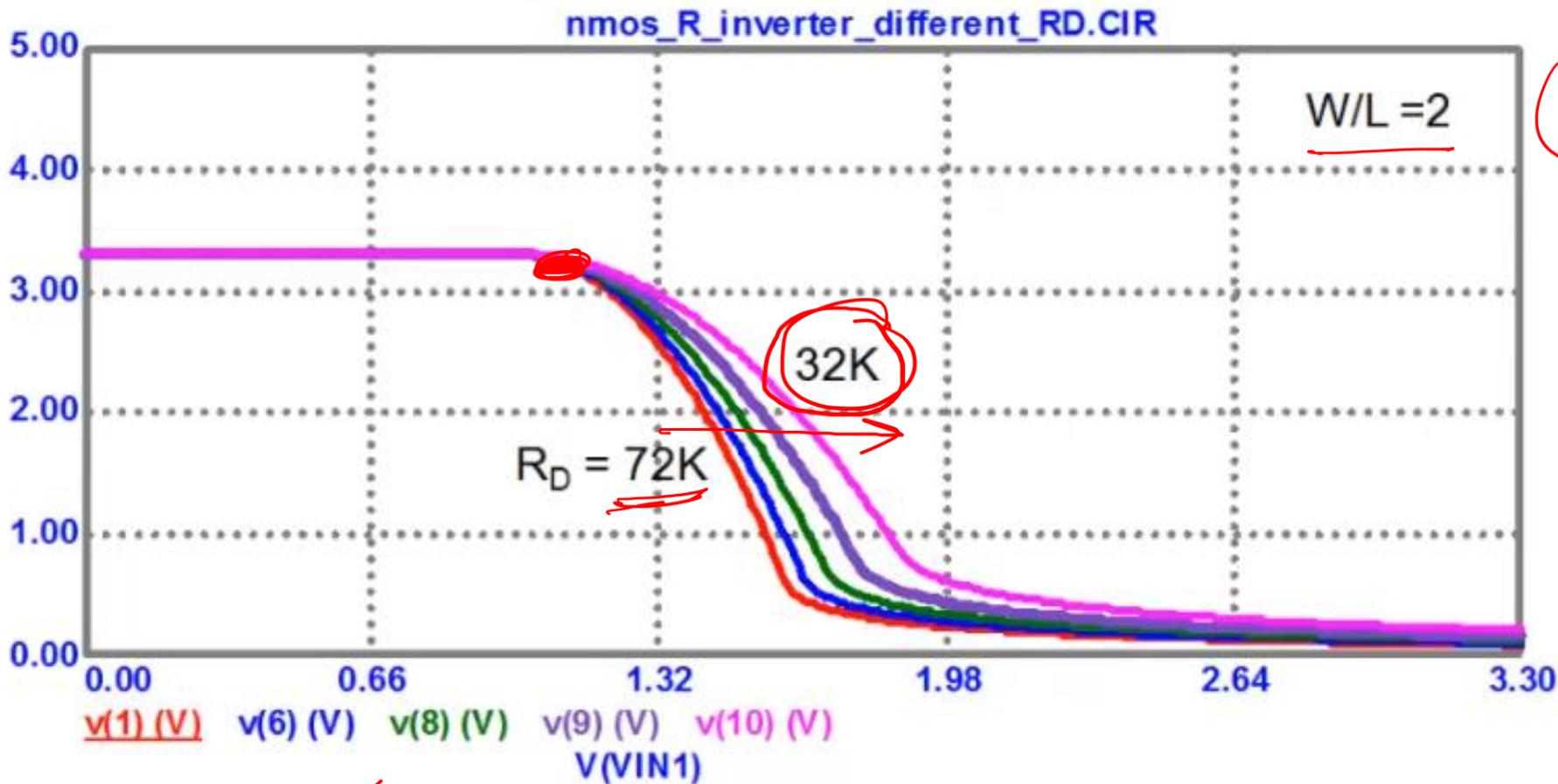
Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L



$$\left(\frac{W}{L}\right) \uparrow \rightarrow I \uparrow \rightarrow R \downarrow$$

Decreasing the pull down resistor shifts characteristics left



$$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$$

$$V_{IL} = 1.07V; V_{IH} = 1.7V$$

$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

$$V_{inv} = 1.5V$$

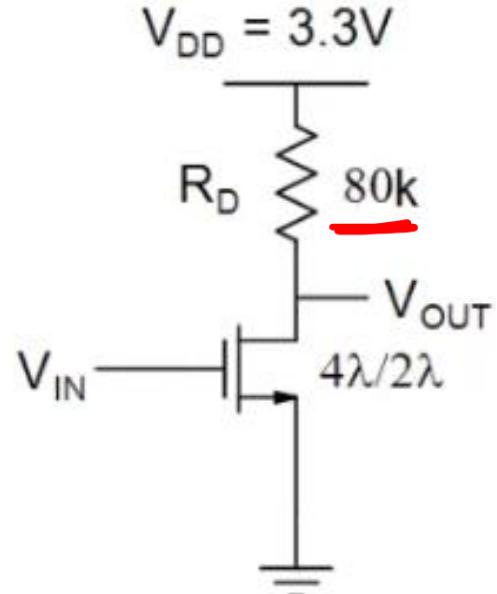
$$R_D = 32k \Rightarrow V_{OL} = 0.22V; V_{OH} = 3.3V$$

$$V_{IL} = 1.16V; V_{IH} = 2V$$

$$NM_L \sim 0.94V; NM_H \sim 1.3V$$

$$V_{inv} = 1.72V$$

Avea ↓



$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

$$R_D = 10k$$

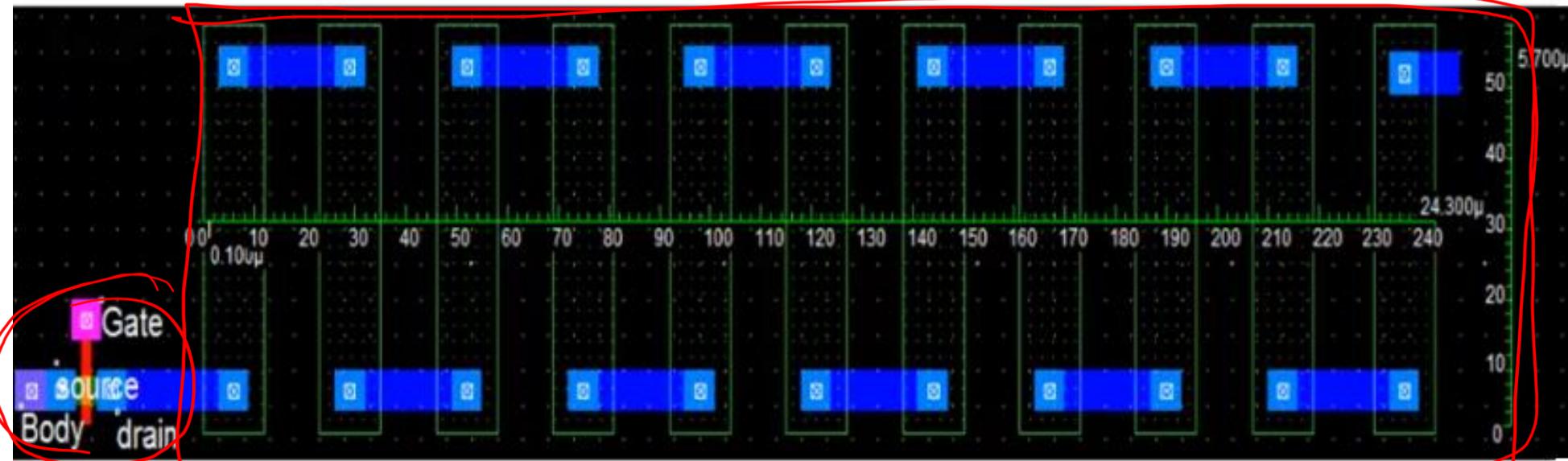
$$W/L = 4\lambda/2\lambda; R_D = 10k \Rightarrow V_{OL} \sim 0.72V$$

$$NM_L = V_{IL} - V_{OL} \sim 0.28V$$

Performance

1. Area
2. Delay
3. Power
4. Noise Margins

Trade off



$$\frac{A_{RD}}{A_{tr1}} \sim 35$$